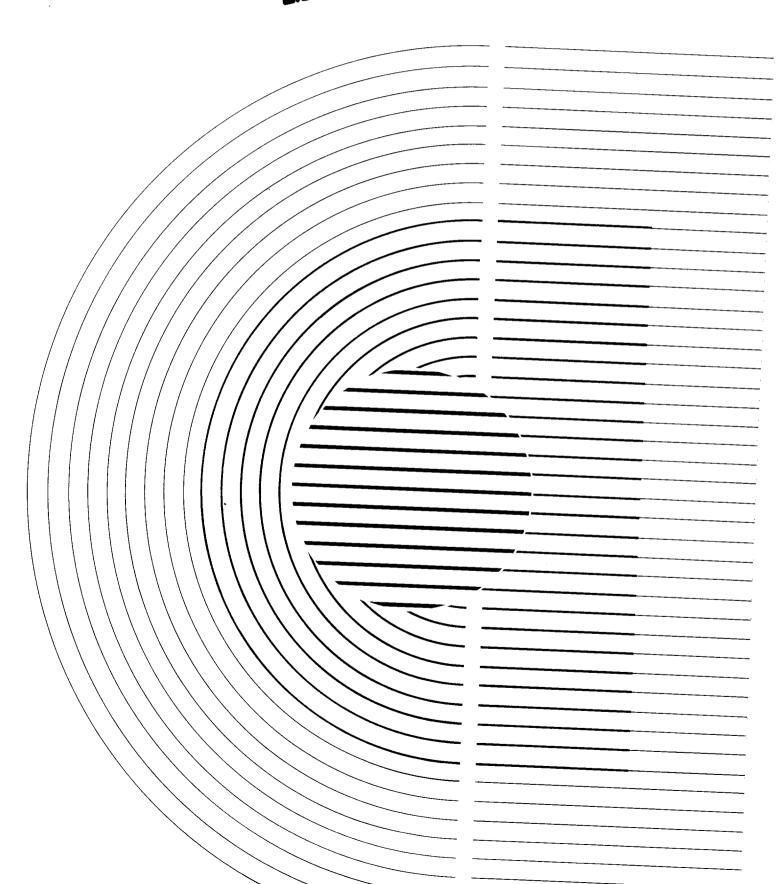


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AHA-1530 User's Manual



4.5 CONFIGURING THE AHA-1530

The AHA-1530 is configurable through jumper settings to operate in a number of application environments. The function of each jumper is shown below.

JUMPER LOCATION

FUNCTION

JID SCSI bus device address	JID JSID	SCSI bus device address SCSI bus device address for an a
ocsi sort/Hard reset option		desir sole/hard reset option

4.5.1 I/O PORT ADDRESSING

The AHA-1530 is addressed through four registers. The base address of these registers is user selectable through jumpers at location JPA. The User can set jumpers for 16-bit or eight-bit I/O address. Installation of a jumper sets the corresponding address bit to a one (1). Unjumpered bits are zero (0).

JPA	Some y	Examples:

16 bit 15 14 13 12 11 10 9 8 7 6 5 4	0	0000000000000	000000000000000000000000000000000000000	8 bit I/O 16 bit I/O 1470H OO O O OO O O O O O O O O O O O O O
2		0	0 0	

4.5.2 MULTIBUS PRIORITY PROTOCOL

For systems using parallel priority, jumper JPR must be removed. For systems using serial priority JPR must be installed.

4.5.3 MULTIBUS RELEASE PROTOCOL

Jumper JCB can be used to select the Multibus release algorithm. If the center pin and pin N are jumpered together, the AHA-1530 will act as if CBRQ* is always driven. It will release the bus after every data transfer.

If the center pin and pin C are jumpered together, the AHA-1530 will use CBRQ* from the Multibus. The AHA-1530, after having won arbitration for the bus, will keep the bus until one of the following events occurs.

- a) CBRQ* rises to indicate another bus drive requires the bus.
- b) PRN* rises to indicate higher priority device requires the bus.
- c) If in block mode, the block transfer count has been exhausted. Block mode is described in Section 3.4.2.2.

4.5.4 MULTIBUS 16-BIT DATA TRANSFER SELECTION

The user can use jumper JD16 to set the Multibus data transfer mode. If jumper JD16 is installed, then data transfers will be 16 bits during DMA transfer. The slave device should have 16-bit transfer capability. The Data Blocks and Controller Command Blocks should be on an even address boundary. If eight-bit operation is required, this jumper should be removed.

4.5.5 VECTORED INTERRUPTS

The interrupt is jumperable to the eight-level vectored interrupt bus VI0* - V17*. The selection of the particular interrupt vector is done by placing a jumper at the correct location on jumber block JVI.

Only one jumper should be installed.

4.5.6 BUS DEVICE ID SELECTION

The Host Adapter can be set to any SCSI Bus Device address, Ø through 7, using jumpers at locations JID and JSID. In a SCSI application, the highest bus address (7) will have the highest priority for bus arbitration. No two SCSI devices can have the same bus address. An example with address = 4 is shown below:

Example ID address = 4

						-		-			
	JID)		JSI	D		JID		JS	ID	
3 2 1	0 0	0 0	0 0 0 0 0 0	0 0 0 0 0 0	7 6 5 4 3 2 1 Ø	3 2 1	0-0	0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0	7 6 5 4 3 2 1 0

Note that jumpers at both JID and JSID must be installed for proper operation of the board.

4.5.7 SCSI RESET SELECTION

The user can select the soft reset mode or the hard reset mode by setting jumper JRST. If the jumper is installed, the Host Adapter will perform a soft reset. The reset mode must be the same as that for all other devices attached to the SCSI. See the SCSI documentation for details of the soft and hard reset condition.

4.5.8 SCSI PARITY

Parity on the SCSI bus is selected with the JPTY jumber. Parity is DISABLED with the jumper in the 'D' position, and ENABLED with the jumper in the 'E' position.





AHA-1530 User's Manual Errata

The microcode for the AHA-1530 has been enhanced to provide additional features. These changes are implemented on all boards with microcode 400063-00B or later.

All changes are listed with reference to the appropriate sections of the AHA-1530 User's Manual.

1.5.3 Operating System Starts I/O

[Change Section 1.5.3]

Figures 1-5B and 1-5C are reversed.

3.2.1 Command Register

[Change Section 3.2.1]

One new Register command has been added to clear the new Received SCSI Reset Status Register Bit. This bit is defined under Section 3.2.2.

05H Clear SCSI Reset Status Bit

3.2.2 Status Register

[Change Section 3.2.2]

The Status Register has been redefined as shown below:

Bit 7	Operation Complete = 1 , Not Complete = 0
Bit 6	Command Register Empty = 1, Not Empty = 0
Bit 5	Mailbox in Overflow = 1
Bit 4	Installed, Always = 1
Bit 3	Invalid Register Command = 1
Bit 2	Power On Self Test Complete = 1
Bit 1	Received SCSI Reset = 1
Bit 0	Initialization Required = 1

The three new Status Register Bits are defined below:

- Bit 3 Invalid register command. This bit is set when an invalid command is written to the register. It may be cleared by issuing a valid command.
- Bit 2 Power On Self Test complete. Self test diagnostics are run at power on. This bit is set after they have been completed successfully.
- Bit 1 Received SCSI Reset. This bit is set after the AHA-1530 receives a SCSI Reset.
 This bit is cleared by issuing the Clear SCSI Reset Status Bit Register Command.

3.4.2 Host Adapter Command Block

[Change Section 3.4.2]

Five commands are presently defined (two new commands have been added):

• Reset SCSI Bus Device

- Firmware Revision Level
- Set Host Bus Transfer Period
- Bus Release Time

• Set SCSI Timeout Period

All other command codes are reserved.

3.4.2.4 Firmware Revision Level

[Add new Section 3.4.2.4]

The ACB-1530 will return four ASCII-coded alphanumeric characters to the area indicated in the command block.

-2-

Byte	Contents
0	8СН
1	MSB Host Adapter Firmware Revision Level
2	
3	
4	LSB
5	Reserved
6	Reserved
7	Reserved

3.4.2.5 Bus Release Time

[Add new Section 3.4.2.5]

The ACB-1530 can be forced to release the Multibus during command and data transfers at a programmed time interval. The equation for programming the time interval is shown below:

T = 20 s + N * 70 s where N = 1 to 255

Byte	Contents
0	91H
1	0 = Disable timer
	1 to 255 = Set timer to value and enable
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved

Note: Programmable Bus Release timing is only functional on part number 411100.

3.4.3 Error Reporting

[Delete table in Section 3.4.3 Replace with following table]

Host Adapter detected errors:

ErrorCode (hex)	Definition
00	No error
01-0F	Adaptec reserved
10	SCSI Selection timeout - Selection timeout has not been disabled, and the target device has not responded to selection within the allocated time.
11	Bus activity timeout - Multibus signal XACK* not received within the user-specified timeout period
12	SCSI parity error

Error Code (hex)	Definition		
13	First Message-in after Reselect is not Identify		
14	Message-in after date phase is not Disconnect and next phase is not Message-in		
15	Byte count underrun - Length limit control field (Controller Command Block: byte 26, bits (0,1>) is 01h and the Status phase is entered with less than the requested number of data bytes transferred.		
16	Invalid Message received from target. The Host Adapter will assert SCSI Reset		
17	No response to SCSI Attention signal		
18	First phase after Reselect not Message-in		
19	No response to Attention asserted to send Bus Device Reset message after Selection		
1A	No Message-in phase after Status phase		
1B	No response to Attention asserted to send Bus Device Reset message		
1C	No Status or Message-in phase after the end of transfer		
1D	No response to Attention asserted to send Abort message		
1E-FF	Adaptec reserved		

[Add new Sections 3.4.4, 3.4.5, 3.4.6, and 3.4.7]

3.4.4 Parity Error on SCSI Bus

If a parity error is detected at any time, the Host Adapter will attempt to send an 05 message (Initiator-detected error) to the target and will record a Host Aadapter error sense byte of 12H.

If there has been no response to the attention condition when the command complete message has been received, the Host Adapter will report error code 17 H (no response to attention) in the Host Adapter status byte.

3.4.5 Reselect by Target With No Outstanding Command Queue Entry

ATTENTION is raised and an ABORT message is attempted to be sent to the target device. All transfers not in the Message-out phase will be thrown away.

3.4.6 Message-in Phase

If an extended message (02H) is received, a message reject will be sent.

If a message reject message (07H) is received, an ABORT message will be sent.

3.4.7 SCSI Reset Conditions

Reselect — First phase is not Mesage-in

Reselect - Not ID msg

Select timeout, then BUSY is asserted.

Two Message-in bytes after transfer is done, the first byte is not a disconnect message.

Data transfer timeout.

No Message-in phase after status phase.

No Message-out phase during a device reset.

Invalid messages received. If a message is received from the target that by definition can only be received from an initiator, or indicates a fatal condition, a RESET is issued. These messages are 05H (Initiator-detected error), 06H (ABORT), 09H (Parity error on MSG transfer), 0CH (Bus device reset).

No status or Message-in phase after data transfer.