Bugs in Black and White: Imaging IC Logic Levels with Voltage Contrast

Voltage contrast imaging allows visual tracking of logical level problems to their source on operating integrated circuits, using a scanning electron microscope. This paper presents an overview of voltage contrast and the methods developed to image the failure of dynamic circuits in the floating-point coprocessor circuitry of the HP PA 7100LC processor chip.

by Jack D. Benzel

As pressure for higher performance and higher integration drives integrated circuit design towards increasing complexity, IC designers need an ever-broadening set of analysis and debugging tools and methodologies for tracking down functional bugs and electrical margin issues in their designs.

In developing the new HP PA 7100LC PA-RISC microprocessor chip, the floating-point arithmetic logic unit (FPALU) megacell used design techniques based on the PA 7100 design.[1] The FPALU design is implemented with mostly mousetrap-style dynamic logic[2] with significant use of single-ended dynamic logic in the last pipeline stage.

Past experience in debugging electrical problems in mousetrap designs has shown these problems to be very difficult to find.[3] A failure mechanism that emerged in prototypes of gate-biased PA 7100LC FPALUs proved highly challenging and evasive and required a large engineering effort to get from detection to the root cause identification. The voltage contrast imaging methodology proved useful in analyzing and later confirming the root cause of the failure mechanism. Results from the analysis allowed us to correct the design and verify its quality.

The Wall

The FPALU failure mechanism was named "the wall" because of its appearance on a frequency-versus-voltage shmoo plot depicting regions of passing and failing vectors (see Fig. 1).

Considerable engineering resources were applied toward finding the root cause of the wall using many of the techniques that had proved successful on previous design projects, including but not limited to shmoo plots, failing vector/opcode analysis, clock phase stretching, focused ion beam (FIB) experiments, and simulations of probable circuit failures.[3] These techniques were not providing enough information, and a new methodology was clearly needed.

Why Voltage Contrast?

Another HP design team had recently had success in using an electron-beam prober[4] to track down the root cause of a noise problem on the same CPU chip.

Previous experience with another project several years ago provided insights into a methodology similar to electron-beam probing called voltage contrast, using a scanning electron microscope (SEM). After considering the various trade-offs it was decided to proceed with the voltage contrast imaging while keeping open the option of going to electron-beam probing if further analysis was required.

SEM Fundamentals

The SEM displays objects by sensing and imaging the release of secondary electrons from the surface of a sample which is held in a very high vacuum. A finely focused beam of electrons accelerated from an electron gun with a thousand-volt potential is swept over the surface of the sample in much the same way that a television screen is scanned. As the high-energy electrons in the beam strike the sample, several valence electrons will be "knocked loose" from the sample as the impinging electrons lose energy. These now-free electrons, or secondary electrons, find their way to the surface of the sample and are released from the surface. A highly biased metal screen situated near the sample collects escaping secondary electrons into a detector which generates a signal proportional to the number of electrons collected. The signal from the detector is amplified and displayed on a CRT screen which is scanned in synchronization with the electron beam sweeping the sample.

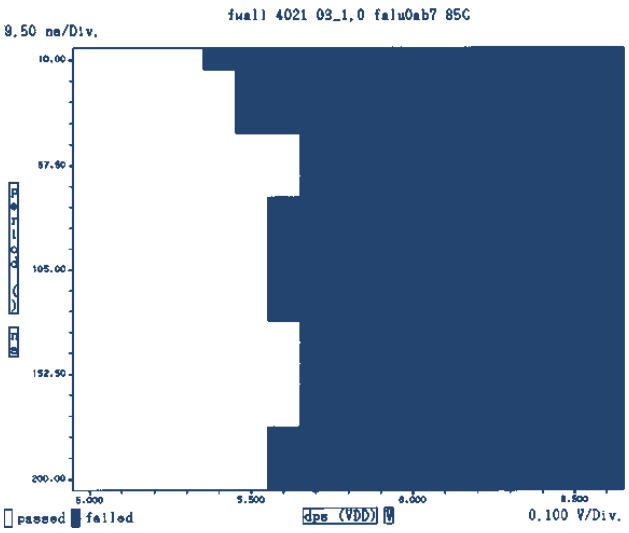


Fig. 1. Shmoo plot of "the wall."

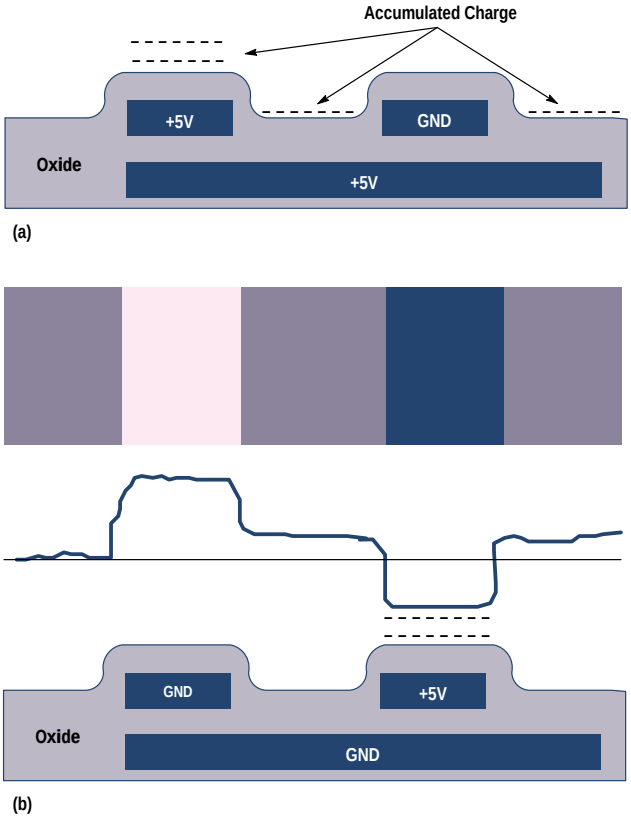


Fig. 2. (a) First pass "charge" of IC surface with secondary electrons. (b) Second pass "read" of charged surface (bottom), resulting video signal (middle), and 2D video image (top).

Voltage Contrast Imaging

Voltage contrast imaging uses the electrical nature of the SEM to view voltage potentials on a sample changing with time. Figs. 2a and 2b show a cross section of the top two metal signal layers of an IC with the metal lines insulated by an oxide.

The imaging is done in two stages: charging and reading. Fig. 2a shows the state of the IC at the end of the charging stage. The positive potential of the buried metal lines attracts and holds the generated secondary electrons on the surface of the oxide above the metal lines. These charges will remain on the surface for long periods of time, basically acting like a capacitor.

Fig. 2b shows the state of the IC at the end of the read stage with the voltage potentials of the metal lines now changed. The resulting detector signal level and the CRT image generated from it are also shown above the cross section. As the electron beam sweeps the surface of the sample, the electrons that were once held by the positive charge of the upper-left and lower metal lines (Fig. 2a) are knocked off the surface and are collected into the detector, generating a bright signal on the CRT. On the other hand, the upper-right metal line is now more positive, and the surface above it will release fewer secondary electrons as the surface capacitively charges, corresponding to a lower number of electrons collected and thus a darker signal on the CRT.

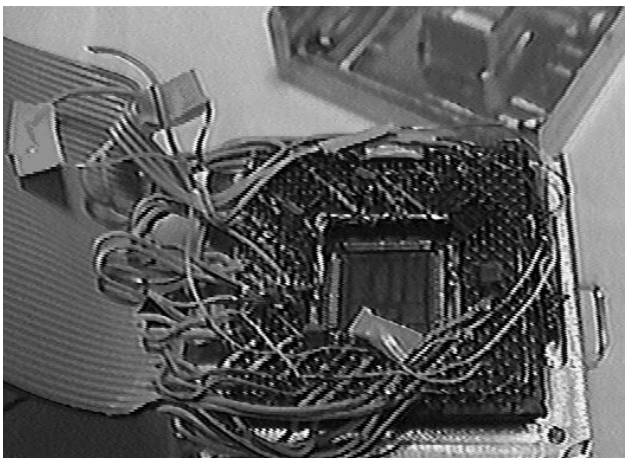


Fig. 3. Video image of DUT fixture for voltage contrast setup with top shield removed.

DUT Preparation

Preparing the IC for the SEM environment required careful attention to several details as follows:

- *Clean Power Environment.* Some previous experiments indicated that the wall was somewhat remedied by a power environment that restricted the V_{DD} current supply. Therefore, careful attention was paid to provide adequate low-inductance power feeds with adequate decoupling capacitance.
- *Simple Vector Stimulus.* Restricted cabling into the SEM chamber and easy portability between two different SEM facilities required a simple method for executing a wall-sensitive floating-point operation (FLOP). A successful method was developed to launch and step through the phases of a FLOP using the JTAG†-conforming serial test port and a serial test board.
- *Image Capture Synchronization.* The capture and imaging of events on the SEM system requires a synchronizing signal generated by the device under test (DUT). Several small surface mount ICs were mounted on the PA 7100LC package to decode the clock signals and derive another synchronizing signal to provide the SEM with an accurate sync pulse that identified the leading clock edge at the starting phase of the failing FLOP.
- *Minimize Outgassing.* To achieve an adequate vacuum in the SEM system, materials that had minimal outgassing were required. This prevented the use of heatshrink tubing and quick-cure epoxies and required careful cleaning of the DUT.
- *Packaging.* The packaging fixture containing the CPU (see Fig. 3) met several requirements. The wall was a high-temperature phenomenon and required heating the part inside of the SEM with large resistors mounted inside the fixture. The metal enclosure shielded all but the die surface from the electron beam, since the beam will positively charge plastics (wiring, capacitors). The shield also prevented electrical signals in the DUT wiring from interfering with the beam's trajectory. The last requirement filled by the fixturing was a compact size to fit inside the small SEM chamber.

† JTAG is the Joint Test Action Group, which developed IEEE standard 1149.1, *IEEE Test Access Port and Boundary-Scan Architecture.*

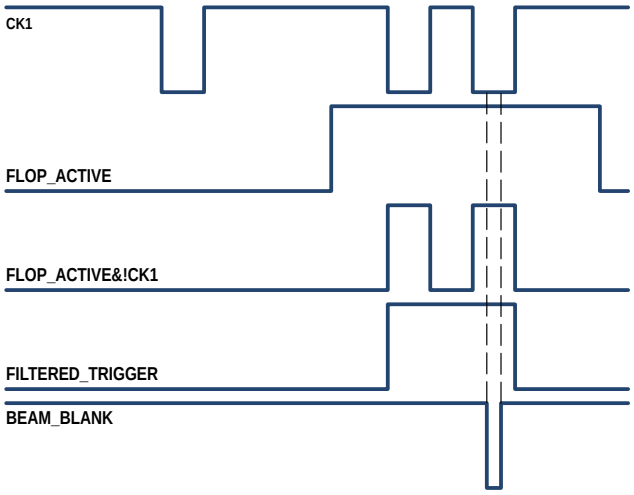


Fig. 4. Beam blanking and synchronization signal generation.

Imaging Dynamic Signals

The electron beam scan is synchronized with the scan of the video display tube and consequently has a slow refresh rate of 1/60 second. This slow refresh rate works well for stationary objects and static electrical signals, but the signals of interest involved in the wall failure are dynamic, typical of mousetrap designs. The imaging of dynamic signals required the development of a new process.

Synchronization and Beam Blanking

The slowest rate at which the DUT could be clocked with reliable operation of the scan path driven through the JTAG port was 2.5 MHz, giving a 200-ns phase or period during which dynamic signals would be active. Connecting a pulse generator to the DUT's sync pulse allowed the generation of a variable-width, variable-delay pulse (see Fig. 4) which was used to blank the electron beam scanning the DUT. Using this blanking signal, the SEM could be controlled to charge or read the IC only during the time of interest when the wall-related signals were active. A 100-ns sample window was chosen for the blank signal, which was centered in the clock phase to reduce possible overlap into adjoining phases.

Once the beam was properly synchronized and blanked, the apparent lack of information in the video image shown in Fig. 5 gave a strong indication that more development was needed.

Image Capture

The next problem to resolve was imaging the brief 100-ns video information successfully. Several ideas were evaluated and tried before an acceptable method was found:

- *Photographic Film Integration.* The SEM focuses the light from a secondary CRT onto the film plane of a Polaroid camera over a period of several minutes while exercising the DUT. This method resulted in either completely black or very indistinct images of the IC.
- *Two-Dimensional Scan.* The SEM can operate with basically a zero-frequency vertical scan rate. This provides an image of a single horizontal slice of the IC surface while improving the refresh rate. Changes in beam intensity were undiscernible in this mode.
- *Two-Dimensional Scan in Oscilloscope Mode.* Using the same two-dimensional scan mode as above, the intensity vector of the SEM's display can be used to drive the vertical component of the video signal. The resulting image is reminiscent of an oscilloscope display showing intensity on the y axis. No discernible changes in intensity were visible in this mode as well.
- *Two-Step Charge/Read.* Instead of trying to charge and read on each or every other FLOP, the process was broken into two steps. The first step involved turning the beam on only during the phase of interest while the part was executing wall FLOPs over a period of three minutes. A long integration time was required because each time the beam turned on it only charged a tiny area of the field of view. At the end of the integration time, the beam was turned off, the IC powered down, and the beam blank removed from the SEM. The IC now had a surface charge that reflected the state of the metal lines during the phase of interest. The second step was to turn the beam on with no blanking to read the surface charge in its first pass over the IC. The resulting video image was clear but brief (one video frame). This process produced an image in which metal lines with a positive voltage were white and metal lines at ground were black. Another small variation in this process was not to power down the part before the read step. The resulting image took a little more thought to interpret because only the metal lines that changed state from the previous step were black or white.
- *Two-Step Charge/Read with VCR Frame Capture.* By adding a VCR to the setup, the resulting video image fed to the CRT could be captured on tape and then freeze-framed for viewing. The purchase of a VCR with a forward and reverse single-frame jog shuttle control greatly aided in isolating the image captured on a single frame. It was apparent from the videotape that the majority of the IC's surface charge was removed in the first sweep of the beam across the die area. This last methodology was used successfully for imaging the dynamic signals in the FPALU.

Results

Once the methodology was established, over 120 images were captured and catalogued on video tape over a four-week period. Several days were spent at the outset trying to understand why an active clock line in the imaged phase

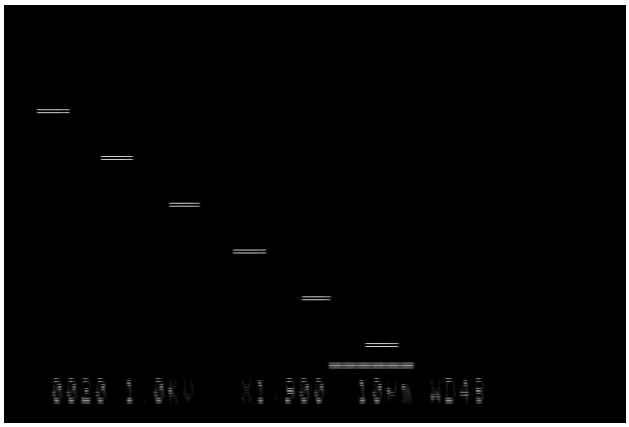


Fig. 5. Video image of the first-pass imaging attempts.

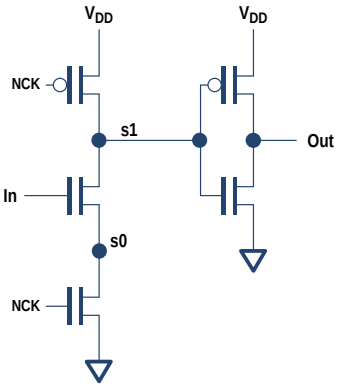
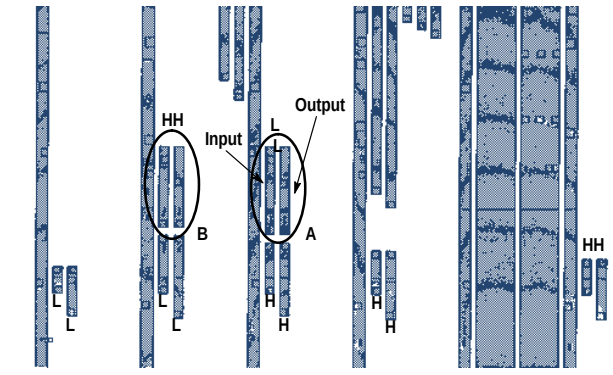


Fig. 6. Zero_topH mousetrap buffer.

was not showing activity, a key indicator that the proper phase of the FLOP was being captured. This issue was never satisfactorily resolved, yet phase-by-phase clock gating in the FPALU ensured that the signals would only be active and thus visible in the phase of interest.

Figs. 6, 7a, and 7b show the schematic, artwork, and voltage contrast image of probably the clearest failure identified. The circuit in Fig. 6 shows a mousetrap buffer whose storage node, s1, was somehow being compromised, possibly through a ground differential problem or a noise spike on the input.



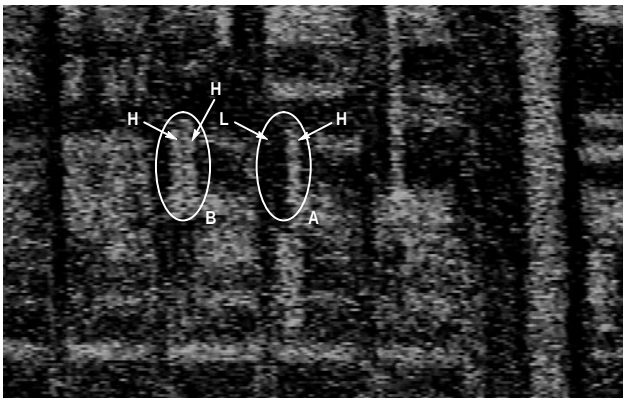


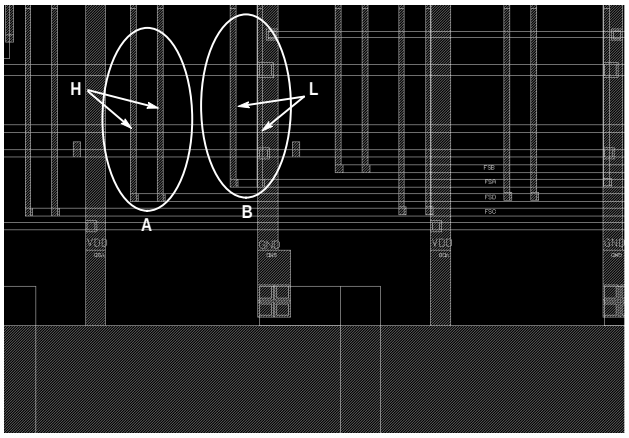
Fig. 7. (a) Metal 3 plot of Zero_topH buffer with failing input/output pair A. (b) Voltage contrast image of victimized buffer with failing input/output pair A.

Circle A in Fig. 7a identifies the buffer's input on the left and the output on the right. The expected value of each metal 3 line is indicated above the lines (L=Low, H=High).

Fig. 7b shows a voltage contrast image captured from the videotape showing the failure of the buffer. The image clearly shows a low level on the input (black) and a high level (white) on the output of the buffer in circle A. Note the difference between circle A and circle B which identifies the input and output of an identical buffer with no failures. It became clear from this picture that the electrical event that caused the buffer to output a high level was transitory in nature and not a static event. The read step of the image was taken with the IC powered down.

Metal 1 and even metal 2 lines can be difficult to image unless they are well-isolated from other metal structures. Fig. 8a shows the artwork and expected values where several metal 1 lines were imaged. The vertical metal 1 route in circle A should have a high or white level, and the route to the right of it in circle B should have a low or black level.

Fig. 8b is the voltage contrast image showing the logical misfiring (high/white) of the metal 1 route in circle B. This



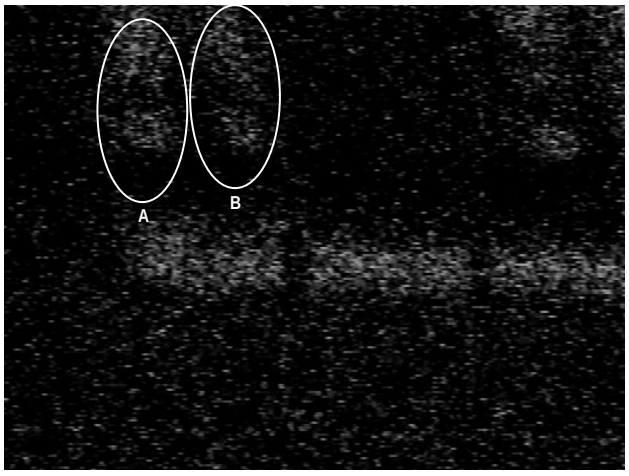
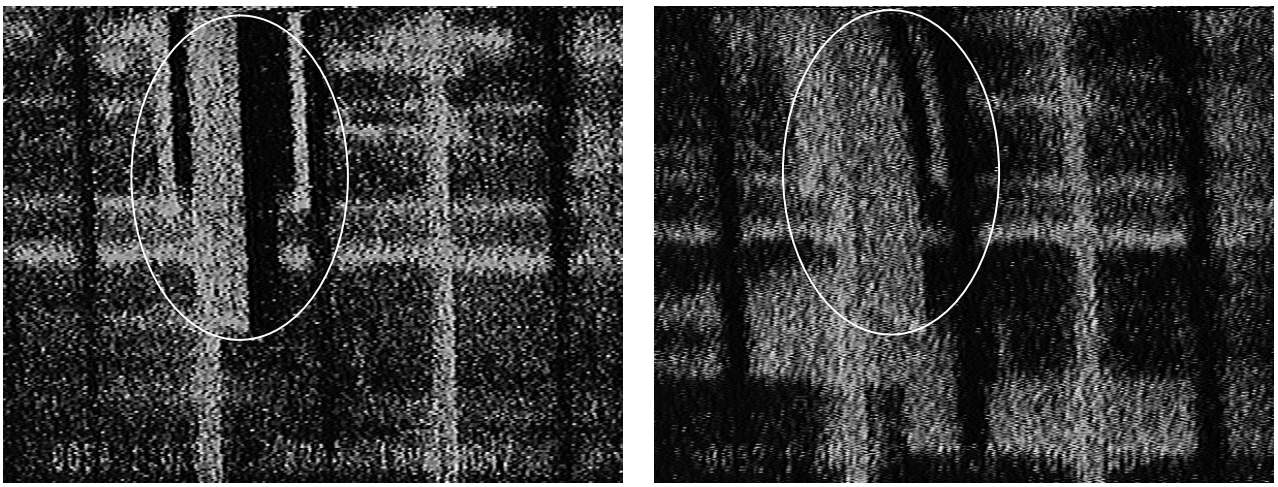


Fig. 8. (a) FS[ABCD] bus artwork. (b) Voltage contrast image of FS[ABCD] bus in metal 1 showing correct firing of the lines in circle A and the incorrect firing of lines in circle B.



(a) (b)

Fig. 9. (a) Metal 3 structure(vertical routing) in passing state at nominal voltage. Horizontal routes are metal 2. (b) Metal 3 structure in failing state at high voltage with wall failure.

failure was not seen until the root cause of the wall was identified and the proper FLOP for arming the failure was identified.

The logical states of individual lines of dense bus structures in lower metal levels can be difficult to discern, yet differences between two states can often be readily identified.

Figs. 9a and 9b illustrate the differencing technique with an example of a metal 3 structure in both a passing and failing state (note the differences in the vertically routed lines in the top-center of the figures). The bend or distortion in Fig. 9b is the result of poor synchronization between the SEM and the VCR that recorded the images. Note also the changes in the horizontally routed metal 2 lines.

One technique that greatly aided the interpretation of the captured images was to plot the artwork of the areas being imaged and annotate the plots with the expected logical levels as derived from a simulator.

Improvements and Future Use

It is difficult to determine if E-beam probing would have provided quicker, more pertinent information than voltage contrast. Each tool has its own benefits and drawbacks that the IC designer must weigh in light of the problem to be solved.

Additional IC physical structures and layouts could make new designs more amenable to voltage contrast imaging as well as E-beam probing and FIB experiments. These features could provide regular, systematic, top-level-metal access to control and data path signals throughout the design. Top-level-metal access could be provided through directed routing or through "via stacks" to top layers from lower-level metal routes. The efficiency of such features in terms of improved accessibility versus increased layout area is unknown.

The image quality obtained from the SEM for voltage contrast work could be improved by changing the electron gun filament from tungsten to a crystalline element. The crystalline filament would increase the beam current and thus effectively provide a brighter image without increasing the beam energy which reduces resolution.

Conclusions

The use of voltage contrast imaging proved to be a useful tool for analyzing and verifying the FPALU margin failure known as the wall. Although the information gleaned from the process did not lead directly to the discovery of the root cause of the failure, the voltage contrast process functioned well as a clue generator as suggested in reference 3 and provided important confirmation of the root cause hypothesis.

Acknowledgments

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