Designing, Simulating, and Testing an Analog Phase-Locked Loop in a Digital Environment

In designing a phase-locked loop for use on several HP ASICs, the digital portion of an existing phase-locked loop was transferred to a behavioral VHDL description and synthesized. A behavioral model was written for the analog section to allow the ASIC designers to run system simulations. A new leakage test was developed that has been very effective in screening out process defects in the filter of the original design.

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This paper describes the design and integration process for a phase-locked loop that is being used on several current HP ASICs (application-specific integrated circuits). The design is based on the phase-locked loop for a previous ASIC, but several improvements were made. First, the digital portion of the phase-locked loop was transferred to a behavioral VHDL* description and synthesized. Reusability was a big consideration in writing the code. The portable nature of the VHDL code enabled us to design several phase-locked loops within a very short time. Second, a behavioral model was written for the analog section to allow the ASIC designers to run system simulations. This model, when combined with the model for the digital section, allows the designer to simulate the phase-locked loop as it locks—it does not merely put out an ideal clock waveform. Finally, in a previous ASIC, a large resistor and capacitor in the loop filter were not adequately tested. For the new phase-locked loop, we developed a leakage test that has been very effective in screening out process defects in the filter.

An analog phase-locked loop presents several challenges to designers in an all-digital design environment. Some all-digital simulators, such as Verilog XL, cannot represent analog signals easily. System designers must either use a mixed-mode simulator to represent the analog portions of the phase-locked loop, or use a simplified model of the phase-locked loop. In ASIC production test, limitations of the production test equipment must be taken into account. For example, an analog measurement may take a long time to complete. Also, functional testers cannot measure frequency, so it is difficult to determine that the phase-locked loop is operating properly in production test.

Previous Phase-Locked Loop Design

The previous phase-locked loop design appeared on an ASIC, where its purpose was to accept an input clock (the video clock) and generate the system clock. The clock signal output from the phase-locked loop was modulated so that the output clock frequency alternated back and forth

between two frequencies slightly above and below the target system clock frequency. This frequency modulation of the system clock was required by the system in which the previous design was used.

The block diagram of the previous phase-locked loop is shown in Fig. 1. The loop consists of an input counter (divide-by-M), a feedback counter (divide-by-N), a phase-frequency detector, a charge pump and filter, a voltage-controlled oscillator (VCO), and other digital control logic. The input counter divides the input clock by either M_{high} or M_{low}. It produces an output pulse (FREF) that is low for one clock cycle and high for the remaining time. The feedback counter divides the VCO output by N_{high} or N_{low}. It produces an output pulse (FBAK) that is low for two clock cycles. The phase-frequency detector examines the relative phase of the rising edges of the FREF and FBAK signals and generates pulses on the UP and DOWN signal lines. The charge pump uses these pulses to adjust the control voltage for the VCO. The output signal is generated by dividing the VCO output clock by 4. The resulting phase-locked loop output frequency is given by:

$$f_{out} = \frac{1}{4}\left(\frac{N}{M}\right)f_{in}. \qquad (1)$$

* VHDL stands for Very High-Speed Integrated Circuit Hardware Description Language.

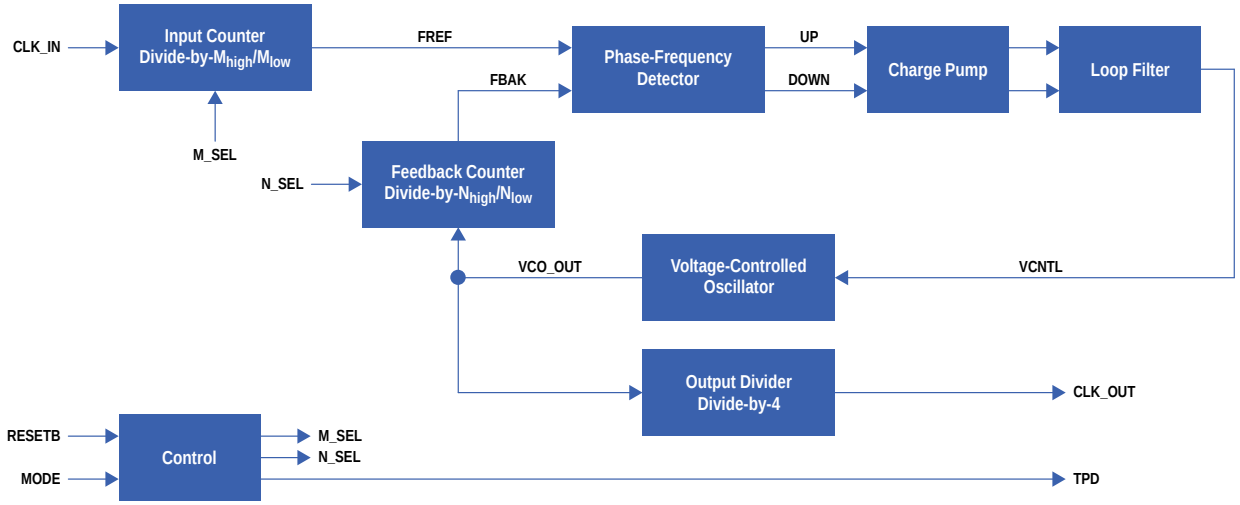

Fig. 1. *Block diagram of the original phase-locked loop design.*

The control block consists of logic that selects one of the operating frequencies. A state machine in this block controls the modulation between the upper and lower frequencies. In normal mode, the control logic sets the phase-locked loop to the upper frequency when it is reset. The loop remains at the upper frequency until the control block receives a signal that indicates that the loop is locked. After this, the loop alternates between the upper and lower frequencies. This is controlled by the N_SEL and M_SEL outputs of the modulator counter.

There were two main problems with the integration of the phase-locked loop. The first problem was that there was no model of the phase-locked loop in VHDL or Verilog that could be used for system simulation. Therefore, no simulations were run with the clock generated by the phase-locked loop. All simulations were run with an external clock, using a different chip mode. This caused the design team to miss a serious bug in the design. When the mode pins were set to enable the phase-locked loop, one block inside the chip was accidently set into scan mode. This problem was not caught until the first prototype parts were placed on a board.

The second problem encountered with this phase-locked loop design was a high production line failure rate. The phase-locked loop tests were not catching all the defective parts. Analysis of the returned parts showed that the failures were caused by defects in the resistor and capacitor in the loop filter, which caused excessive leakage, changing the filter characteristics. The production tester had no way to test for this, so a new test had to be created. Here the lack of a good simulation model for the phase-locked loop was a real handicap. The original tests for the phase-locked loop were debugged on the tester. When trying out new tests, we had no way of simulating them to verify their correctness. Thus, it took two or three iterations before the tests were correct.

New Design Approach

Other ASICs being designed by our design center required phase-locked loops with similar characteristics. These ASICs were designed in a different manufacturing process. Therefore, the phase-locked loop had to be redesigned so that it would be leveragable to many different chips. As a result, it was decided to break up the design into two parts (Fig. 2). The digital logic would be designed using a VHDL synthesis strategy. Behavioral VHDL code would be written and then synthesized into our standard cell library. The code would be written so that it was easy to customize for new projects. Once the synthesis was complete, the netlist for the digital block would be routed and then integrated into the top level of the phase-locked loop. The analog portions of the phase-locked loop would be designed using a full-custom methodology. We would leverage the analog blocks from the previous phase-locked loop, but they might have to be modified and resimulated. Every new phase-locked loop design would undergo a final stability analysis.

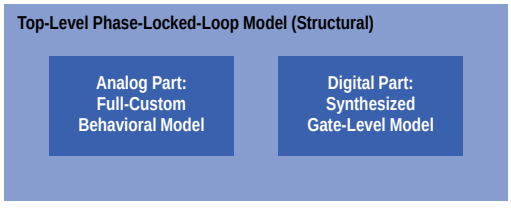

Fig. 2. *Structure of the phase-locked loop model.*

Model Structure

In the current design flow, the customer designs the chip by writing behavioral code in VHDL, synthesizing the design, and running final simulations in Verilog. To have a phase-locked loop model available for system simulations, we needed both a VHDL model and a Verilog model. The structure of the model is the same for both VHDL and Verilog. In the top level of the model are a digital part and an analog part. The model used for the digital part is simply the gate-level netlist for the digital block. Delays were calculated from the routing capacitance and were back-annotated using Standard Delay Format (SDF). The model for the analog part was written separately in VHDL and Verilog. These models were written at the behavioral level.

The logic for the digital section of the new phase-locked loop was highly leveraged from the old design. In most cases, the original phase-locked loop schematics were used as a guide, and the VHDL models for all the blocks inside the digital section were written so that the synthesis tool would produce equivalent logic. Constants were used in the code so that the design could be easily adapted. This made it much easier to change the design when specifications changed.

The analog section of the phase-locked loop was modeled in two parts. The first part modeled was the phase-frequency detector. The phase-frequency detector puts out a pulse on either its UP or DOWN output whose width equals the distance between the rising edges of the divider outputs FREF and FBAK. The state table for the phase-frequency detector is shown in Fig. 3. This was a fairly straightforward model to write, since the inputs and outputs were digital signals.

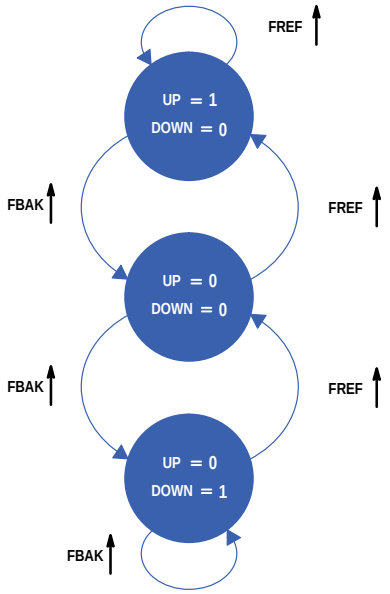

Fig. 3. *State table for the phase-frequency detector.*

Model for the Charge Pump and VCO

Finally, a model needed to be written for the charge pump, filter, and VCO. A simplified model of the charge pump and filter is shown in Fig. 4. A positive pulse on the UP signal will cause the voltage on VCNTL to rise, and a positive pulse on the DOWN signal will cause VCNTL to fall. The filter is added to ensure the stability of the loop.

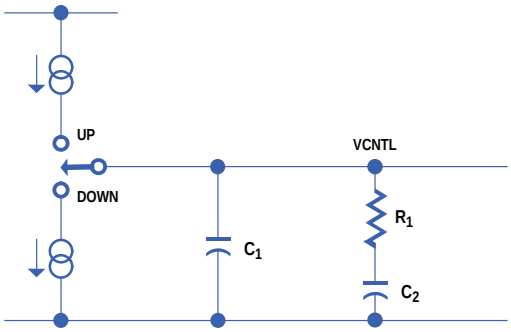

Fig. 4. *Simplified charge pump and filter model.*

A model was needed that would not slow down the simulation too much, and that could be written easily in both Verilog and VHDL. One problem with Verilog is that there is no easy way to define analog signals (although they could be represented with arrays or integers).

This problem was solved by using a variable of type time to represent the period of the VCO output clock. As pulses on the UP and DOWN signals arrive at the charge pump model, the length of the period is adjusted accordingly. The model calculates the width of the pulse on the UP or DOWN signal and divides by the maximum period count to determine the amount of correction to the period.

The model operates much differently than the analog circuit. The operation of the analog circuit is shown in Fig. 5. When the UP signal is high, the charge pump charges C_1 and the voltage VCNTL rises. When UP is low, charge shifts from C_1 to C_2 through the resistor and VCNTL falls.

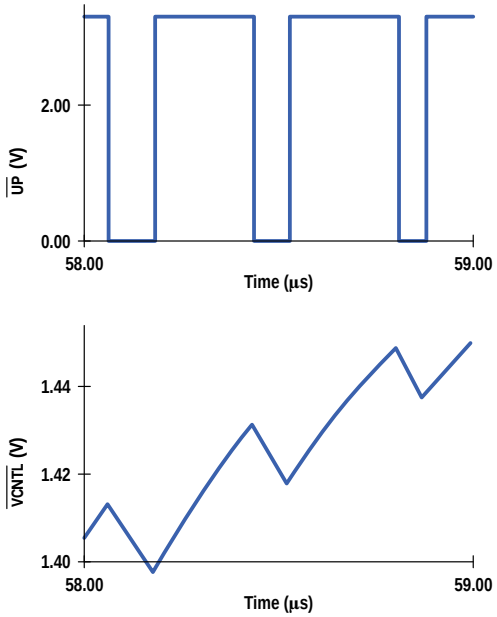

Fig. 5. *Operation of the charge pump.*

In the simulation model of the charge pump and VCO, the model calculates the width of the pulse on the falling edge of the UP signal. It then applies the correction to the period of the VCO. Some time later it will reduce the correction by half. This roughly approximates the rise and fall of the VCNTL voltage in the real circuit. The operation of the model is shown in Fig. 6.

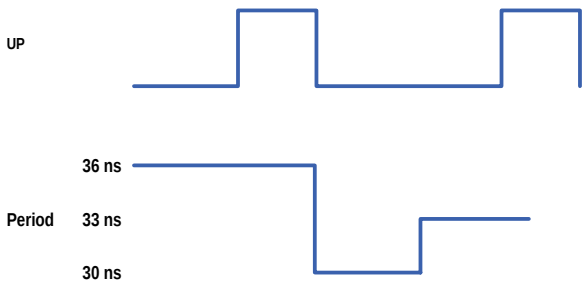

Fig. 6. *Operation of the charge pump model.*

In practice, this model works very well. The model locks to the proper frequency, and if modulation is used, the phase-locked loop will modulate between the proper two frequencies. However, the transition from one frequency to another will be much different from the actual phase-locked loop. Typically, the model locks much faster than the actual circuit.

Process for Developing New Phase-Locked Loop Designs

The intent from the beginning was to create a design that was easy to modify and adapt. Each ASIC has its own requirements for the input and output frequencies. Here is the procedure for developing a new customized version of the phase-locked loop.

1. Copy the VHDL code for the digital block and make changes to customize the code. Usually this involves changing constants in the code for the M counts, the N counts, and the modulation counts.

2. Simulate the entire phase-locked loop in VHDL to make sure that the operation of the digital block is correct.
3. Synthesize the digital logic using Synopsys.
4. Have the resulting netlist placed and routed in a block. We use Cadence's Cell3 to do placement and routing.
5. Calculate circuit delays from the routing capacitance. Calculate RC delays.
6. Do a timing analysis for the digital logic using the calculated delays.
7. Do a logic simulation using the real delays.
8. Make modifications to the phase-locked loop production tests.
9. If necessary, adjust the artwork for the analog blocks according to the specifications for the new phase-locked loop (for example, to adjust the frequency range of the VCO).
10. Redo the stability analysis for the phase-locked loop.
11. Place the routed digital block into the artwork for the top-level phase-locked loop.

Modifications to the digital section of the phase-locked loop can be done in about a week. This was very helpful for some ASIC designs because the system requirements for the phase-locked loop were changed several times. Changes to the analog section usually take much longer.

Problems with the Model

The availability of the complete model for the phase-locked loop was a great advantage. It enabled us to debug production tests for the loop before the chip was released. In addition, it allowed the customer to do system-level simulations that included the full modulating capability of the phase-locked loop. Our customers have used this capability to catch problems in the clocking and to debug corner-case problems. However, there were some minor problems with the model.

The first problem is that the model of the charge pump and VCO is very sensitive to the simulation resolution. The model was developed and runs fairly well with a resolution of 10.0 ps. It does not work very well when simulations are run with 1-ns resolution. This is because the model needs the extra resolution when adjusting the VCO clock period.

The second problem is that it is difficult to initialize the model. Because there is a feedback loop in the model, unknown values present at the beginning of the simulation propagate around the loop. To get the phase-locked loop to initialize, it is necessary to put the loop into its digital test mode or to force the counter reset signal in the phase-locked loop to 0 and then release it. Most people prefer the latter option because it requires less effort and doesn't require changing the system tests.

Once the model is initialized and running, it is still susceptible to unknown values being introduced. Since the phase-locked loop contains two asynchronous clock domains (the input clock and the VCO output clock), occasionally there will be a setup or hold violation on a synchronizer flip-flop. As a result, the output of that flip-flop becomes unknown, and this unknown value propagates around the loop. This problem could be averted if there were a synchronizer flip-flop model that did not go to an unknown state on a setup or hold violation.

Testing and Test Development

Our experience with phase-locked loop designs has showed us the need for more complete testing of the loop. Originally, three main tests were created for the production test of the loop:

- An analog test ran the phase-locked loop in all functional modes, allowed the loop to lock, and then made match assertions for 0 and 1. This test only tested that the phase-locked loop was producing a clock waveform. It did not test the frequency or duty cycle of the loop output.
- A digital test tested the functionality of the digital block through four ad-hoc test points inserted in strategic locations.
- A VCO linearity test applied three different clock frequencies to the clock input of the phase-locked loop. The loop was allowed to lock, and then the control voltage to the VCO was measured with the precision measuring unit of the tester. The test program then checked that the control voltage was higher for higher frequencies. This test was dropped from the production test because of concerns that the large capacitance of the precision measuring unit was altering the voltage measurement when it was connected.

These three tests did not fully cover the phase-locked loop. The digital logic was covered pretty well, and the basic functionality of the analog part was tested, but the production test did not catch any parameter variations that would cause the phase-locked loop to fail to lock. To address this concern, four additional tests were developed for later phase-locked loop designs, and three of these tests have been incorporated into the final production test.

Lock Test. A test was needed that would give some indication that the phase-locked loop was able to lock. To accomplish this, a new test was created. This test checks an internal signal in the phase-locked loop that indicates that the loop is close to being locked. This signal is one of the four test points that appear in the phase-locked loop design. To run this test, the loop is placed in one of its fixed frequency modes and allowed to lock. The internal lock signal is then checked to be sure that the loop has locked.

Clock 1× Test. Other ways of testing that the phase-locked loop was able to lock were also investigated. One test involved setting the loop into a frequency mode in which its output frequency was equal to the input frequency (or some even multiple). Then the loop was allowed to lock. After the loop had locked, the output divider was reset to make the phase predictable, and the clock output was strobed during the clock low time for 100 cycles. Then the output was strobed during the clock high time for 100 cycles. The idea was that if the phase-locked loop was not at the correct frequency, the phase would drift and there would be strobe failures. This test did not work very well in practice. When the loop was put into a chip and simulated, the difference between fast and slow delays made it impossible to find a good time to strobe the output clock. As a result, this test had to be dropped from the production test.

Leakage Test. In one ASIC, the phase-locked loop circuit was suspected of causing an excessive production line failure rate. After some investigation, the filter of the phase-locked loop was identified as the cause of these failures. Manufacturing defects in the large resistors and capacitors caused excessive leakage, changing the characteristics of the filter and preventing proper operation of the phase-locked loop. To screen out these defects, a new test was developed to check the filter for excessive leakage. In this test, the filter's analog signal is multiplexed out to a dedicated test pin and the charge pump circuit is turned off by means of a control bit. A voltage of 3.3 volts is applied to the pin and a current measurement is done with the tester's precision measuring unit. Parts with excessive leakage current are discarded. The implementation of this and other phase-locked loop tests has resulted in a 98% reduction in the line failure rate due to the phase-locked loop.

Charge Pump Tests. Another circuit not adequately tested in the original phase-locked loop was the charge pump. To remedy this a new test was developed to ensure that the charge pump was able to source and sink current within its design specifications. To allow for this test, new circuitry was added to disable either the M or N counter in the digital test mode. In the test, the chip is put into the digital test mode with the N counter disabled. A clock is applied to the M counter and the M counter is allowed to count until three pulses have occurred on its output. At this point, the UP signal will be high and the DOWN signal will be low. The clock is stopped at this point, a voltage of 1.3V is applied to an analog test pin at the output of the loop filter, and the current sourced by the charge pump is measured and checked against the expected current. The same test is repeated, this time disabling the M counter and allowing the N counter to count until three pulses have occurred on its output. At this point, the DOWN signal is high and the UP signal is low. A voltage of 1.3V is applied to the analog test point and the current drawn by the charge pump is measured.

Summary

We have greatly streamlined the procedure for designing, integrating, and testing a new phase-locked loop. In many cases, changes to the phase-locked loop can be made by resynthesizing and rerouting the digital block and then performing a stability analysis. The customer has access to a detailed model of the phase-locked loop in either VHDL or Verilog, and can use this to test the proper connection of the phase-locked loop and the surrounding system. Production tests can be debugged with simulation before they are put onto a tester. Finally, standard phase-locked loop tests have been written that run on our digital IC tester. These tests increase the test coverage for the phase-locked loop, increasing the quality of products shipped with these phase-locked loops in them.

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