Design Methodologies and Circuit Design Trade-Offs for the HP PA 8000 Processor

This paper discusses the various design methods used in the PA 8000, specific design techniques for the new packaging technology, the clock distribution scheme, cross-chip signal integrity issues, and some of the new tools and techniques.

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The increasing demands for greater processor performance to remain competitive in today's computer market necessitate careful attention to the methods used in designing processors to achieve these performance goals. Processor designs are increasing in complexity to meet performance goals, with such features as out-of-order execution and superscalar operation. Design cycles are decreasing in length, so design quality must increase as well. All of these factors call for new design techniques to ensure continued success.

This paper will present some of the design methodologies and choices used in the design of the HP PA 8000 CPU, the first HP processor to implement the PA-RISC 2.0 architecture and the first capable of 64-bit operation. The various design methods used in the PA 8000, specific design techniques for the new packaging technology used, the clock distribution scheme, and cross-chip signal integrity issues will be discussed. We will also present some of the new tools and techniques employed by HP to ensure a high level of quality on first silicon, based in large part on our experiences with previous PA-RISC microprocessor designs.

Design Trade-Offs and Methodologies

Processor design is a continuous series of trade-offs between die area, complexity, performance, speed, power use, and design time. Given the complexity of a four-way out-of-order processor such as the PA 8000, it is not appropriate to employ the same circuit design techniques for all blocks on the chip. For the PA 8000, three major circuit design techniques were used.

The first is the traditional *static design* approach, in which all output signals are held true as long as the inputs to the static cell remain constant. Storage of values, or *state*, is in latches, and logic functions are implemented using a variety of different logic blocks, allowing minimization of area or path evaluation time. Since static logic is fairly immune to noise effects (at least on a local basis), this is the safest design approach. Frequently this is also the design approach that needs the fewest engineering resources. The synthesis and layout steps can be accomplished by automated tools, with oversight by the designer to ensure that the block satisfies requirements, timing paths are met, electrical rules (such as metal electromigration) aren't violated, and so on.

Static design techniques are not ideally suited for large fan-in and fanout functions. Because of their pullup/pulldown design, static gates are not the fastest evaluation method for certain high fan-in/fanout applications. *Single-rail dynamic logic* or *domino logic* is better suited to these applications, particularly OR functions. A good example of such a function is the operand dump lines from register files. For an out-of-order processor with operand data coming from both rename and architected state registers, the number of drivers on one bus is quite large. In the case of the PA 8000 there are 56 rename registers and 32 architected state registers on both the integer and floating-point sides. Trying to drive a single bus with 88 static drivers is a much more difficult task than using single-rail dynamic logic. The lower capacitance of simply using an n-channel FET driver and a bus precharger for the nondump state helps tremendously in this instance. Static logic will also consume more area to implement these types of functions because it requires extra p-channel FET pullup trees in each block. However, dynamic logic is more susceptible to noise, requires more careful design attention than static logic, will in general use more power, and since it is a clocked mechanism, also increases the clock load. This type of logic is employed in the data path portions of the PA 8000.

Single-rail dynamic logic does fail in some instances, particularly when trying to use the inversion of a value in the middle of a logic chain, or using an AND function. In this instance and where static logic is not fast enough, a *dual-rail dynamic logic* scheme can be employed. In this type of logic, both the positive sense and the negative sense of a signal are derived, both in a low-go-high fashion.* Inversions are accomplished simply by switching the low-sense and high-sense signals between gates. This logic can be quite fast since the design of the gates optimizes one transition edge and dynamic techniques are employed in the pulldown trees of the logic gates. In addition, since timing information is included with the transition of one or the other output sense, it is a self-timed mechanism. By employing latches that sense just the first transition of an output

* Low-go-high means that the signal starts at the ground voltage and transitions only once during an evaluate state to the supply voltage V_{DD}.

pair, this type of logic can be pipelined and used in multiple stages. Dual-rail dynamic logic does consume a large amount of area and power, and therefore was employed only in the most time-critical portions of the PA 8000, most notably the floating-point execution units.

Alpha Particle Sensitivity

The decision to use lead solder bump technology to enable flip-chip die attach for the PA 8000 presented a new design challenge for the team. Previous designs were all wire-bonded dice in ceramic pin-grid array packages (CPGA). To prevent alpha particles (which are identical to helium nuclei) emanating from the package or wire bonds from upsetting sensitive storage nodes within the processor, a silicon compound is used on the die surface. The flip-chip attach method, however, places arrays of mostly lead (Pb) hemispherical bumps over a significant portion of the die surface. The bump material contains some heavy elements that are radioactive and the decay of these elements produces alpha particles and beta and gamma rays that can cause a *single-event upset* of a sensitive storage node.

The single-event upset is a high concern in integrated circuits because a change of state of a storage node can have serious consequences for executing programs. Any alpha particle that leaves the solder bump has sufficient mass and energy to cause an ionized trail of hole-electron pairs that create mobile charges that can flood a positively charged storage node and cause an unintended state change of a memory element. To minimize this undesired event, certain design changes were adopted for PA 8000 memory circuits.

A SPICE current pulse model that simulated the behavior of an alpha particle was derived from both empirical measurements on existing products and simulation using IC process modeling software. A design rule for the minimum storage charge ($Q_{critical}$) was set and all storage nodes were designed to meet the new guideline, then verified by SPICE simulations using the alpha particle current pulse model.

Clock Distribution Scheme

In a high-frequency design such as the PA 8000, minimizing cross-chip clock skew is critical to ensure the maximum amount of time for logic and data path operations to complete. Lack of attention to clock distribution for the entire chip will result in a lower frequency of operation and more design resources being spent on reducing delays in budgets that contain cross-chip paths. Excessive clock skew also increases the likelihood of introducing races into the design that will need to be identified and fixed. For these reasons a considerable amount of effort was spent in the investigation and design of the clock distribution scheme for the PA 8000.

Also affecting clock skew across the chip is the amount of load on the global clock signal. With single-rail and dual-rail dynamic circuitry in the data path sections, the overall clock load is greater than it would have been had only static circuitry been used. This places an additional burden on the clock distribution network because skew increases with load for a given clock network definition.

The clock distribution method employed on the PA 8000 is an H-tree metal structure (see Fig. 1) to deliver the clock signal from the C4 solder bumps to a first-level on-chip clock receiver. The output of this receiver is then routed using matched wire lengths to a second level of clock buffers, with each buffer carefully positioned on the chip and the output load of each buffer matched as closely as possible. Given the large size of the die for the PA 8000 (19.2 by 17.8 mm), process variation will inevitably make the FETs used in these second-level clock buffers unequal in strength. The design of these buffers attempted to minimize this speed variation. A graph of the overall skew using the final clock distribution scheme is shown in Fig. 2. Using this design, the overall clock skew across the die was held to 170 picoseconds.

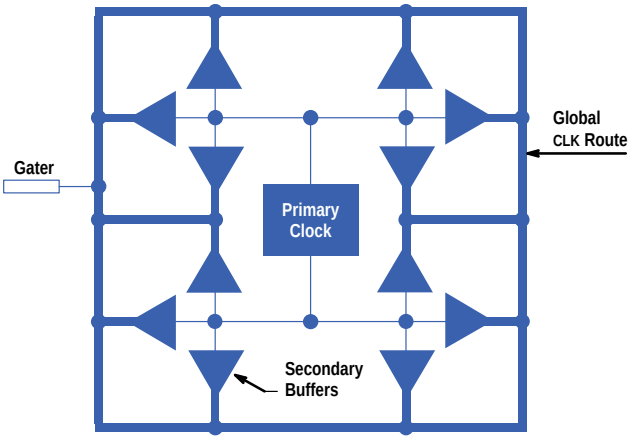

Fig. 1. *H-tree distribution network.*

From the second-level clock buffers, careful attention was paid to the routes of the buffered clock outputs to the next level of circuitry. To minimize the power dissipation of the chip and provide nonoverlapping clocks to control blocks, controlled

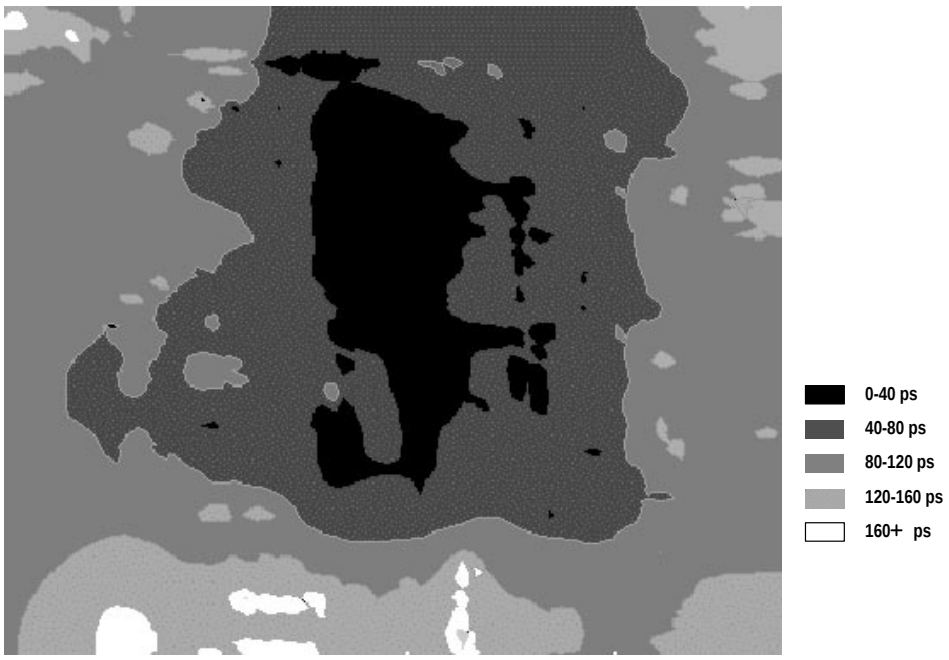

Fig. 2. *Clock skew topography map.*

buffer blocks called *clock gaters* are employed. Different types of clock gaters can generate overlapping and nonoverlapping clocks, and each size of gater is rated for a specific amount of output load. Checks were performed to ensure that the proper loading was maintained on all gater outputs, since the clock outputs for these gater blocks were guaranteed to a certain specification only under a rated load range. Whenever possible, the clock gaters were qualified with control signals to strobe their clock outputs only when necessary. This allows the clocks for various functional units to be clocked only when actual work needs to be done, reducing overall chip power dissipation.

Timing

To ensure high-frequency operation and a short post-tape-release period, vigorous timing checks were employed by PA 8000 block and top-level designers. The timing effort on the PA 8000 was far greater than on previous HP processors, and was a significant factor in producing first silicon that ran at the targeted design frequency from the first boot of the operating system.

The size of the die complicated top-level timing analysis because the sheer distance some signals had to travel added significant delay to cross-chip budgets. Over-the-block routing was necessary given the large number of top-level signals present on the chip. Noise and capacitance to metal layers inside of the blocks being routed over had to be factored into the top-level timing analysis.

Repeaters were employed on the PA 8000 for long-route, timing-critical signals to reduce the delay and allow for faster signal edges. In some cases this was accomplished with one noninverting buffer, and in other cases split inverters along the route were used. Where possible, single inverters were used in cross-chip paths if this level of inversion could be absorbed by the receiving or driving logic, thus speeding up these paths.

Block designers ran timing simulators, both path-driven and stimulus-driven, to check the internal timing of their blocks and to verify that their published drive and receive times for global signals were valid. Close to tape release, a large effort was put into driving down the number of slow cross-chip paths, which threatened the frequency goal of the PA 8000.

In addition to the timing checks performed on the PA 8000, other quality checks were performed to detect potential problems discovered on previous processors. The checks will be described in the remainder of this article. Most of these problems are related to noise events on signals and supplies that trip sensitive circuitry, causing failures.

Latch Margin Checks

Latches are an important part of any processor design. A large amount of state information about a currently running program needs to be stored. Control logic and data paths both employ latches to a large degree. Latch designs trade off setup, hold, and in-to-out delay times by optimizing the size of various FETs in the latch structure, particularly the feedback inverter, which holds the state of the latch and must be overcome to change the state. The PA 8000 design employs transparent latches in which the input signal passes through a series n-channel FET and thus suffers a gate threshold voltage drop as well.

Since changing the state of a latch inadvertently is potentially disastrous, avoiding poor latch designs was a critical design goal. For this reason, a specific tool was developed to analyze the electrical margins of a latch and was run on all the latches on the PA 8000. The complexity of this tool grew from a desire to be able to check both full and half latches. A full latch consists of two cross-coupled inverters while a half latch has a single FET connected to the inverter output (see Fig. 3).

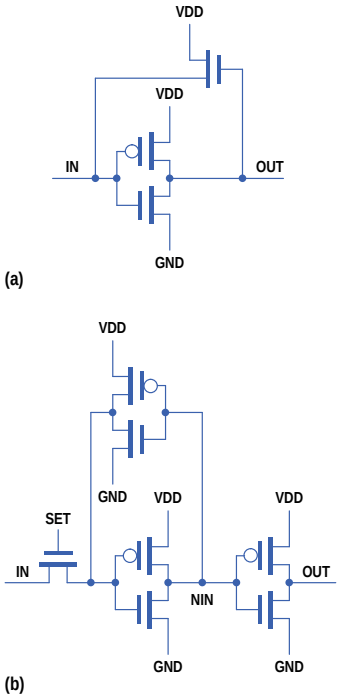

Fig. 3. *Two types of latches. (a) Half latch. (b) Full latch.*

The latch check program evaluated the set drive path to determine if it was strong enough to overcome the feedback FETs. Since the input drive signal must be known to accomplish this evaluation and extracting this drive signal from all of the places where latches are used is a rather complex task, the program had to make some assumptions about the driving block when run only on the latch cell. For critical paths or latches with particularly small margins, the actual driving path was placed into a small schematic and the program was run on this schematic to ensure that the latch was acceptable.

Signal Noise Checks

In implementing the PA 8000, additional levels of interconnect were required with finer geometries than had been used on past designs to connect the blocks on the chip together. This posed a number of problems in guaranteeing that the design would be electrically robust at the high frequencies at which the PA 8000 operates. Experience during electrical characterization of previous designs indicated that internal signal integrity would be a serious issue for the PA 8000.

Signal Integrity Issues in Advanced Processes

Three major problems arise with interconnect as processes continue their inexorable march toward smaller dimensions and higher frequencies:

- Signal cross talk is very significant at the 0.5-µm process generation and beyond.
- Signal rise and fall times decrease as transistor speed increases.
- Signal coupling increases because smaller dimensions are used for interconnect. The smaller dimensions especially increase coupling between metal lines on the same interconnect layer.

Signal cross talk (noise effects) includes both capacitive and inductive components. In the equations $i = C\,dv/dt$ and $v = L\,di/dt$, all of the factors—C, L, dv/dt, and di/dt—are increasing with decreasing interconnect dimensions and faster transistors. This leads to voltage and current disturbances in lines that couple to adjacent metal lines through mutual capacitive and inductive effects. An example of an interconnect and circuit topology that can cause these problems is shown in Fig. 4.

Very fast edge rates require high transient currents (tens of amperes) from the off-chip and on-chip power networks. High currents are also present in the main clock network on the chip. Power supply networks require careful design to minimize inductive and capacitive effects on voltage levels. Clock nets also need to maintain good voltage levels as well as minimize clock skew delays between various blocks.

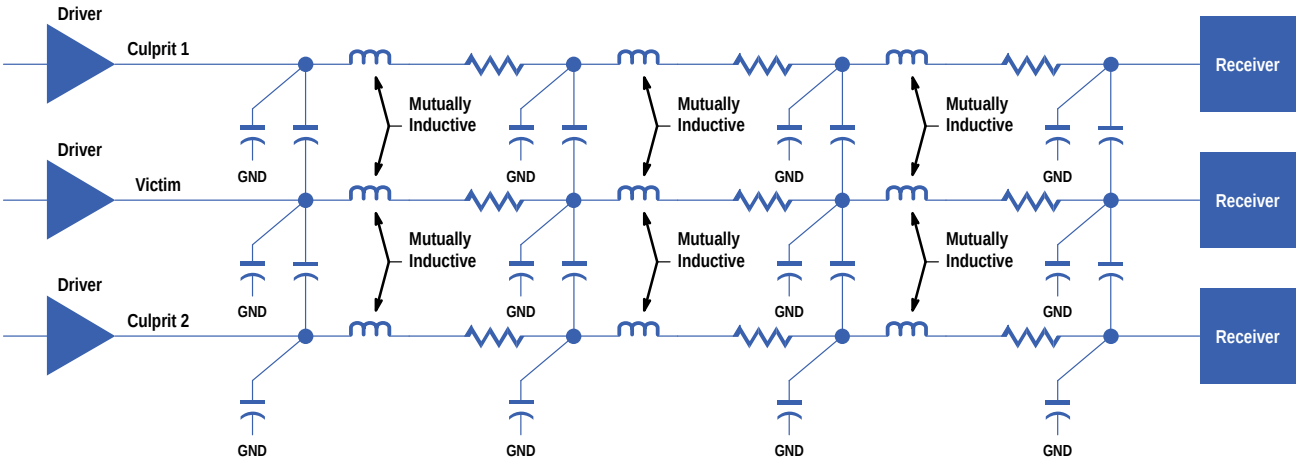

Fig. 4. *Interconnect topology causing crosstalk problems.*

Solving Signal Integrity Problems

Different approaches can be used to solve signal integrity problems. In general, combinations of the following techniques were used on the PA 8000:

- Adjust spacing of signals relative to each other
- Include shields above and below signals
- Include restoring logic (repeaters) in the route
- Design signal receivers that reject noise events.

A key component of the effort to correct signal integrity problems is a toolset that can be used to identify them in the first place. This toolset needs the ability to do RC extraction and the ability to identify circuit topologies that may be susceptible to noise problems. RC extraction allows determination of the extent of possible coupling problems. By combining it with identification of susceptible circuits, solutions to problems can be implemented.

To identify circuits with noise susceptibility, an existing internal tool was heavily modified and extended to allow easy traversal of the current schematic or artwork netlist hierarchy. This tool could display all connections of a given signal down to the transistor level, including information on FET sizes and estimates of capacitive loading (from schematics) or extracted capacitive load (from artwork). Information on port directionality and other text properties added by the block designer could also be displayed, as well as what terminals of a FET are connected to the signals. One additional important feature of the tool was that it could track any changes in real time, as soon as they were made by designers. This tool was used for many purposes by designers in addition to its use in noise checks.

The latching methodology used on the PA 8000 has a potential failure mode: excursions of a signal beyond a supply rail (e.g., below local ground for a given latch) could cause the latch to lose its value. An example of this is illustrated in Fig. 5. The latch shown is holding a high value—node IN1 is at V_{DD}, held by the weak feedback inverter. If the victim line is at 0V and

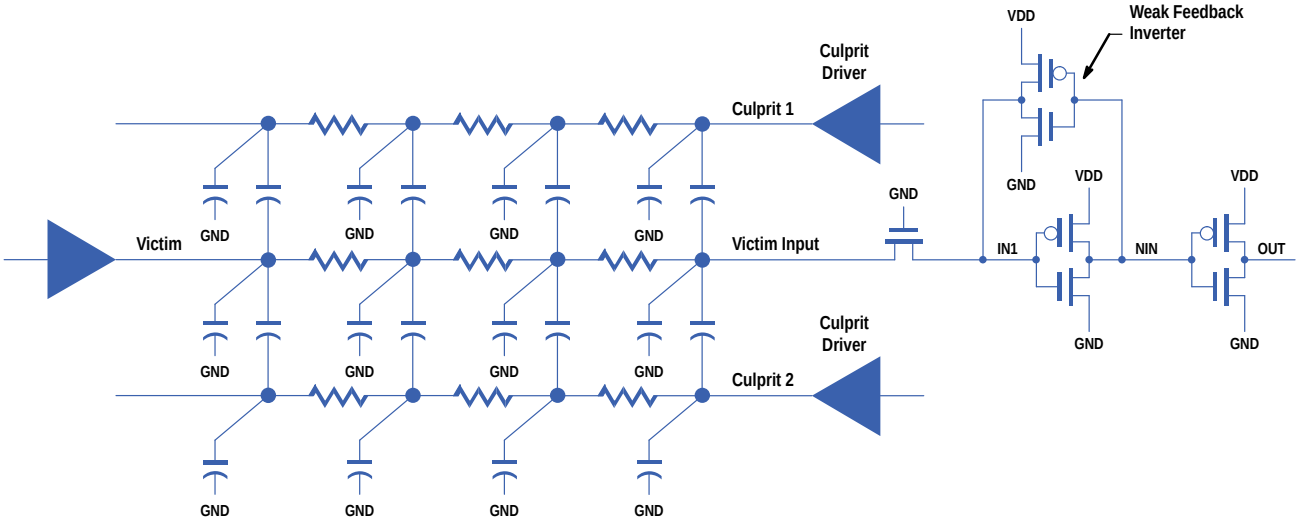

Fig. 5. *Latch failure caused by cross-chip noise.*

the culprit lines are at V_{DD} and transition to 0V quickly, an excursion of the input signal below local ground is possible, induced by capacitive coupling from the culprit lines to the victim line as the culprit lines transition from 1 to 0. This input signal excursion can cause the n-channel FET pass gate that serves as the input to the latch to turn on even though its gate is held at 0V (V_{GS} for the transistor is greater than V_{TN}). This is because the victim input is temporarily below local ground. With this n-channel FET pass gate on, the latch can spuriously dump the value it was holding by discharging the IN1 node if the transient is enough to overcome the feedback inverter and trip the forward inverter. This type of failure may change the state of the chip, and is a serious problem that must be avoided.

Other possible problem circuits were also identified by this tool, including heavily ratioed* combinations of p-channel FETs and n-channel FETs and long routes connected to gate inputs of pass FET latches. However, diffusion-connected inputs were the most common problems. To identify diffusion-connected inputs, the netlist traversal tool was run on every top-level signal in the design. The tool identified top-level signals connected to the source or drain of a pass FET in a latch. This gave a textual report of all connections down to the FET level for every top-level signal, in addition to the FET terminal connections and whether the signal was an input or output of that particular leaf cell.

Once the report was generated, a parser analyzed the connectivity to determine if any signal connected to a FET diffusion was also an input (outputs of leaf cells were ignored). Other checks were performed for additional suspect circuit topologies. When potential problem signals were identified, the information was integrated with RC extraction results to determine priorities for fixing signals, and the results were distributed to designers to give them feedback on which signals in their blocks needed to be fixed. Extensive simulations showed that only routes longer than a specified threshold length would need to be fixed. This threshold gave designers a limit at which they would have to do something to reduce susceptibility to noise on a signal being received by their block.

In most cases, designers used one of the techniques described above to alleviate these noise problems. The most popular solution inserted a restoring inverter in front of the pass gate and modified the latch slightly to make it logically equivalent to the latch that needed to be replaced, as shown in Fig. 6. The restoring inverter in front of the pass FET makes the latch far more immune to noise events on the input. At other times, repeaters (inverters and buffers) were inserted in routes to cut down the distance of the route, thus reducing the susceptibility of a given line to transitions by its neighbors.

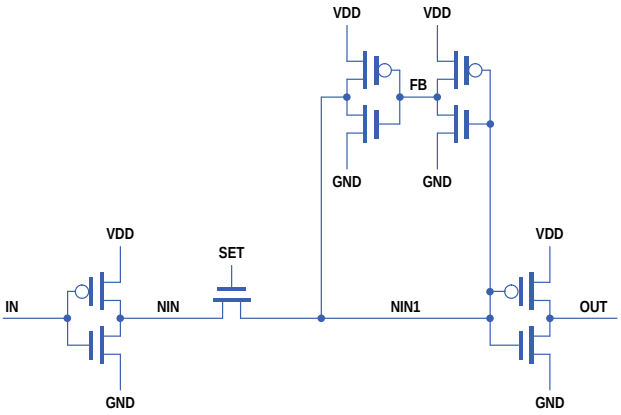

Fig. 6. *Input noise resistant full latch.*

Signal Integrity Results

Overall, the techniques described above were effective in eliminating noise-induced electrical failures in the PA 8000 design, and probably saved several months of characterization to investigate noise failures that would have existed had this tool not been developed. Over 7000 potential problems were flagged with the first run of the tool. All of these problems were investigated and either fixed or waivered before tape release. The PA 8000 was a very electrically robust design given its complexity level when silicon was received.

One drawback of this tool was that it was only run on top-level signals. Since some of the blocks on the PA 8000 were very large, long routes and therefore noise problems could also be embedded inside blocks. One such problem was found during characterization of the chip at the block level. We are currently extending the noise analysis tools to operate at deeper levels throughout the chip hierarchy to thoroughly check all signals on the chip. RC extraction is being extended to allow deeper levels of extraction without long run times, and inclusion of inductive effects is also being investigated.

A limitation of this type of tool is that it can generate a lot of noise, that is, report problems that really aren't problems. This affects designer productivity because the problems reported by the tool must be investigated. However, the penalty and cost for finding a noise problem in a design can be very high, especially late in the characterization process, so effort spent early

* Heavily ratioed combinations are combinations of inverters and other FETs in which the effective p-channel FET drive strength is significantly different from the effective n-channel FET drive strength.

to eliminate possible problems is very worthwhile. We are currently developing more advanced tools to eliminate some of this noise and make sure that only problems serious enough to warrant fixing are included.

Block Quality Checks

Block design, especially for complex blocks, is a time-consuming process in which—despite the best intentions of the designer—problems can sneak through without being noticed. For this reason several additional tools were developed to allow designers to check for potentially troublesome circuits in their blocks.

One tool checks for so-called "ugly" polysilicon structures. Given the resistance of the polysilicon layer in the HP process used to fabricate the PA 8000, long polysilicon routes are undesirable and can cause numerous problems, chief among these being slow speed. Standard cell routed blocks suffered less from this problem because the routers employed used only metal layers for signal interconnect. Long polysilicon problems occurred primarily in semicustom and full-custom designs. This tool flagged polysilicon routes between 25 and 50 micrometers long as warnings and over 50 micrometers as errors.

With the significant use of clock gaters to create many different flavors of clocks, both overlapping and nonoverlapping, races were expected to be more prevalent in the PA 8000 design. Pass-gate blocks in particular cause these types of problems. Clock-qualified signals (signals derived from clock edges) driving other clock-qualified nodes were checked to cover signal races not detectable by the previous race checking methodology used in PA-RISC processor designs.

Summary

All of the techniques described above helped to make the PA 8000 processor a successful project, achieving its frequency, performance, and aggressive post-tape-release schedule. This was a great achievement given the sheer complexity of the design, the fact that it was a new processor architecture, and the number of new technologies employed in the design. This success is due in large part to the design methodologies used for this processor, particularly the new methodologies developed for the PA 8000 design.

Acknowledgments

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