

HARD DISK MICRO DECISION

SERVICE GUIDE

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600 McCormick Street
San Leandro, California 94577

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MD-HD Service Guide

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HARD DISK MICRO DECISION SERVICE GUIDE

1. INTRODUCTION

This guide is intended to explain the disassembly, troubleshooting, repair and reassembly of the Morrow Hard Disk Micro Decisions, including the MD-5, MD-11, MD-16, and MD-34.

The manual guides you through the replacement of major assemblies: power supply, disk drives, and motherboard. If you attempt to perform repairs at the component level (other than ROM upgrades), you do so at your own risk, as this voids any remaining factory warranty.

Tools Required

The following equipment is recommended for troubleshooting and disassembly:

- o Known good terminal set up for 9600 baud
- o Hard Disk Supersoft Diagnostics Diskette & Manual
- o Phillips screwdriver
- o IC puller
- o Voltmeter
- o Needle-nose pliers
- o Hard Disk Micro Decision User's Guide

Important Precautions

Avoiding loss of data - If the owner has not backed up the hard disk onto floppies, doing so should always be the first step in servicing the computer. The Diagnostics Diskette has options for running the Fullback program or PIP.

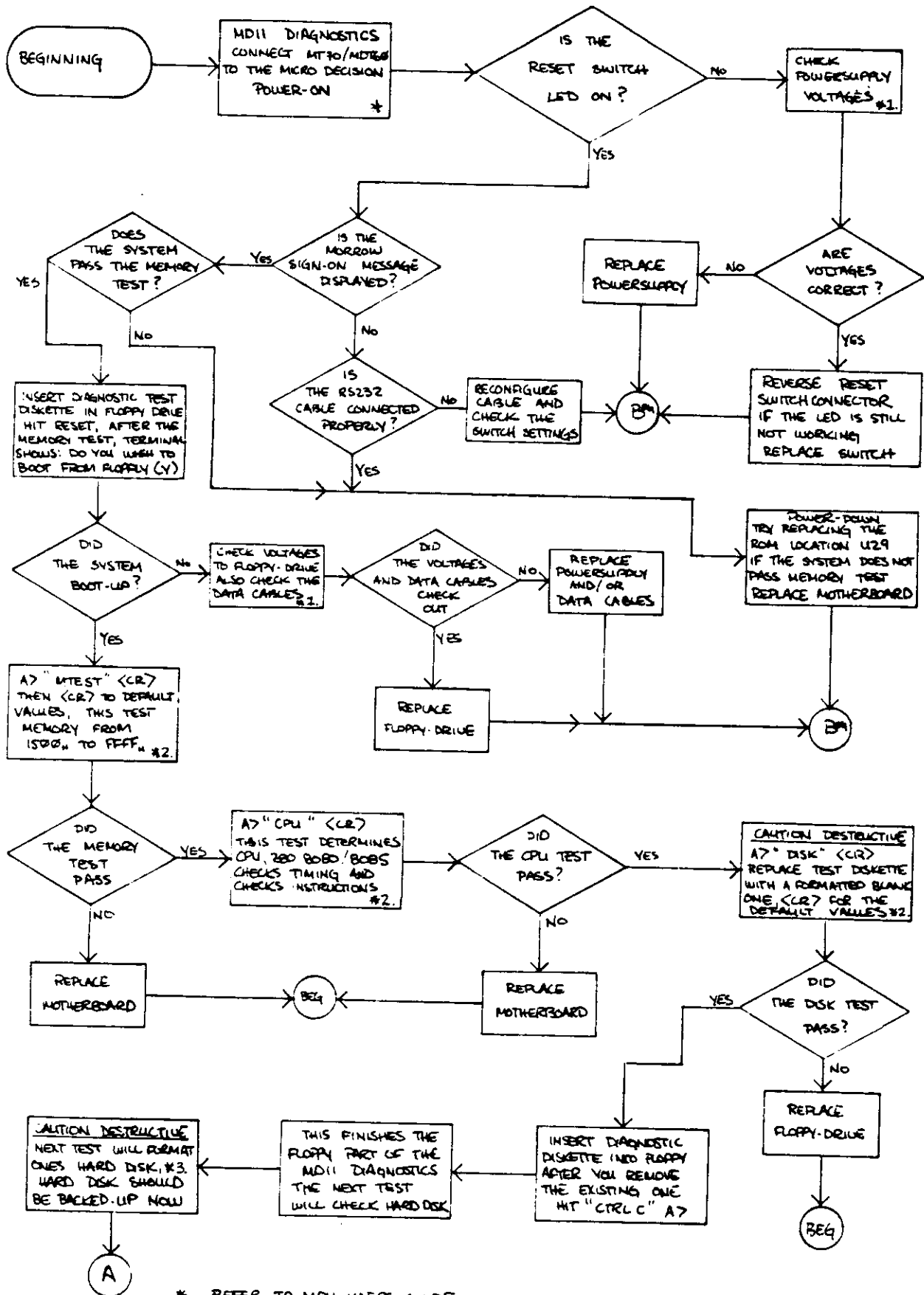
In situations where it is impossible to back up the disk, you will have to rely on the owner's backups.

Electrostatic discharge - When working with the motherboard, you should wear a grounded wriststrap. At a minimum, spray carpets in the area with a diluted mixture of liquid fabric softener.

Parking the hard disk - Always park the hard disk after applying power to the computer, unless a defect makes doing so impossible. PARK.COM is present on all standard Morrow hard disks and on the Diagnostic disk.

2. TROUBLESHOOTING

Follow the steps on the next three pages for isolating a defective subassembly. Replacement procedures are in later sections. Appendix A describes error codes.

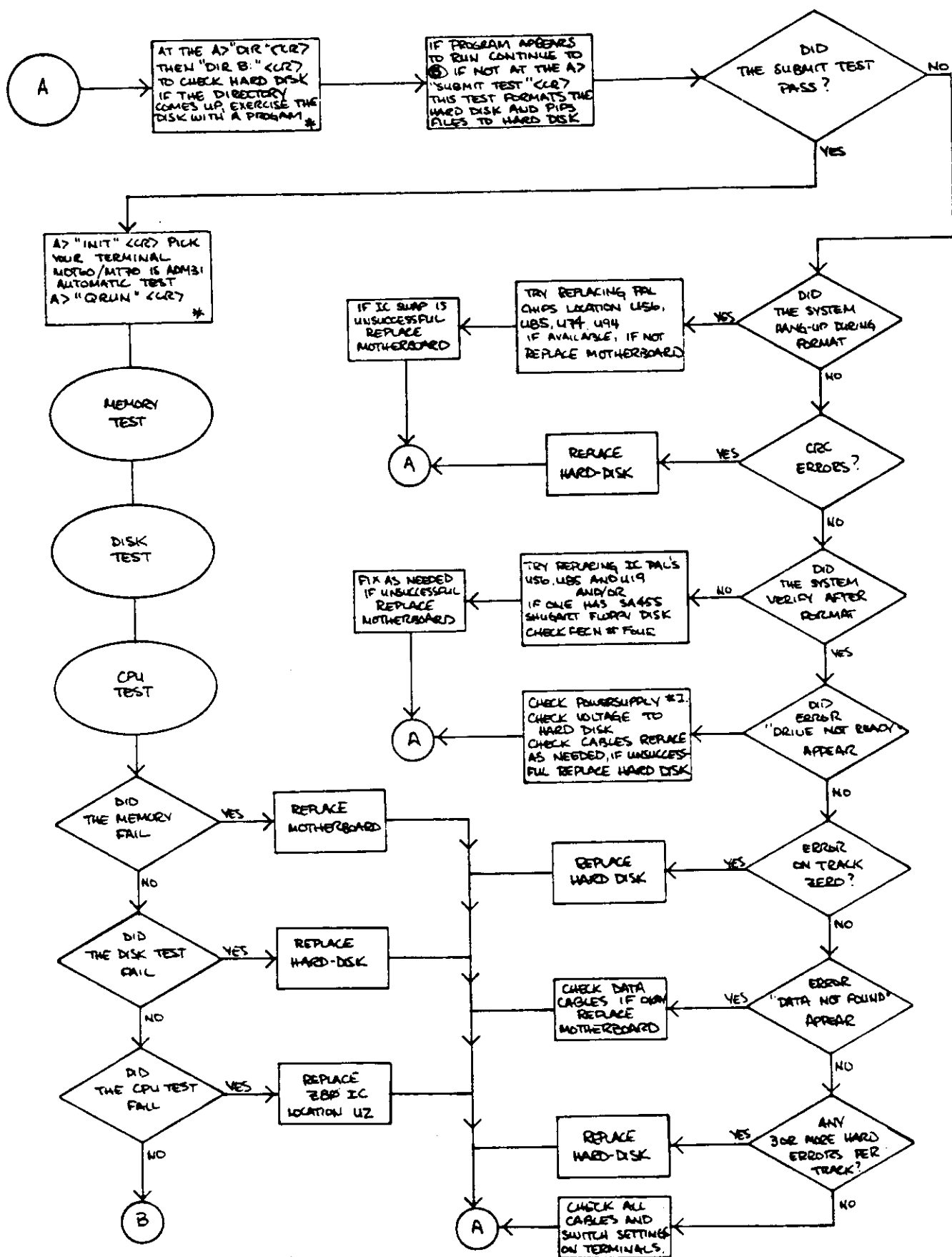


* REFER TO MDI USERS GUIDE

*1. REFER TO PAGE 5-1 SERVICE GUIDE

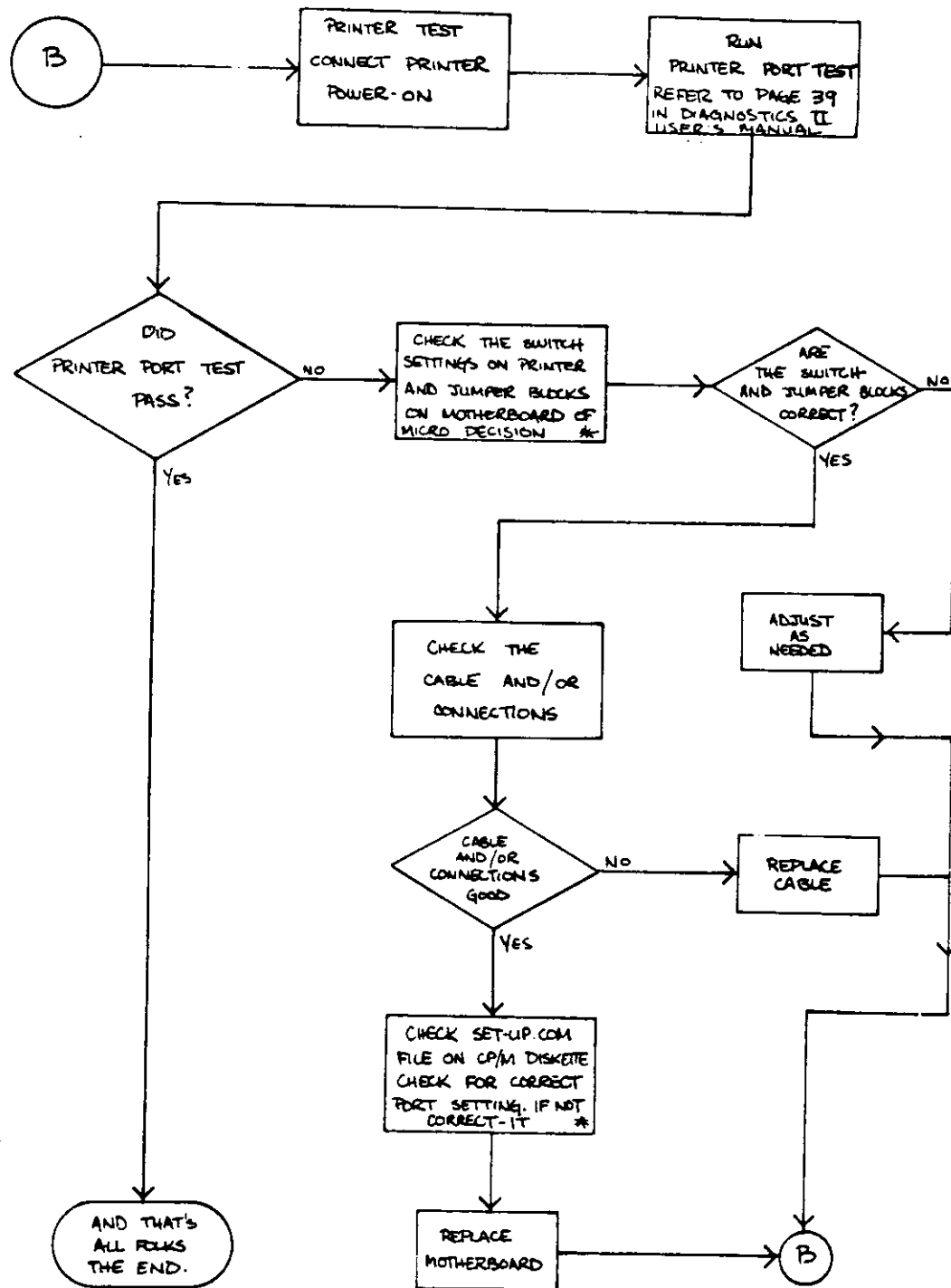
*2. A> "FILENAME": MEANS TYPE THAT FILENAME

*3. CUSTOMER IS RESPONSIBLE FOR BACKING-UP HARD DISK



* A>"FILENAME": MEANS TYPE THAT FILENAME

*1 REFER TO PAGE S-1 SERVICE GUIDE



* REFER TO MD11 USERS GUIDE

3. DIAGNOSTICS

The Service Aids Kit includes a Diagnostics Disk for the Hard Disk series of Micro Decisions. Its tests are documented in the Supersoft Diagnostics II manual, which is the same manual used for the MD-1/2/3 series of Micro Decisions.

The Micro Decision also contains diagnostic routines in its BIOS ROM. To access them, locate the unnumbered diagnostics jumper near the center of the motherboard (see Figure B-1). Short it with a jumper block and turn on the computer. If the power-on memory test passes, the following appears:

- | | | |
|------------------------|---|--------------------------|
| 1. PORT 1 | \ | |
| 2. PORT 2 | > | BARBER POLE TEST PATTERN |
| 3. CENTRONICS PORT | / | |
| 4. LOOP BACK ON PORT 2 | | |
| 5. RAM TEST | | |
| 6. FDC R/W | | |
| 7. FDC SEEKTEST | | |
| 8. VFO TEST | | |
| 9. BOOT | | |

Enter #:

Some of these duplicate the functions of the disk-based Supersoft Diagnostics, but they have the advantage of being available even when you have floppy drive problems.

Description of tests:

NOTE: To stop any test, press any key and wait for the Diagnostics Menu to reappear. Exit by booting (option 9).

PORT 1 test - sends a barber pole pattern to the terminal.

PORT 2 test - sends a barber pole pattern to the PRINTER/MODEM port.

CENTRONICS PORT test - sends barber pole pattern to CENTRONICS port.

LOOP BACK ON PORT 2 test - tests the PRINTER/MODEM port's Z80 DART. You must use a dummy connector with pin 2 jumpered to 3 and 5 to 20.

RAM test - continuously tests all of RAM reporting defective address and bit number.

FDC (Floppy Disk Controller) and VFO (Variable Frequency Oscillator) tests - not implemented at this time.

BOOT - proceeds to boot from the disk in the normal fashion.

4. COVER REMOVAL

Before removing the cover, be sure to:

1. PARK the hard disk if possible.
2. Turn off power to the computer and any connected peripherals.
3. Disconnect any cables from the rear panel.
4. Unplug the computer from the AC power source.

To remove the cover:

1. Tip the front of the unit up, so that you have access to the base of the chassis.
2. Using a Phillips-type screwdriver, remove the four screws closest to the outside edges. There are two on either side.
3. Set the unit back on its feet, and slide the cover forward (toward the drives) until it is completely off the chassis.

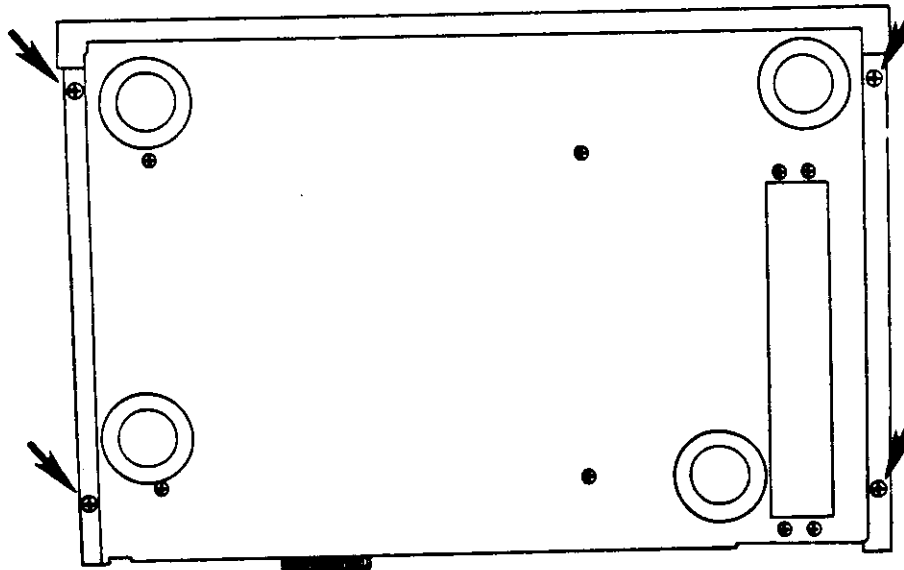


Figure 4-1: Cover Removal, Location of Screws

To replace the cover, reverse the procedure above.

5. POWER SUPPLY

Power Supply Voltages

The hard disk Micro Decisions employ an 80 watt switching power supply that must be connected to a proper load before voltages can be checked. If there is a short in the system, or the supply is unloaded, it shuts down automatically.

If the fuse inside the supply is blown, this generally indicates problems with the supply itself.

Most supplies have an unused wiring harness attached to the top. Voltages can be checked at that connector. They should be as follows, within 10% :

Unused wiring harness

Black	Ground
Red	+5
Blue	-12
Pink	+12

In units without the extra harness, +5 and +12 can be checked at the disk drives:

Disk drive harness

Black	Ground
Red	+5
Blue	+12

Removal

1. Tip the front of the unit up, so that you have access to the base of the chassis.
2. Locate and remove the four mounting screws on either side of the power supply's ventilation grill (see Figure 5-1).
3. Set the unit back on its feet. Lift the power supply out, and set it aside. The power connector should still be connected.

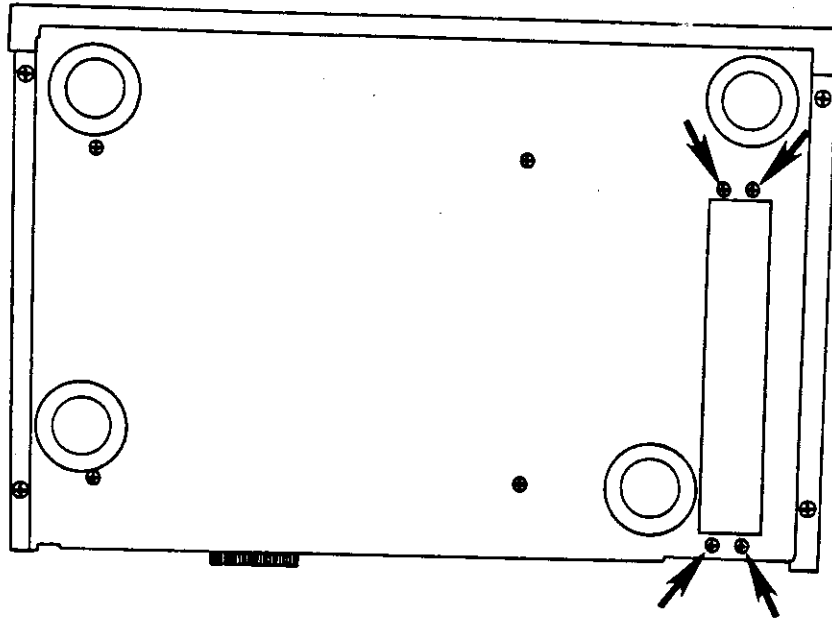


Figure 5-1: Power Supply Removal (Location of Screws)

Replacement

To replace the power supply, set it in the proper place and use the four mounting screws to secure it to the base of the chassis.

6. DISK DRIVES

Removal

Before removing the hard disk drive, be sure all data has been backed up on floppy diskettes! Also note that the power supply must be removed before the hard disk drive can be removed (see previous section).

1. Remove the two side mounting screws from the hard disk. These screws are on the same side as the power supply. (See Figure 6-1).

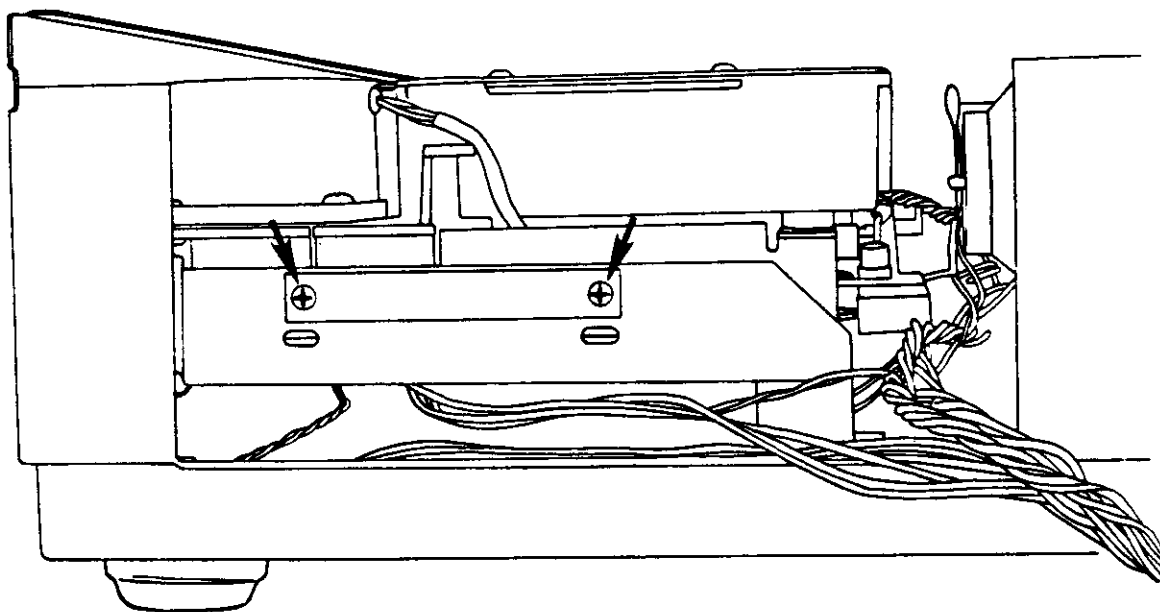


Figure 6-1: Side Mounting Screws, Hard Disk Drive

2. Remove the two mounting screws between the hard disk and the floppy disk drive (see Figure 6-2).
3. Remove the two side mounting screws from the floppy disk drive (see Figure 6-3). These screws are located on the left side of the drive, as you face the front of the unit.
4. Remove both drives and set them aside **carefully!**

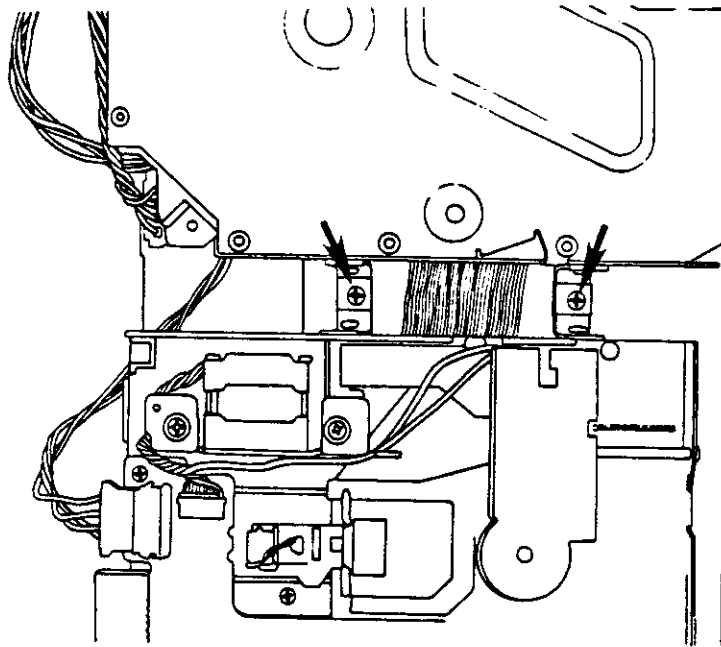


Figure 6-2: Disk Drive Removal

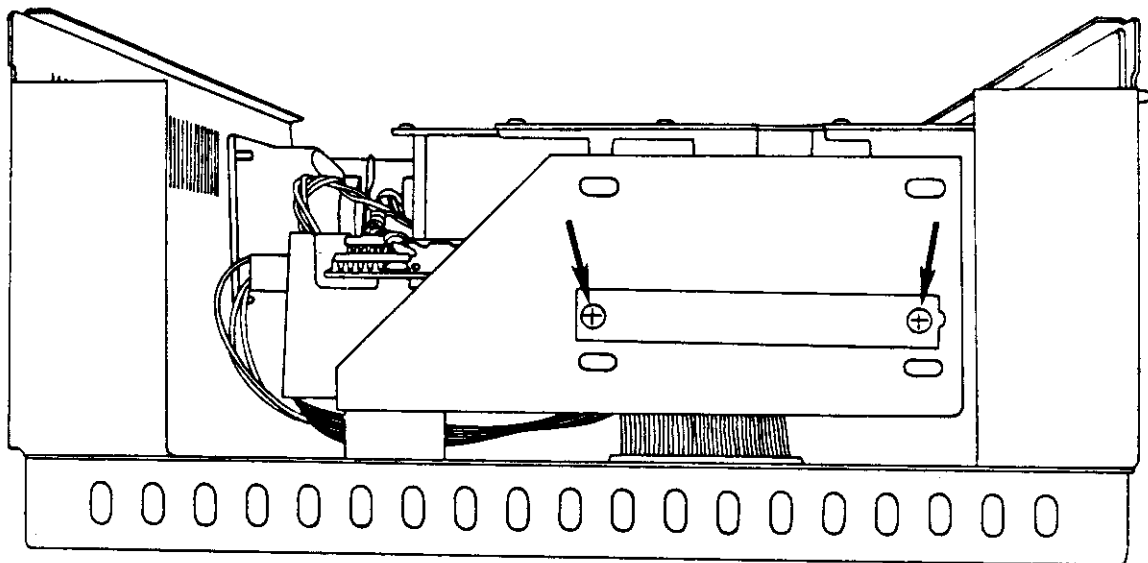


Figure 6-3: Floppy Disk Drive Removal

Replacement

1. Install the floppy drive first by replacing its two side mounting screws.
2. Install the hard disk, first putting in the middle mounting screws, then the hard disk drive side mounting screws.

7. MOTHERBOARD

Removal

CAUTION:

To avoid electrostatic discharge, which can cause serious damage to the motherboard, moisten the carpet with a spray bottle of water and touch the chassis frequently as you work. Handle the motherboard by the edges, and avoid touching IC leads and/or solder connections.

1. Remove the disk drives as explained in Section 6.
2. Turn the unit upside down and remove the four screws on the bottom of the chassis (see Figure 7-1).

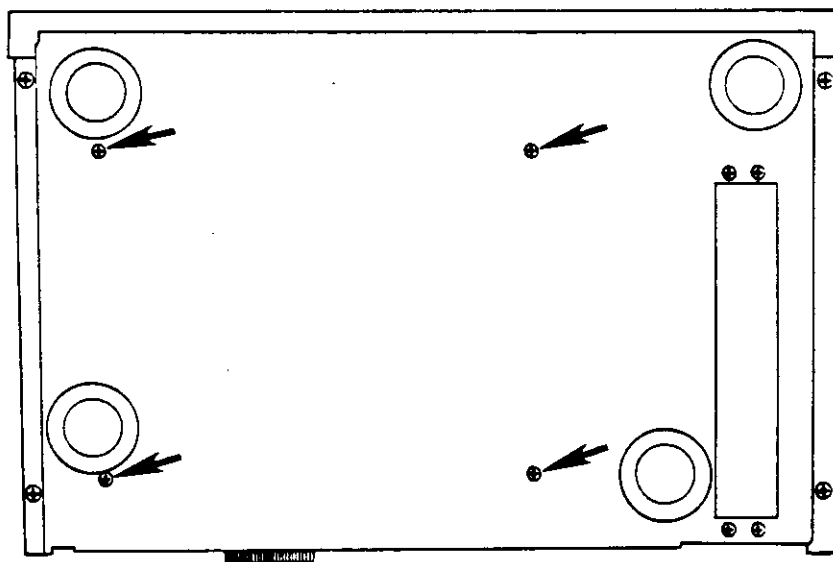


Figure 7-1: Motherboard Screw Locations (Chassis Base)

3. Remove the two screws on the rear panel that hold the motherboard and rear panel cut-out plate (Figure 7-2). To prevent the board from falling, gently support it with your hand when removing the last screw. Set the screws and plate aside.

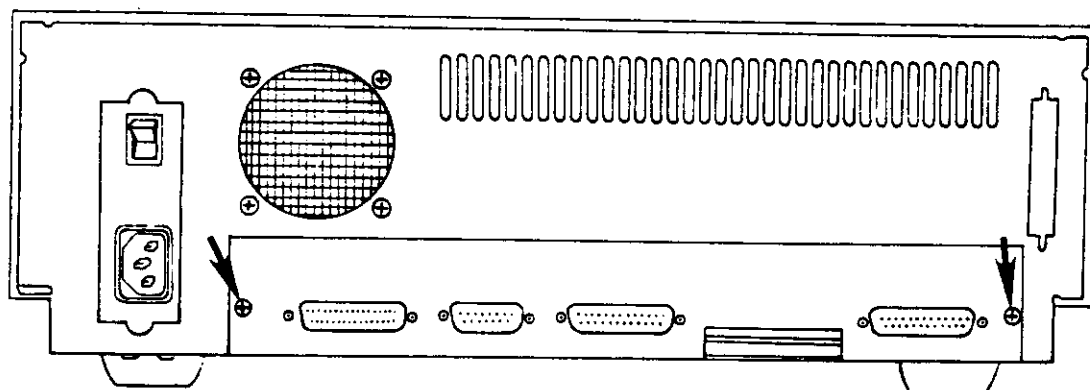


Figure 7-2: Motherboard Screw Locations (Rear Panel)

4. Disconnect the power cable, fan and reset cable from the motherboard. You will not be able to disconnect the ribbon cables leading to the disk drives, as they are glued to the motherboard and are replaced along with the board.
5. Carefully slide the motherboard out of the chassis.

Prior to Replacement

- o Verify that all jumpers are set as desired (Appendix B). For users that operate their terminals exclusively at 19.2K baud, you can install a jumper at JP5 to cause initial ROM messages to be sent at 19.2K. If you've installed the Diagnostics Jumper, don't forget to remove it.
- o Verify that ROM chip U29 (Figure B-1) is of the latest revision. It is sometimes necessary to update the CPM3.SYS and SYSLDR.COM files when upgrading a ROM. This information is available through Morrow Dealer Support.
- o Be sure that all socketed IC's are seated properly with no bent leads.

Replacement

Reverse the steps for removal. Be careful to reconnect the fan, reset switch, and power harness properly.

APPENDIX A. EXTENDED ERROR CODES

The display of extended error codes is enabled when the diagnostics jumper (Figure B-1) is in place.

This section lists and explains the various BIOS and ROM error codes. Table A-1 lists the BIOS Level Error Codes; it includes the error codes returned, actual error messages, and a description of the cause of each error. Table A-2 covers the details of ROM (low-level) disk operation error codes.

Table A-1: BIOS LEVEL ERROR CODES

Error Code	Error Message	Cause	Solution
ERwp	Write Protected	The floppy diskette is write-protected.	Remove the write-protect tab on the diskette.
ERsk	Seek Error	The heads were moved to the wrong track.	Check power supply or the hard disk drive.
ERdac	Data Address CRC	The value of one or more bits in the data field changed since the data was last written.	Format and reload the hard disk; if no errors, replace the motherboard.
ERidc	ID Address CRC	The value of one or more bits in the header field changed since the header was last written.	Format and reload the hard disk; if no errors, replace the motherboard.
ERnf	Not Found	The data requested was not found on the diskette.	Check voltage to the floppy drive, replace data cable, check software for errors.
ERnr	Drive Not Ready	The hard disk is not rotating at the proper speed, or the floppy drive does not have a diskette in it when selected.	Check floppy drive door, check power supply.
ERmf	Media Failure	The sector size specifier in the data field doesn't match the system specification.	Check floppy drive; see if FOREIGN.COM is active.
EReq	Equipment Failure	There are two possible reasons for this error: either track 0 cannot be found, or the last hard disk operation terminated in a Write Fault condition.	Check hard disk drive. Reload "COPYSYS" to hard disk.

Table A-1: BIOS LEVEL ERROR CODES, Continued

ERuk	Unknown Error	The error is not known to the system.	Go to flowchart.
ERbm	Unable to ReMap	When the hard disk is in the process of trying to remap a sector, and the bad map cannot be opened or closed, this error will be generated.	Check motherboard and/or hard disk.

Table A-2 below covers the ROM level error codes, which exist only in the disk module. The value placed in the err flag, and passed back to the BIOS, is remapped in ertran. Notice that the two most significant bits are used to indicate remappable errors and those errors that should NOT be retried.

Table A-2: ROM (LOW-LEVEL) DISK OPERATION ERROR CODES

Error Code	Error Message	Cause	Solution
1 Eun	Unreadable Media	The system is unable to read anything from the disk.	Check floppy disk drive and/or software.
43 Ehd	Header Error	There was an error in reading the header field.	Check floppy disk drive.
43 Eha	Mismatch: Header ID Address Mark	The system could not find an address mark on the disk.	Check floppy disk drive.
44 Ehc	Mismatch: Header CRC	The header's CRC value is incorrect.	Check software.
45 Eda	Mismatch: Data Address Mark	The system could not find the data address mark following the header.	Check motherboard.
46 Edc	Mismatch: Data CRC	The data field's CRC value is incorrect.	Check motherboard.
7 Esk	Mismatch: Track Number (seek error)	The track number read from the current track does not match the or desired track (PHYTRK).	Check power supply, floppy disk drive motherboard.

Table A-2: ROM (LOW-LEVEL) DISK OPERATION ERROR CODES, Continued

88 Ehn Mismatch: Head Number	The head number read from the track does not match the desired head number (PHYHD).	Check the hard disk or floppy disk drive, or components located at U56, U74 or U85 on the motherboard.
49 Esn Mismatch: Sector Number	The system could not find the number of the current sector (PHYSEC).	Same as above.
8A Ess Mismatch: Sector Size	The size of the sector read from the current track does not match the desired sector size (\$SIZMSK) in the current Mtab's dskdefl.	Same as above.
8 Enh Drive Failure to Find Track 0	The drive's track 0 sensor isn't working.	Reformat & reload hard disk.
8C Emc Maximum Cylinder Number Exceeded	A track beyond the maximum track number was requested.	Same as above.
D Enr Drive Not Ready	The hard drive's Ready line did not assert, or for a floppy drive, the diskette is not turning.	Check power supply, hard disk, and data cables.
8E Eto Motor Time-out	The last disk operation failed to complete before the timer "timed-out".	Same as above.
8F Ewp Write Protected	The system attempted to write on a floppy diskette that was write-protected.	
90 EWF Write Fault	The Write Fault line was asserting after the last hard disk write operation.	
91 Ebf Bad Map is Full	The current sector remapping operation could not be completed because the bad map is already full.	
92 Ebi Bad Map ID Does Not Match	The ID byte, carried in the the bad map's pointer structure in the boot sector, is incorrect.	

Table A-2: ROM (LOW-LEVEL) DISK OPERATION ERROR CODES, Continued

93 Ebr Mismatch: Bad Map Revision Number	The revision in the header to the bad map is too low.
94 Ebn Bad Map Not Open	An attempt was made to close the bad map before it was opened.
95 Euk Unknown Error Code	The error was not known to the system.

APPENDIX B: MOTHERBOARD PORTS, CONNECTORS & JUMPER BLOCKS

Figure B-1 illustrates all of the motherboard connectors, jumper blocks and critical chip locations. It can be used for reference when reading the rest of this section.

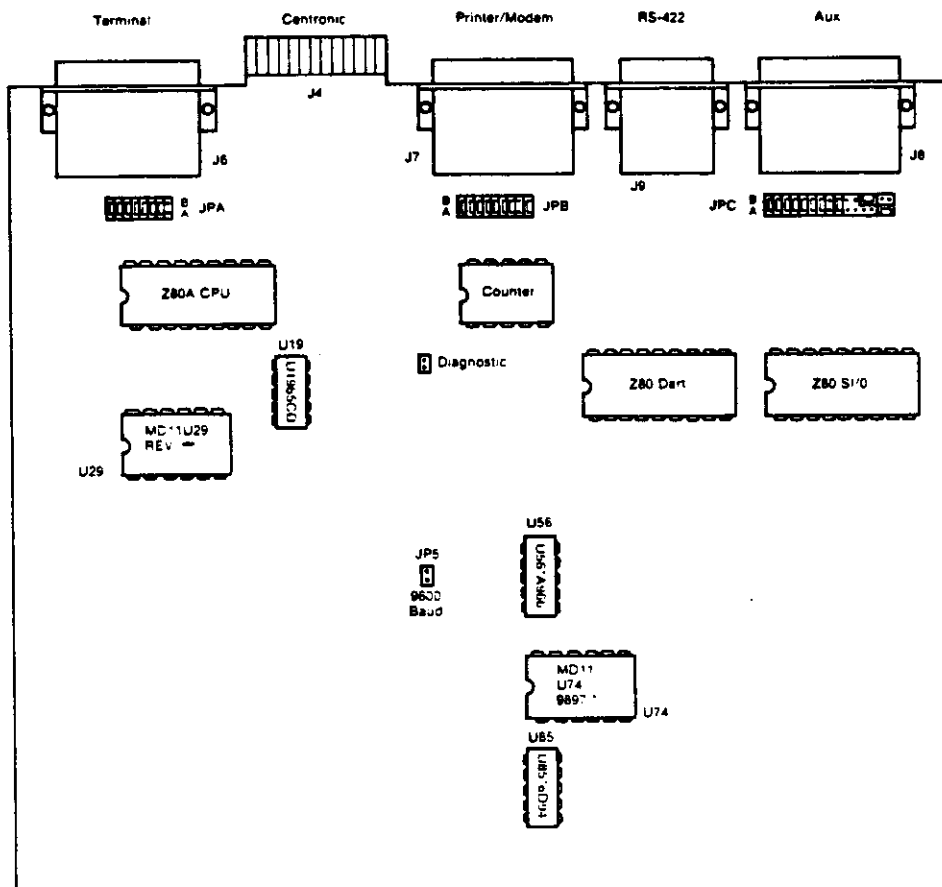


Figure B-1: Motherboard Details

The jumpers this section covers, and the details they determine, are:

JPA	TERMINAL connector pinouts
JPB	PRINTER/MODEM connector pinouts
JPC	AUXILIARY connector pinouts
JP3	Data-in select between RS-232 & RS-422
	AUX connectors
JP5	ROM boot message at 9600 / 19.2K baud
Unnumbered	Diagnostics mode on boot yes / no

JP1, JP2

JP1 determines how much of memory is shared by both banks, and must be left IN for proper operation of CP/M as configured by Morrow. JP2 is actually bridged by a circuit board trace. If the trace is cut, JP2 determines whether pins 7-9 of JPC are low (normal) or high.

Serial Connectors (JPA, JPB, JPC)

The serial connectors on the motherboard conform to RS-232 standards and use DB 25/S connectors. Figure B-2 illustrates the connector layout, and Table B-1 identifies the signal associated with each of the pins.

Most peripheral options can be handled with the SETUP program. If you want to use a non-Morrow modem on either of your serial ports, however, it may be necessary to reconfigure the pinouts of that port with jumpers contained on the Micro Decision circuit board.

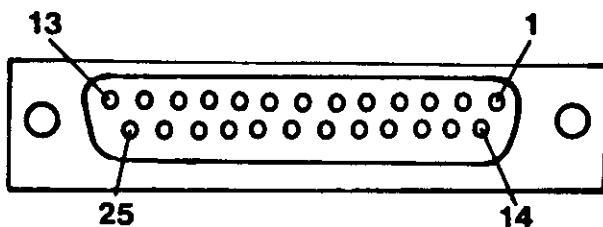


Figure B-2. Serial Port Pin Arrangement - Rear View

Table B-1. RS-232 Signal Descriptions

Pin #	Signal
1	Frame Ground
2	Receive Data Input
3	Transmit Data Output
4	Request To Send Input
5	Clear To Send Output
6	Data Set Ready Output
7	Signal Ground
8	Carrier Detect Output
9 *	+12V Output
10 *	-12V Output
11 *	Alternate Handshake Line
14 *	+5V Output
17 *	Receiver Clock Output
20	Data Terminal Ready Input
24 *	Transmitter Clock Input

* These signals are available on the printer/modem and auxiliary connectors only.

On the circuit board in front of each serial connector is a set of jumper headers labeled JPA, JPB and JPC.

JPA has 8 pairs of jumpers for defining the terminal port; JPB has 9 pairs that define the printer/modem port. JPC has 15 pairs that define the auxiliary port.

Slip-on connectors are used to make the RS-232C pin assignments. By changing the positions of some connectors, the ports can be configured for use with modems. (For those familiar with telecommunications jargon, the jumpers select whether the serial connector is set up to talk to DCE or to DTE equipment.)

Accessing the Jumpers

Before you begin, PARK THE HARD DISK, TURN OFF THE MICRO DECISION POWER SWITCH and UNPLUG THE POWER CORD.

- o Remove the four screws securing the cover to the chassis.
- o Carefully slide the cover towards the front (it is not necessary to remove it completely). Each jumper block is located in front of the related serial port.

JPA/JPB Factory Settings

You would configure the terminal port for a modem if you wanted to call up the Micro Decision from a remote terminal or computer and use it as if you were connected locally.

The signal present on each jumper pin in JPA and JPB is shown in Table B-2 along with the factory setting for the feeding of the signals to the RS-232C connectors. This signal configuration is accomplished through circuit board wiring and the factory jumper settings, as shown in Figure B-3.

Table B-2: JPA/B Pinouts (Terminal Setup - DTE)

<u>JPA/B Pin#</u>	<u>Signal</u>	<u>RS-232C Pin#</u>
(1A)	RxD to DART	2
(2A)	RD to device	3
(3A)	DSR to device	6
(4A)	DSR/ to DART	4
(5A)	DTR from device	20, 5
(6A)	DTR/ from DART	20, 5
(7A)	+12V	8
(8A)	+12V	8
(9A) *	+12V	8, 11
(9B) *	DET from device	8, 11
(8B)	CTS/ to DART	8
(7B)	CD from device	8
(6B)	CTS to device	20, 5
(5B)	CTS/ to DART	20, 5
(4B)	RTS from device	4
(3B)	RTS/ from DART	6
(2B)	TxD from DART	3
(1B)	TD from device	2

* JPB only

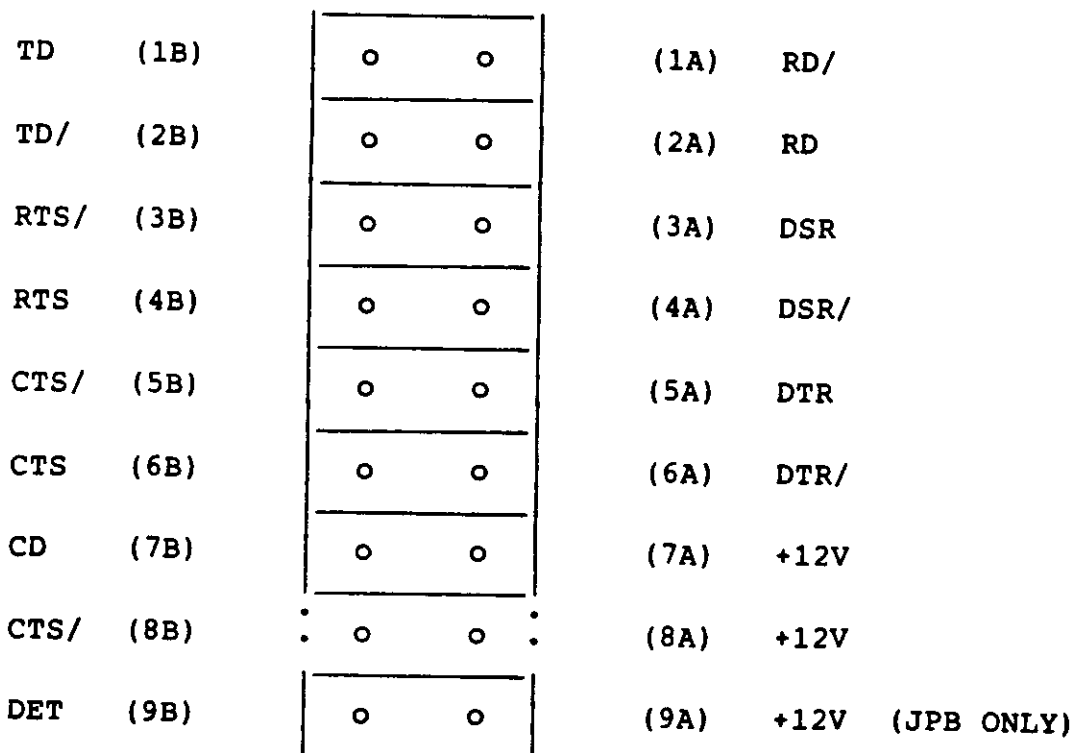


Figure E-2. Factory Jumper Settings for JPA/B

When setting up JPA or JPB for use with a modem, the jumper modifications depend on whether your modem cable has pin 2 at one end tied to pin 3 at the other, and vice versa. This crisscrossing is frequently, but not always, found in modem cables. If you're not sure which type you have, use an ohmmeter or continuity tester to find out.

JPA and JPB Settings for Modems

For cables that crisscross pins 2 and 3, arrange the jumpers as shown below.

TD	(1B)	o	o	(1A)	RD/
TD/	(2B)	o	o	(2A)	RD
RTS/	(3B)	o	o	(3A)	DSR
RTS	(4B)	o	o	(4A)	DSR/
CTS/	(5B)	o	o	(5A)	DTR
CTS	(6B)	o	o	(6A)	DTR/
CD	(7B)	o	o	(7A)	+12V
CTS/	(8B)	o	o	(8A)	+12V
DET	(9B)	o	o	(9A)	+12V JPB ONLY

Figure B-4: JPA/B Settings for Modems Using Null Modem Cables

For cables that connect pin 2 to pin 2 and pin 3 to pin 3, set your jumpers as shown in Figure B-5.

TD	(1B)	○	○	(1A)	RD/
TD/	(2B)	○	○	(2A)	RD
RTS/	(3B)	○	○	(3A)	DSR
RTS	(4B)	○	○	(4A)	DSR/
CTS/	(5B)	○	○	(5A)	DTR
CTS	(6B)	○	○	(6A)	DTR/
CD	(7B)	○	○	(7A)	+12V
CTS/	(8B)	○	○	(8A)	+12V
DET	(9B)	○	○	(9A)	+12V

Figure B-5: Alternate JPA/B Settings for Modems

Factory Settings for JPC

The Auxiliary port would be configured for a modem if you want to use the Micro Decision as a terminal contacting remote computers or data bases.

NOTE: The Auxiliary port comes from the factory configured as DTE; with most modems you have to change jumper settings on JPC as well as installing the software for this port. However, with Morrow's MM300 modem and ReachOut software, neither operation is required.

The signal present on each jumper pin in JPC is shown in table B-3, along with the factory setting for the feeding of the signals to the RS-232C connector. The signal configuration is accomplished through circuit board wiring and the factory jumper settings, as shown in Figure B-6.

Table B-3: JPC Pinouts (Modem Setup - DCE)

<u>JPC Pin#</u>	<u>Signal</u>	<u>RS-232C Pin#</u>
(1A)	RxD to ZSIO	2
(2A)	RD to device	3
(3A)	DSR to device	6
(4A)	CD to ZSIO	4
(5A)	DTR from device	20
(6A)	DTR/ from ZSIO	5
(7A)	TTL false (<-3V)	8,11
(8A)	TTL false	8,11
(9A)	TTL false	8,11
(10A)	Receiver clock to device	17
(11A)	RS-232 Receiver input	N/C
(12A)	TTL output of RS-232 rcvr	N/C
(13A)	Transmit clock to RS 422	N/C
(14A)	Transmit clock to ZSIO	N/C
(15A)	Transmit clock to ZSIO	N/C
(15B)	Receiver clock to ZSIO	N/C
(14B)	RS 422 receiver clock	N/C
(13B)	Baud clock output	N/C
(12B)	Rcvr clock input to ZSIO	N/C
(11B)	TC (external clock)	24
(10B)	RS-232 level clock out	N/C
(9B)	DET (alternate handshake)	8,11
(8B)	CTS/ to ZSIO	20
(7B)	CD from device	8,11
(6B)	CTS to device	5
(5B)	CTS/ to ZSIO	20
(4B)	RTS from device	4
(3B)	RTS/ from ZSIO	6
(2B)	TxD from ZSIO	3
(1B)	TD from device	2

TD	(1B)	o	o	(1A)	RD/
TD/	(2B)	o	o	(2A)	RD
RTS/	(3B)	o	o	(3A)	DSR
RTS	(4B)	o	o	(4A)	DSR/
CTS/	(5B)	o	o	(5A)	DTR
CTS	(6B)	o	o	(6A)	DTR/
CD	(7B)	o	o	(7A)	<-3V
CTS/	(8B)	o	o	(8A)	<-3V
DET	(9B)	o	o	(9A)	<-3V
	(10B)	o	o	(10A)	
	(11B)	o	o	(11A)	
RxCB	(12B)	o	o	(12A)	
U2CLK	(13B)	o	o	(13A)	
	(14B)	o	o	(14A)	
	(15B)	o	o	(15A)	

Figure B-6: Factory Jumper Settings for JPC

JPC Settings for Modems

The jumper settings for JPC depend upon the type of modem cable you have. For cables that crisscross pins 2 and 3, arrange the jumpers as shown in Figure B-7.

TD	(1B)	o	o	(1A)	RD/
TD/	(2B)	o	o	(2A)	RD
RTS/	(3B)	o	o	(3A)	DSR
RTS	(4B)	o	o	(4A)	DSR/
CTS/	(5B)	o	o	(5A)	DTR
CTS	(6B)	o	o	(6A)	DTR/
CD	(7B)	o	o	(7A)	<-3V
		:	:		
		:	:		

(The rest are the same as factory.)

Figure B-7: JPC Settings For Modems with Null Modem Cable

When using a modem cable that connects pin 2 to pin 2 and 3 to 3, the jumper setup is the same as above except for positions (1A), (2A), (2B), and (1B). See the difference below.

TD	(1B)	o	o	1	(1A)	RD/
TD/	(2B)	o	o	2	(2A)	RD
		:	:			
		:	:			
		:	:			

Figure B-8: Alternate JPC Setting for Modems

JP3

JP3 is a 3-pin header located between the Z80 SIO chip and the RS-232 AUX connector. It determines whether inbound data to RxD of the SIO comes from pins 5 and 6 of the RS-422 Aux connector, or pin 2 of the RS-232 Aux connector.

Z80 SIO

o o o
 \ /

Factory setting: Received data to SIO from RS-232

AUX
Connectors

JP5

JP5 is a two-pin header between U53 and U54, toward the center of the board. If it is unjumped, any pre-boot ROM messages are sent to the console at 9600 baud. These include "Testing memory", the ROM version number message, the ROM diagnostics, and "Do you want to boot from the floppy?"

This baud rate is in effect until CPM3.SYS is loaded during the boot process. Then the baud rate contained there, as configured by the SETUP program, takes over.

With JP5 jumpered, these messages are transmitted at 19,200 baud.

The default post-boot console baud rate in CPM3.SYS and CPM3F.SYS is 9600. If this has not been changed by SETUP, jumpering JP5 changes the default to 19,200. If it has been changed with SETUP, the baud rate changes during boot to whatever value was selected with SETUP.

The Diagnostics Jumper

This is a two-pin header that has no JP number. It is located next to U22 towards the center of the motherboard.

When jumpered, the Micro Decision displays a diagnostics menu immediately on power-up or a reset. The available options include barber-pole output patterns to the serial and parallel ports. There is also a loop test on the printer/modem port. Finally is an infinite loop memory test that is identical to the normal power-up memory test. See Section 3.

Secondly, with the jumper in place, any CP/M disk error messages are accompanied by a more-specific error code, as a diagnostic tool. The error codes are listed and defined in Appendix A. This jumper is meant to be in place only while the Micro Decision is being serviced.

Port Addresses

The TERMINAL and PRINTER/MODEM ports are controlled by a Zilog Z-80 DART (dual UART). The AUXILIARY port is controlled by a Zilog SIO (serial I/O) chip. The DART port locations are shown in Table B-4.

Table B-4: DART Port Locations

<u>Port</u>	<u>Location</u>
Terminal Data Port	060H
Terminal Status Port	061H
Printer/Modem Data Port	062H
Printer/Modem Status Port	063H
Auxiliary Data Port	070H
Auxiliary Status Port	071H

The bits that represent Character Ready and Transmit Ready in the controller's STATUS register are:

CHAR RDY = bit 0
TRANSMIT RDY = bit 2

I/O Ports

The Micro Decision uses all 256 I/O ports. The address lines are decoded to provide nine blocks of ports, as listed in Table B-5 below.

Table B-5: I/O Port Assignments

<u>Range</u>	<u>Name</u>	<u>Function</u>
00 - FF	IO00	Expansion bank 0
10 - 1F	IO10	Expansion bank 1
20 - 2F	IO20	Expansion bank 2
30 - 3F	IO30	Expansion bank 3
40 - 4F	LPORTS-WRITE	
50 - 5F	TIMER	8253 counter timer
60 - 6F	DART	Dual UART
70 - 7F	LPORTS-READ	

RS-422 Pin Connections

The RS-422 connector leading from the MODEM port is a high speed synchronous serial port. It allows you to send to and receive information from a mainframe computer. The pin connections are detailed in Table B-6 below.

Table B-6: RS-422 Pin Connections

Pin #	Signal
1	Transmitted data +
2	Transmitted data -
3	Transmit clock +
4	Transmit clock -
5	Received data +
6	Received data -
7	Receiver clock +
8	Receiver clock -
9	Ground
10	Ground
11	Ground
12	Ground
13	Ground
14	Ground
15	Ground

Expansion Connector (J5)

J5 is a 40-pin connector near the disk drive connector. It is intended for future use a connector to circuit boards that provide enhancement functions, such as a networking board.

Table B-7: J5 I/O Bus Connector Pinouts

<u>Pin</u>	<u>Signal</u>	<u>Description</u>
1	/BRD	Buffered I/O read
3	/BWR	Buffered I/O write
5	/RESET	Z80 reset line (output)
7	/4M	4MHz Z80 clock
9	/IO00	Decoded I/O space at 00-0Fh
11	/IO10	Decoded I/O space at 10-1Fh
13	/IO20	Decoded I/O space at 20-2Fh
15	/IO30	Decoded I/O space at 30-3Fh
17	AB3	Address line 3
19	AB2	Address line 2
21	AB1	Address line 1
23	AB0	Address line 0
25	DB7	Data bus bit 7
27	DB6	Data bus bit 6
29	DB5	Data bus bit 5
31	DB4	Data bus bit 4
33	DB3	Data bus bit 3
34	-12	-12VDC
35	DB2	Data bus bit 2
36	+12	+12VDC
37	DB1	Data bus bit 1
38	+5	+5VDC
39	DB0	Data bus bit 0
40	+5	+5VDC

Parallel (Centronics) Port (J4)

The pinouts of the 34-pin edge connector are listed below.

Table B-8: Parallel Connector Pinouts

<u>MD-out</u>	<u>Signal</u>	<u>Cent. Pin #</u>
2	STROBE	1
4	DATA BIT 0	2
6	DATA BIT 1	3
8	DATA BIT 2	4
10	DATA BIT 3	5
12	DATA BIT 4	6
14	DATA BIT 5	7
16	DATA BIT 6	8
18	DATA BIT 7	9
20	ACKNOWLEDGE	10
22	READY/BUSY	11
25	RESTORE/PRIME	31
27	CFAULT	32

Odd pins 1-23 and 33 are grounded; all others are not connected.

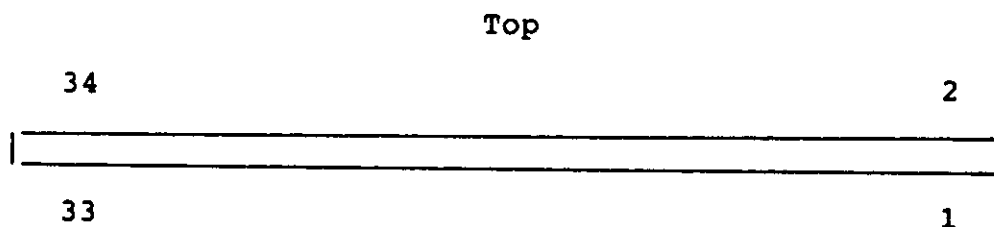


Figure B-9: Parallel Port Orientation (Rear View)

APPENDIX C. THEORY OF OPERATION

Architecture

Hard Disk Micro Decisions are designed to support the CP/M 3.0 operating system. Their features include:

- o 128K Ram, 2 banks of 64K sharing 4K common
- o 3 serial ports (one can be configured EIA 422)
- o 1 parallel port
- o Integrated floppy/hard disk controller
- o Special hardware data transfer mode (allows reads from current bank and writes to alternate bank)

Memory Organization

The 128k of dynamic RAM is organized as two blocks of 64k each. The top 4k of the 64k address space is common to both banks. Most of the operating system and the disk buffers are located in bank 2 so that users are allowed a much larger TPA space (56k) in bank 1. Bank 2 consists primarily of disk cache buffers.

In addition to RAM there is an 8k ROM that is activated upon power on or upon a cold reset. A short group of diagnostic routines are run, and when the boot process is finished the ROM is disabled. ROM is re-enabled as special code that the Z80 executes while doing disk transfers. During disk transfers instructions relating to the flow of control are executed from ROM while actual control codes are loaded to the controller PAL, while each byte is read/written directly into the bank 2 (or bank 1) disk buffers. Remember, the disk buffers are part of bank 2, and not separate RAM like most systems, so disk access is extremely fast.

The logic for controlling the memory is very complicated and is implemented in a PAL (Programmed Array Logic). The important thing to know is that the boot ROM actually becomes active for disk transfers, so upgrades and revisions to the disk controller would require that the boot ROM be changed. The architecture of the computer is shown in Figure C-1.

Interrupt Logic

The interrupt logic is relatively simple. Interrupts can be generated by any one of the three serial ports, the parallel port, or the disk logic. The three serial ports are implemented by a dual UART (DART) and a single UART (SIO). These devices are wired to support Z80 Mode 2 interrupts.

The serial ports generate interrupts upon buffer full, buffer empty, or error. The parallel port also generates an interrupt for each byte transferred. The disk logic generates interrupts on index pulses, upon no header match error, and whenever the floppy motor turns off after its 4 second on time. Each of these interrupt conditions generates a unique vector in a0-a7. Of course the I register previously loaded by the programmer contains a8-a15, and upon interrupt this address points to the starting address of the interrupt handling routine.

The Disk Controller

The real efficiency and advanced performance of the hard disk Micro Decision are to be found in the disk controller design.

First of all, the same logic supports both the floppy disk and the hard disk. Second, data transfers take place directly between the shift register where the bytes are assembled, and RAM. Finally, for the floppy disk, most of the logic is actually implemented in software, with the Z80 being synchronized with the byte transfers. The same is true for hard disk operation, except that there is not enough time between bytes for any real program flow.

The disk controller can be viewed as a 24-bit-wide state machine:

- o 8 control bits originate in the control ROM/latch (U19 & 35)
- o 8 bits of next-address information are taken from the Z80 address bus, while the Z80 executes code from a specially remapped section of the ROM. Each instruction fetch is synchronized with the bytes of read/write data.
- o 8 bits of data, which may be viewed as a pipe between RAM and the disk byte shift register. When reading a header this byte contains data to be compared with the incoming data stream.

When reading data, bytes assembled in the shift register are loaded to contiguous memory locations at the end of each cycle. For writing, bytes are gathered from RAM, loaded into the shift register and shifted out into the write data stream. This simple arrangement is complicated only by the fact that CRC data bytes are assembled in hardware and shifted into the shift register in serial form and not transferred to or from RAM. Remember, when reading a header and comparing CRC bytes, the incoming data is not assembled into the shift register, but rather compared with the contents of the shift register.

The disk controller logic is implemented in a FPLS (Field Programmable Logic Sequencer). This device is supported by an additional PAL called the Write PAL, and the Dram PAL, control ROM and the top 4k of the boot ROM.

Low Level Code

For hard disk Read/Write/ReadHeader/Format operations, the Z80 executes code (entry 27E0) to simply develop "next address" information, and to service "Index" and "Not Match" interrupts. Most control bytes originate in the ROM.

The Z80 code for hard disk operations resides from 2000h to 2FFFh:

2000 - 23FF	Not used
2400 - 27FF	PREBUF
2800 - 2BFF	Actual R/W Buffer
2C00 - 2FFF	POSTBUF

The ROM overlays RAM. For example, during a write to the hard disk, the data to be written is fetched from ??? 280C, and the next instruction is fetched from ROM at the same address. The address lines also determine the next control byte; the Z80 is synchronized to the end of each read/write byte.

Four sections of ROM can be mapped into locations 2000 through 2FFF. Each section provides the "next address" instructions for one of the following operations:

0	Read data
1	Write data
2	Read header
3	Format track

Each 1K section is actually 32 contiguous bytes, repeated 32 times. Therefore the four 4K options actually reside in only 512 bytes of ROM.

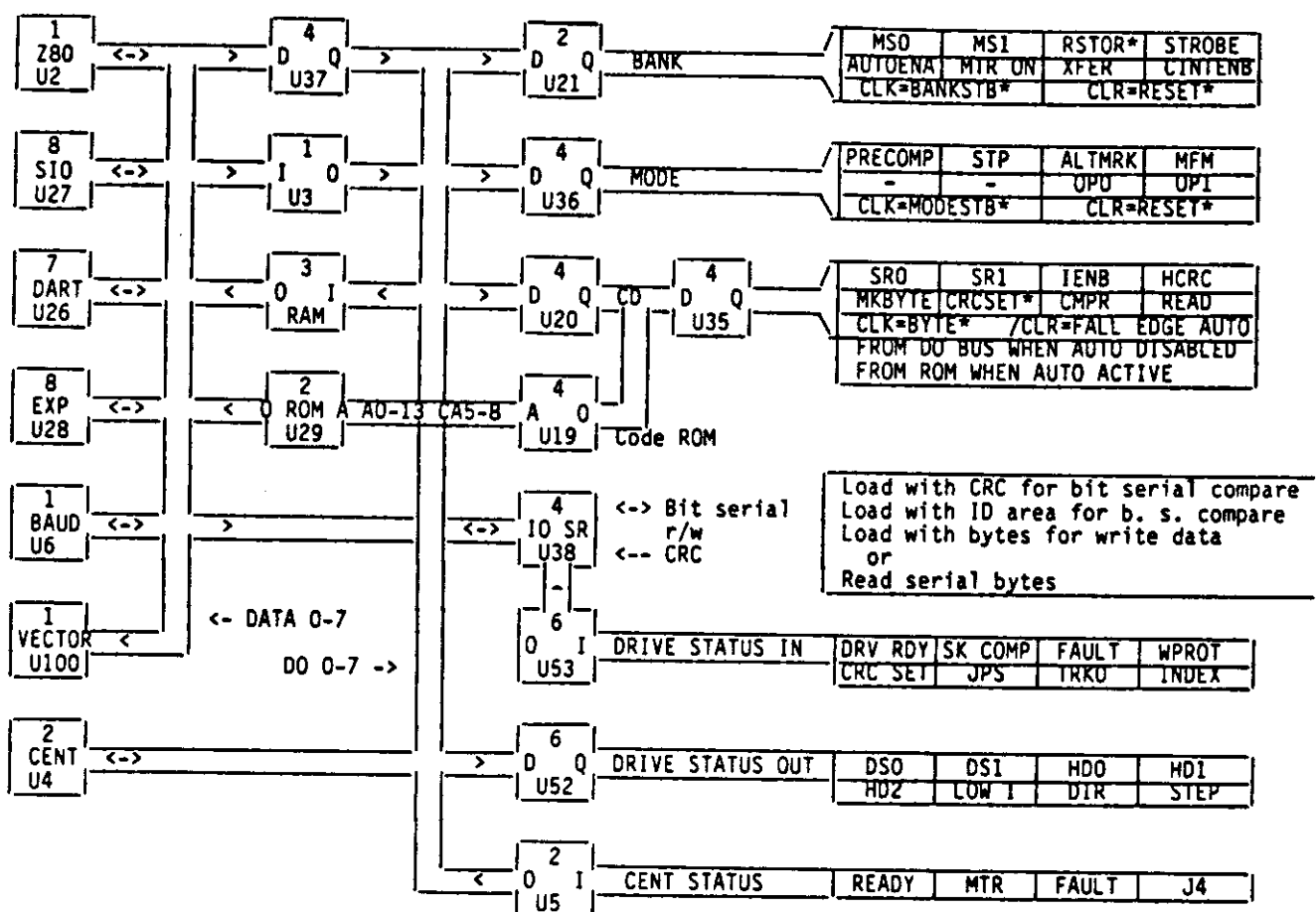


Figure C-1. Hard Disk Micro Decision Architecture

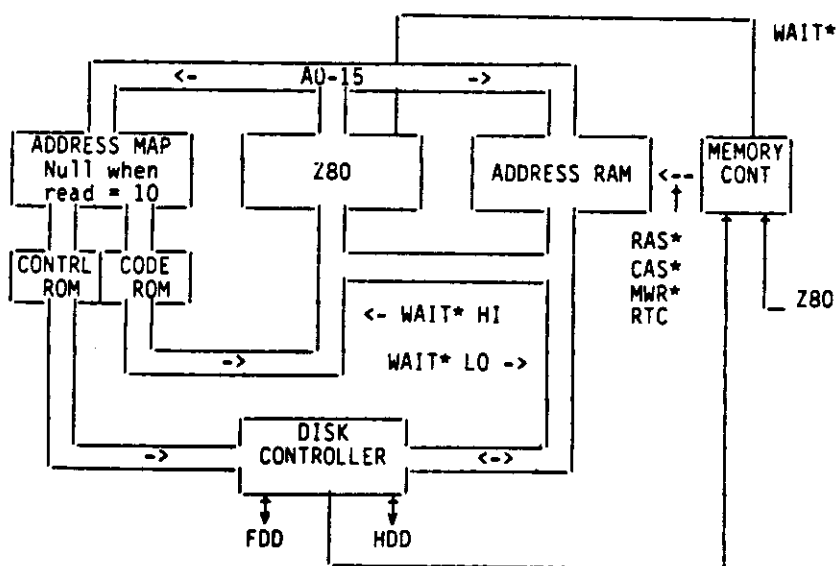
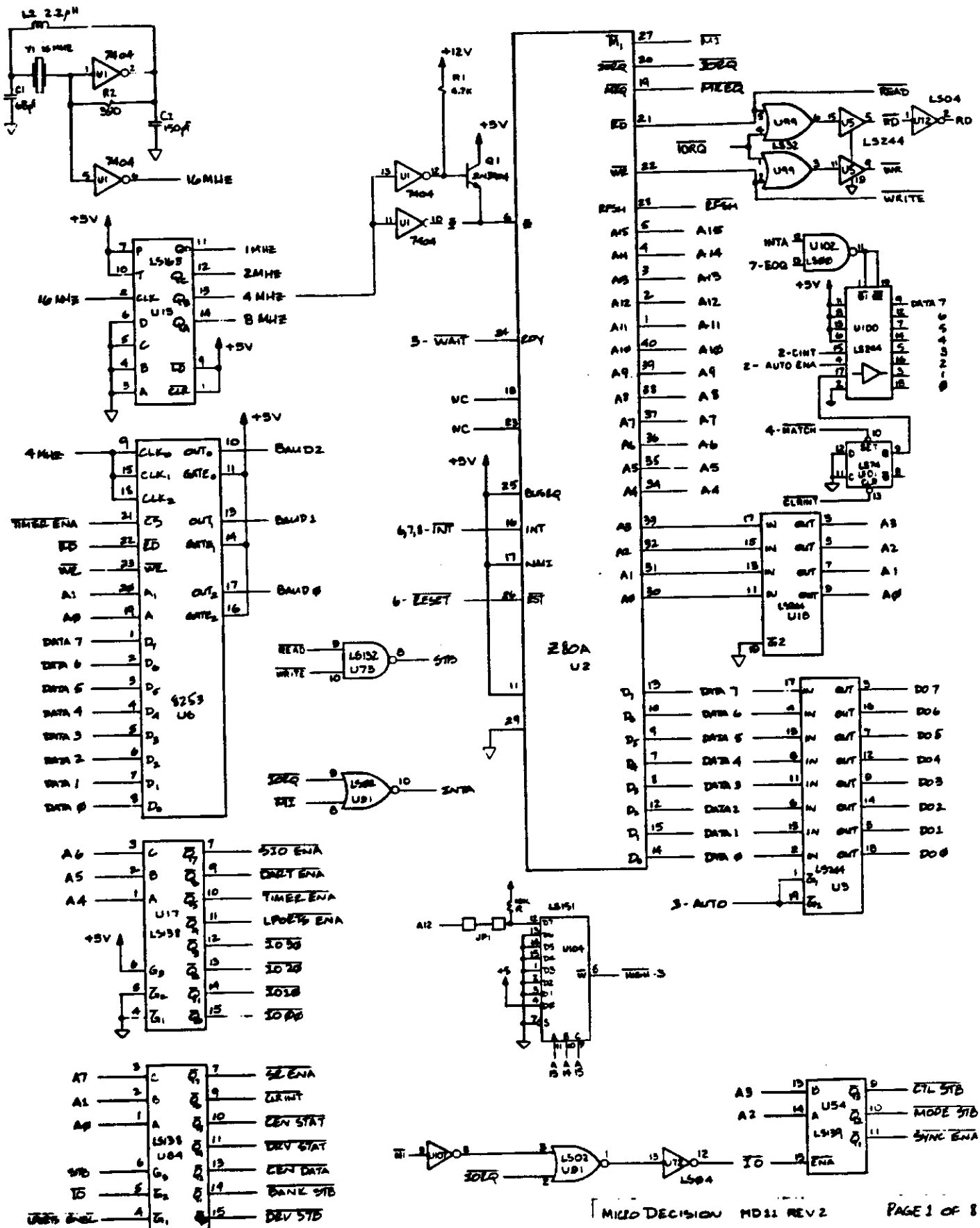
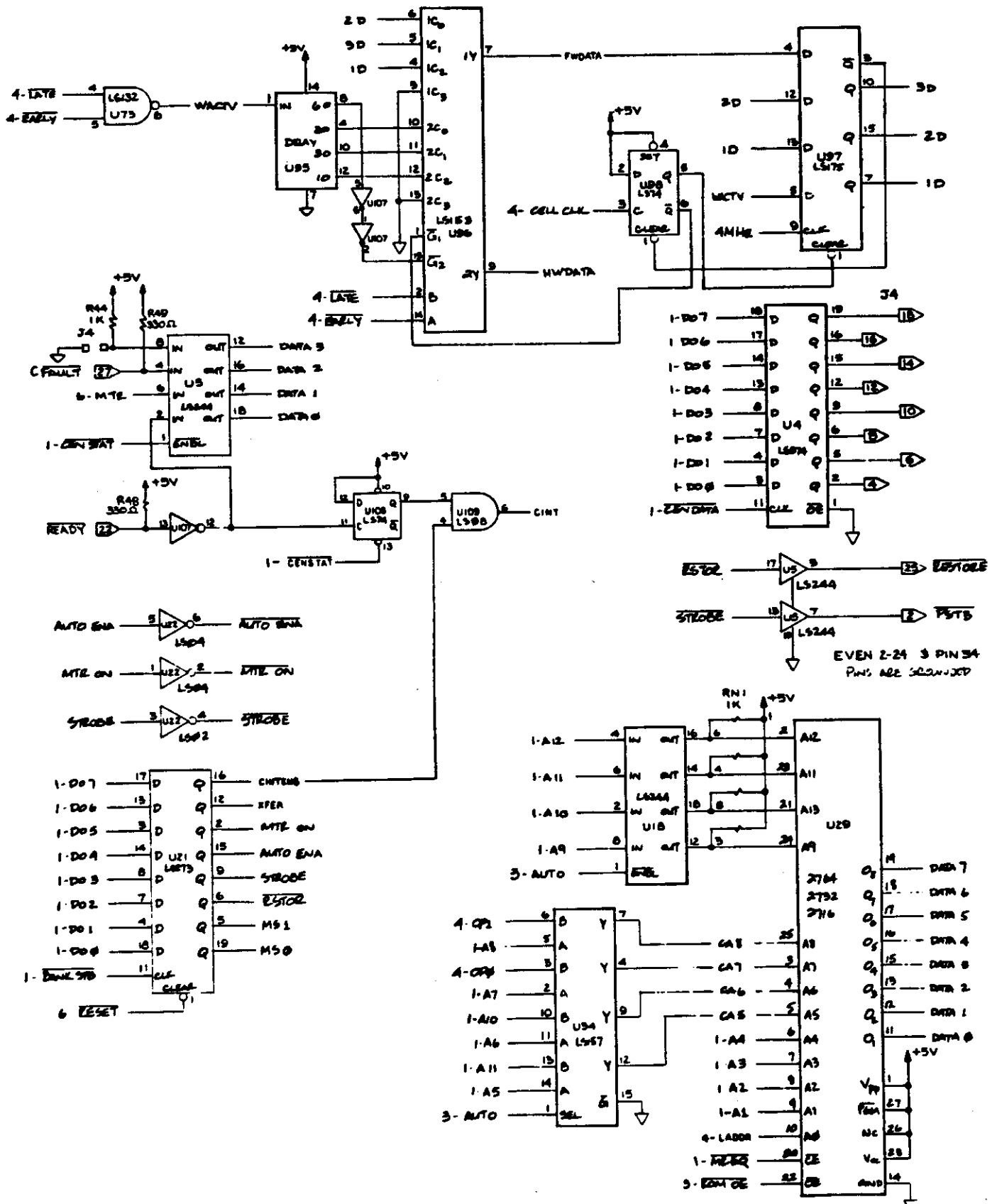


Figure C-2. Disk/Memory Transfer Routing

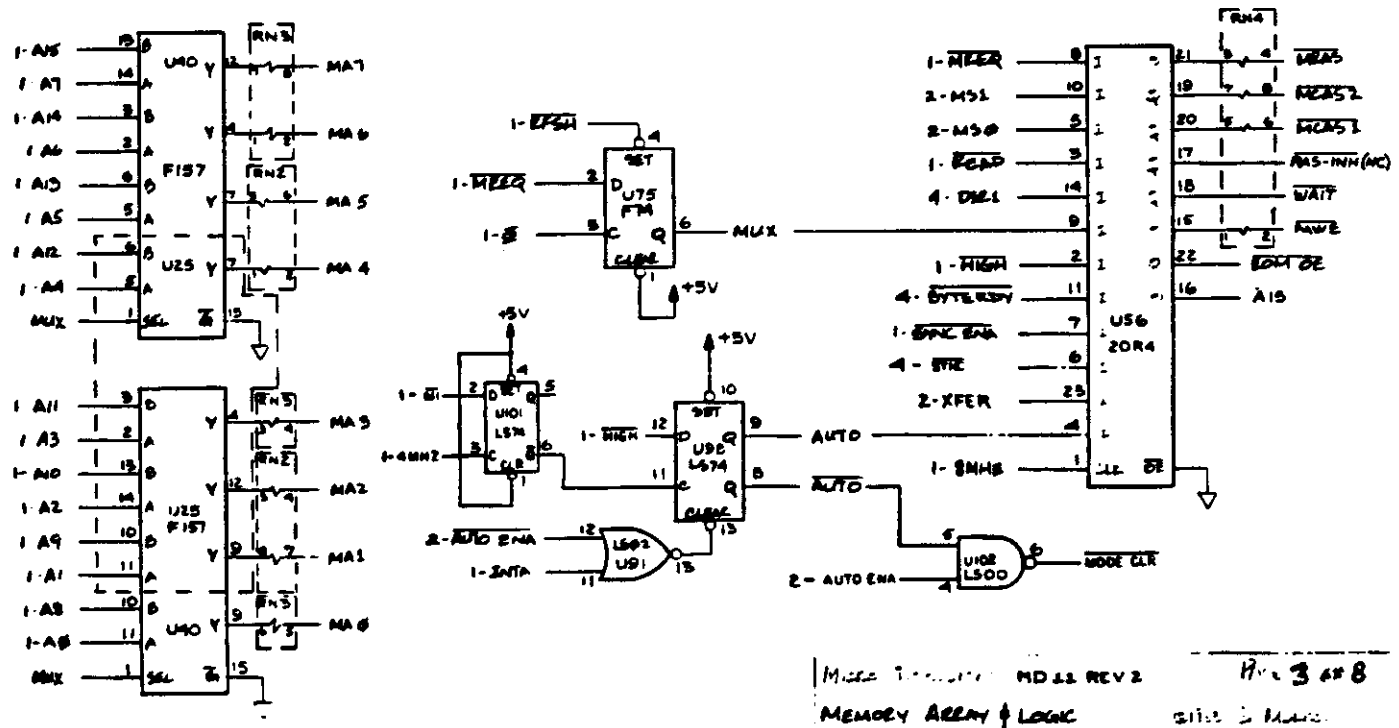
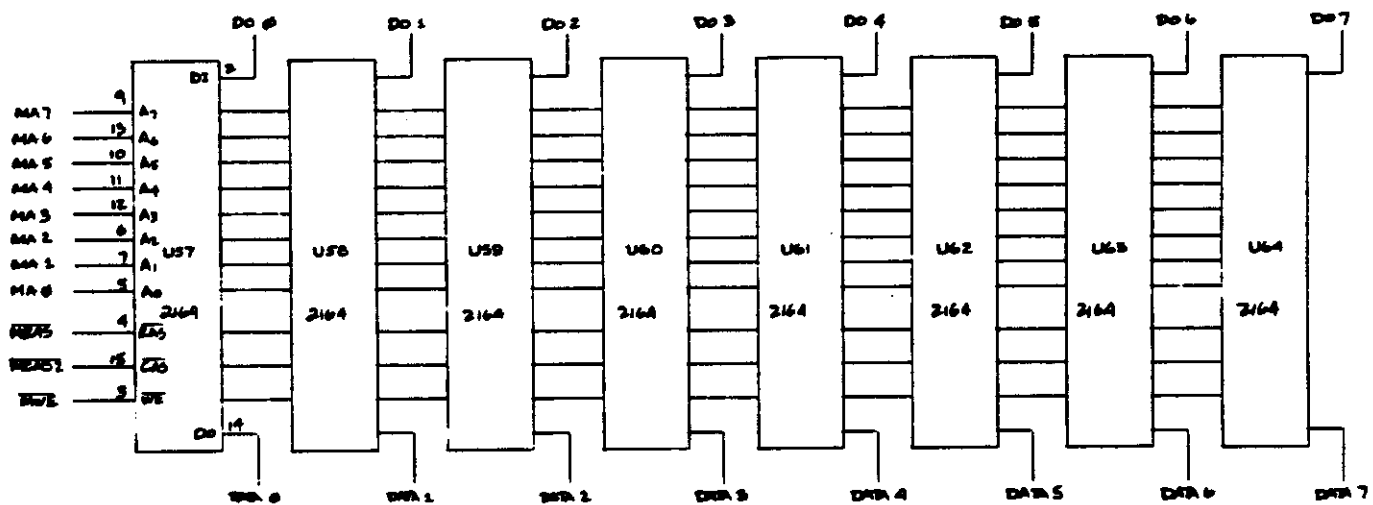
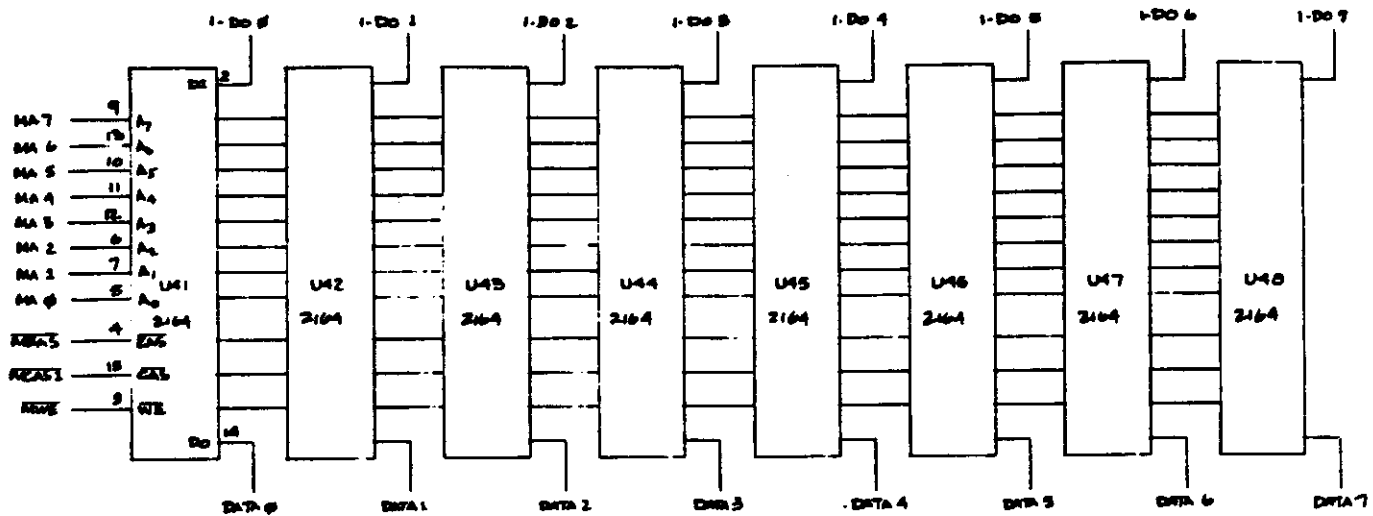
APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



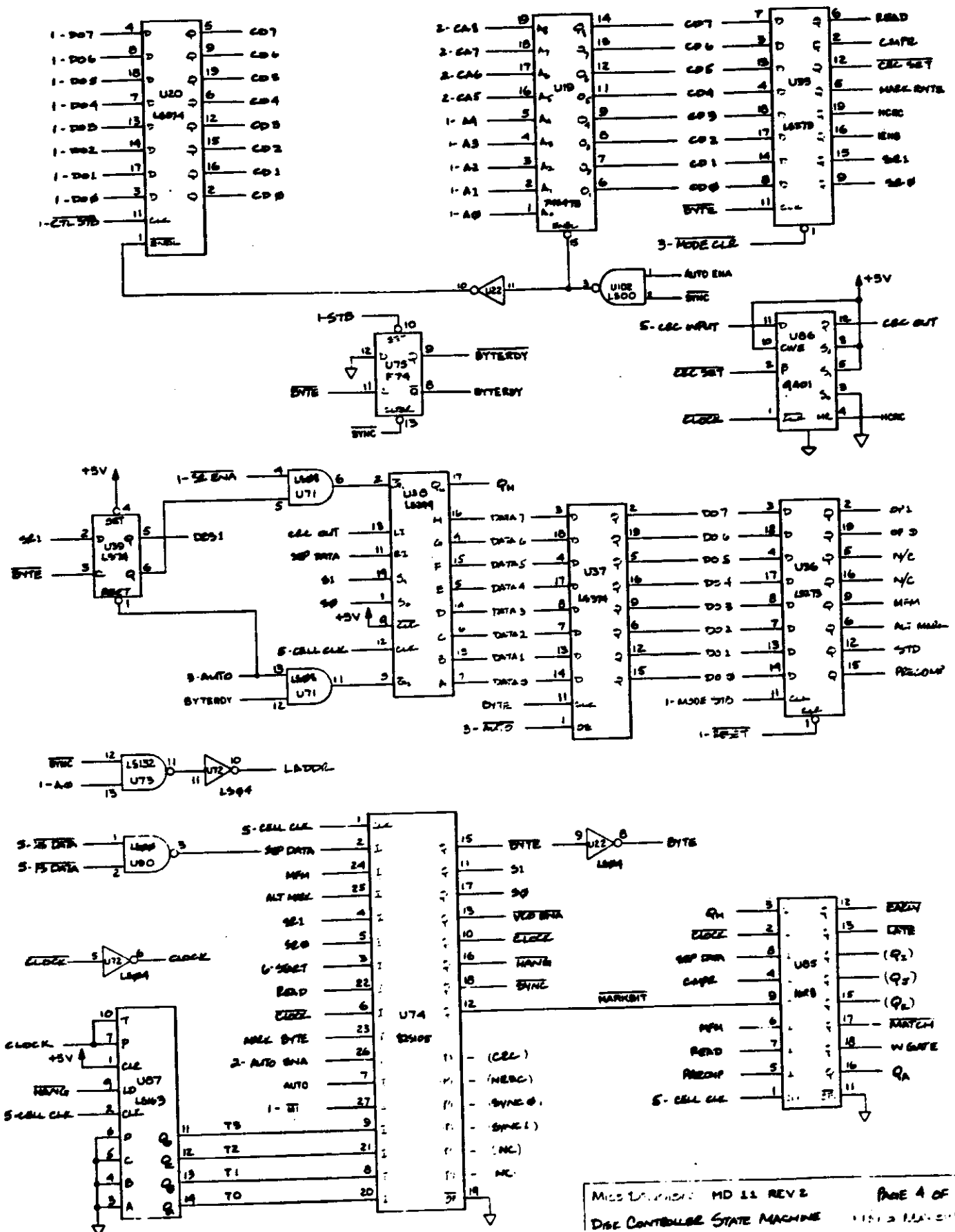
APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



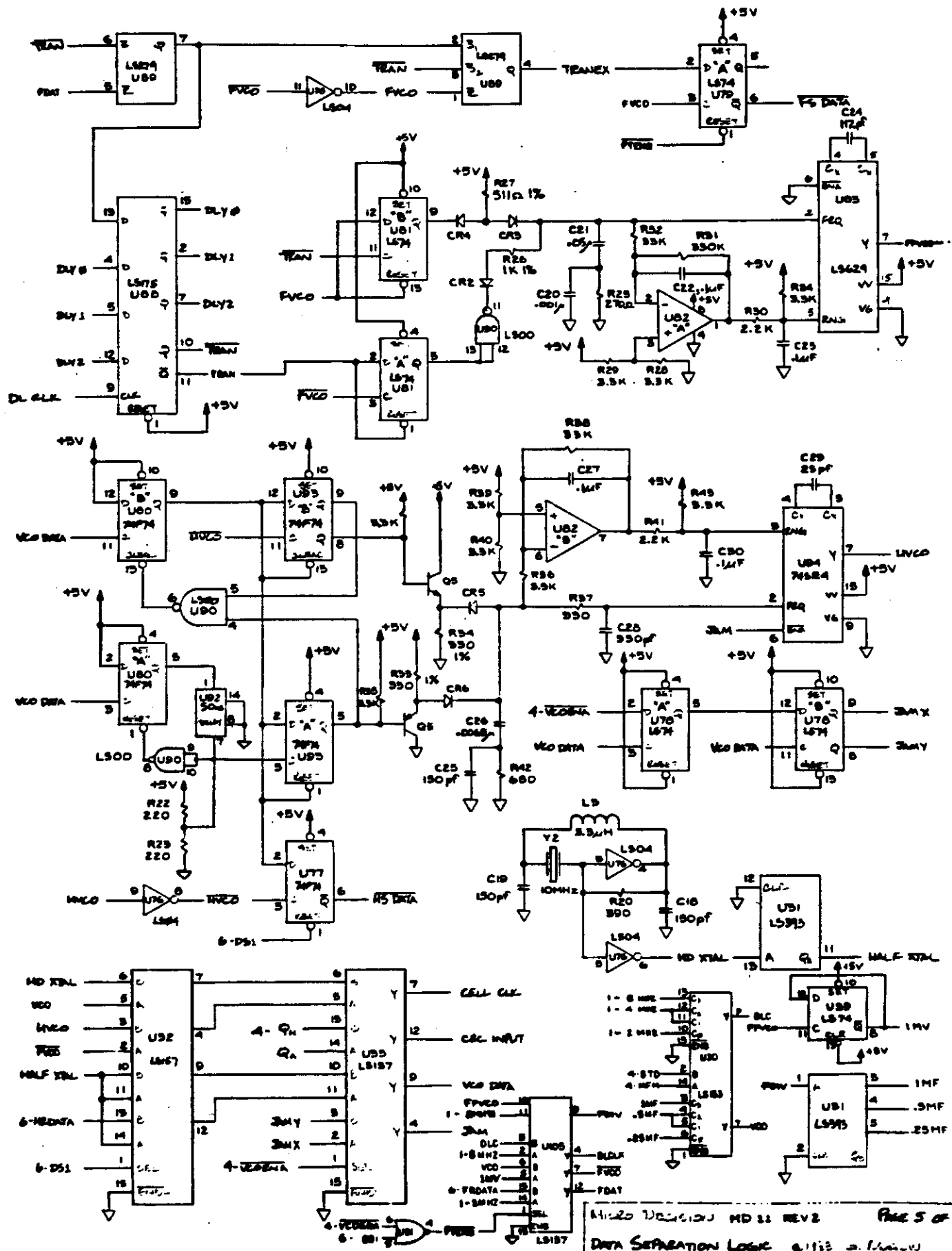
MD 11 REV 2
MEMORY ARRAY & LOGIC

Nov 3 48

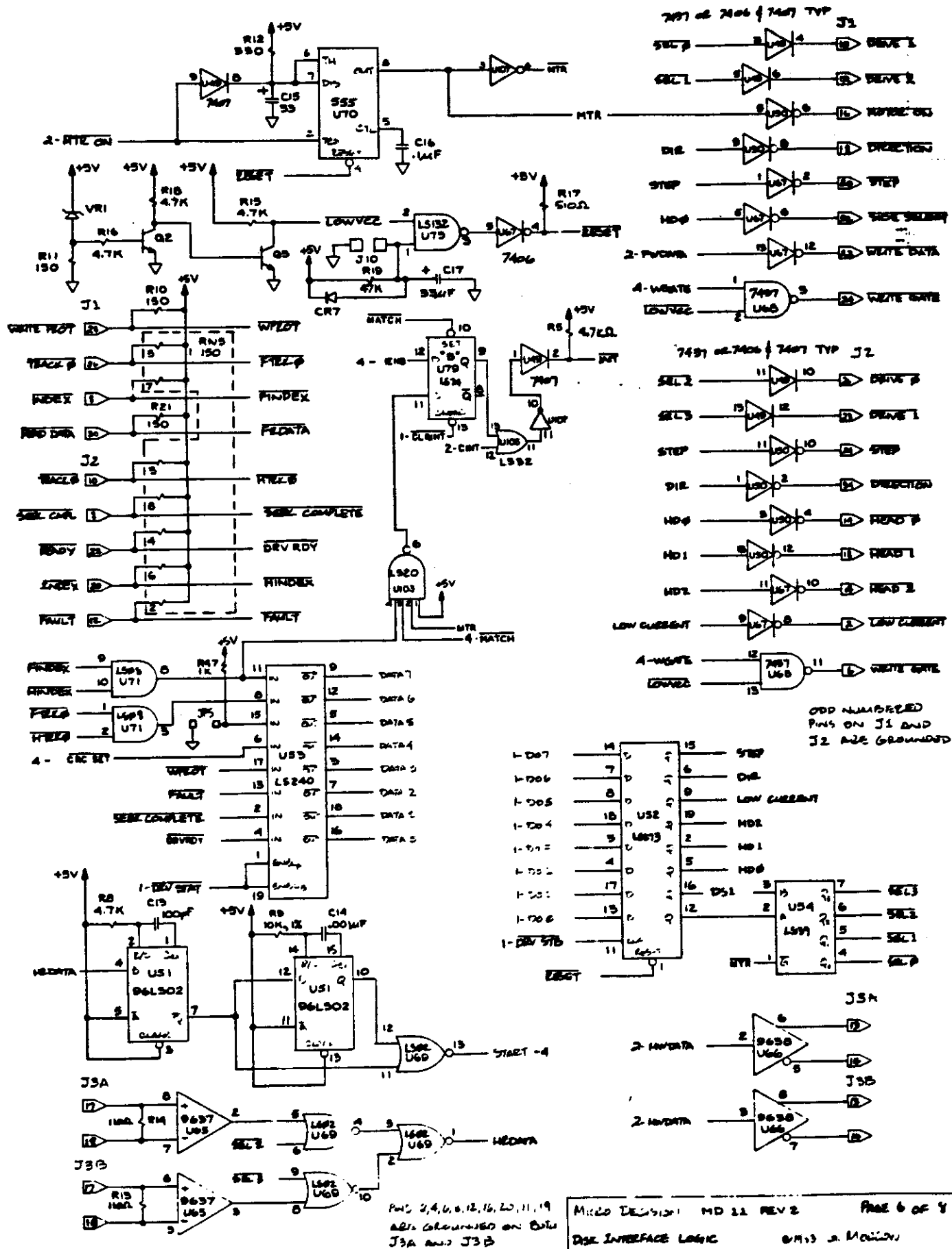
APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



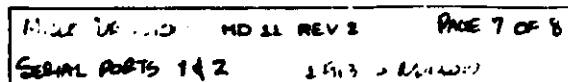
APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



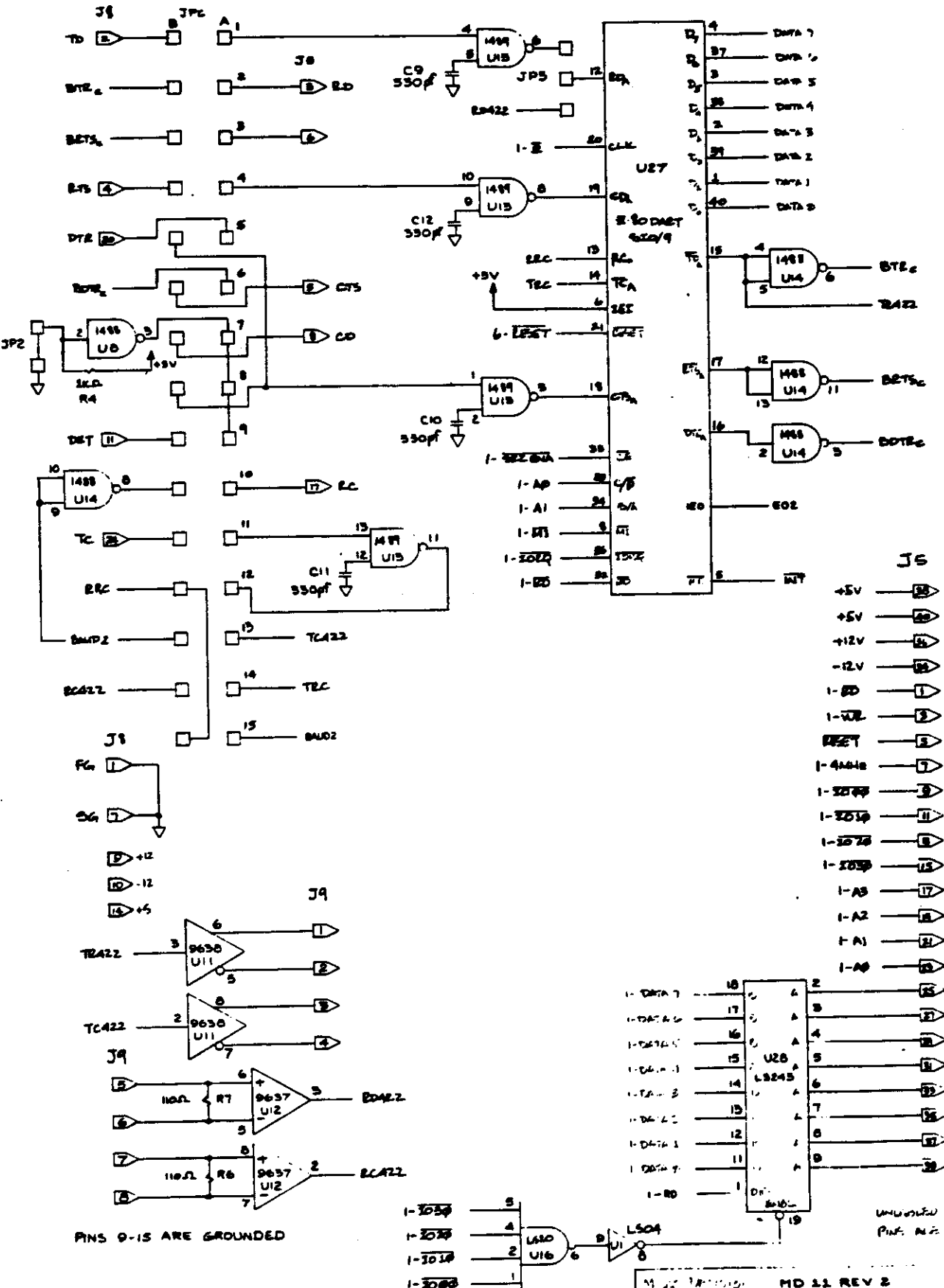
APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



APPENDIX D: MOTHERBOARD SCHEMATIC DIAGRAMS



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MD 11 REV 2
SERIAL PORT 3 & EXPANSION PORT

APPENDIX E. REPLACEMENT PARTS LISTIntegrated CircuitsLocation

126-0237-00	Z80 processor	U2
126-0244-00	Z80 DART	U26
126-0245-00	Z80 SIO	U27
126-0247-00	74S124	U94
126-0250-00	DL8000 delay line	U92
126-0251-00	DDL50 delay line	U95
127-0001-00	2764 BIOS ROM	U29
127-0002-00	74S472/82S147	U19
127-0003-00	82S105 FPLS	U74
127-0004-00	16R8 PAL	U85
127-0005-00	20R4 PAL	U56

Assemblies and Mechanical Parts

225-0031-00	U.S. AC power cord
230-0007-00	Rubber feet
235-0002-00	Plastic hex standoffs for motherboard
400-0028-00	Serial printer/modem cable, 48"
400-0054-00	Parallel printer cable
400-0039-00	Reset switch & wire harness
400-0057-00	34 strand ribbon cable, 14"
400-0058-00	34 strand ribbon cable, 10"
400-0059-00	20 strand ribbon cable, 14"
500-0034-00	CPU motherboard
501-0056-01	110/220 VAC power supply
600-0104-00	Fan with wiring harness
800-0014-00	16 megabyte hard disk (CMI 5619)
800-0015-00	5 megabyte hard disk (Seagate ST506)
800-0021-00	11 megabyte full-height hard disk (CMI 5412)
800-0027-00	11 megabyte half-height hard disk (Shugart SA712)
800-0029-00	Hard disk for MD-34 (40 meg unformatted)
800-0005-00	Shugart SA455 floppy drive
800-0006-00	Qume QT142 floppy drive

Software and Manuals

<u>Program</u>	<u>Diskette(s)</u>	<u>Manual</u>
Personal Pearl	701-0002-00	270-0042-01
CP/M 3.0	701-0026-00 (MD-11)	270-0015-01
	701-0090-00 (MD-16)	"
	701-0095-00 (MD-5)	"
	701-0100-00 (MD-34)	"
MBASIC	701-0039-00	270-0021-00
Correct-It	701-0040-00	270-0089-00
NewWord	701-0056-00	270-0071-00
Backfield	701-0059-00	N/A
SuperCalc	701-0064-00	270-0092-00
MD-HD User's Guide		270-0076-00

