BUFFER INTERLACE CONTROLLER
an option for use with
Varian Data 620/i COMPUTER SYSTEM

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BUFFER INTERLACE CONTROLLER MANUAL

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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

Model 620/i-20 Buffer Interlace Controller (BIC) is a special purpose hardware option available for use with the Varian Data 620/i Computer System. The BIC contains two address registers, a sequence control unit and necessary interface hardware (see figure 1-1). The primary purpose of this option is:

a. to permit 16-18 bit word block transfers at a maximum rate of 202,000 words-per-second, to and from the computer memory and peripheral device controllers connected to the Input/Output (I/O) line. (Typical transfer rate approximately 30,000 words-per-second without the use of this option).

b. to free the Central Processor (CPU) to perform other program functions during block transfers.

Typical uses of the BIC include control of magnetic tape and disc devices, card and paper tape readers and punches, analog-to-digital controllers, etc. A prerequisite for BIC is a 620/i Direct Memory Access option (DMA).

Peripheral devices may then be operated under program control or under direction of the BIC. Up to four BICs may be added to a computer system and a maximum of ten peripheral controllers may be interfaced with each computer system.

Priorities for optional controllers having trap or interrupt capability are established by the order of their placement on the I/O line. The BIC is assigned a priority, however no priority is normally available for peripheral controllers connected to it.

The BIC is packaged on one 620/i etched circuit, plug-in card (DM-126), which is installed in a Model 620/i-01 Memory Expansion/Peripheral Controller Chassis. (See figure 1-2). Compact construction and excellent circuit reliability is achieved through the exclusive use of integrated circuit components.

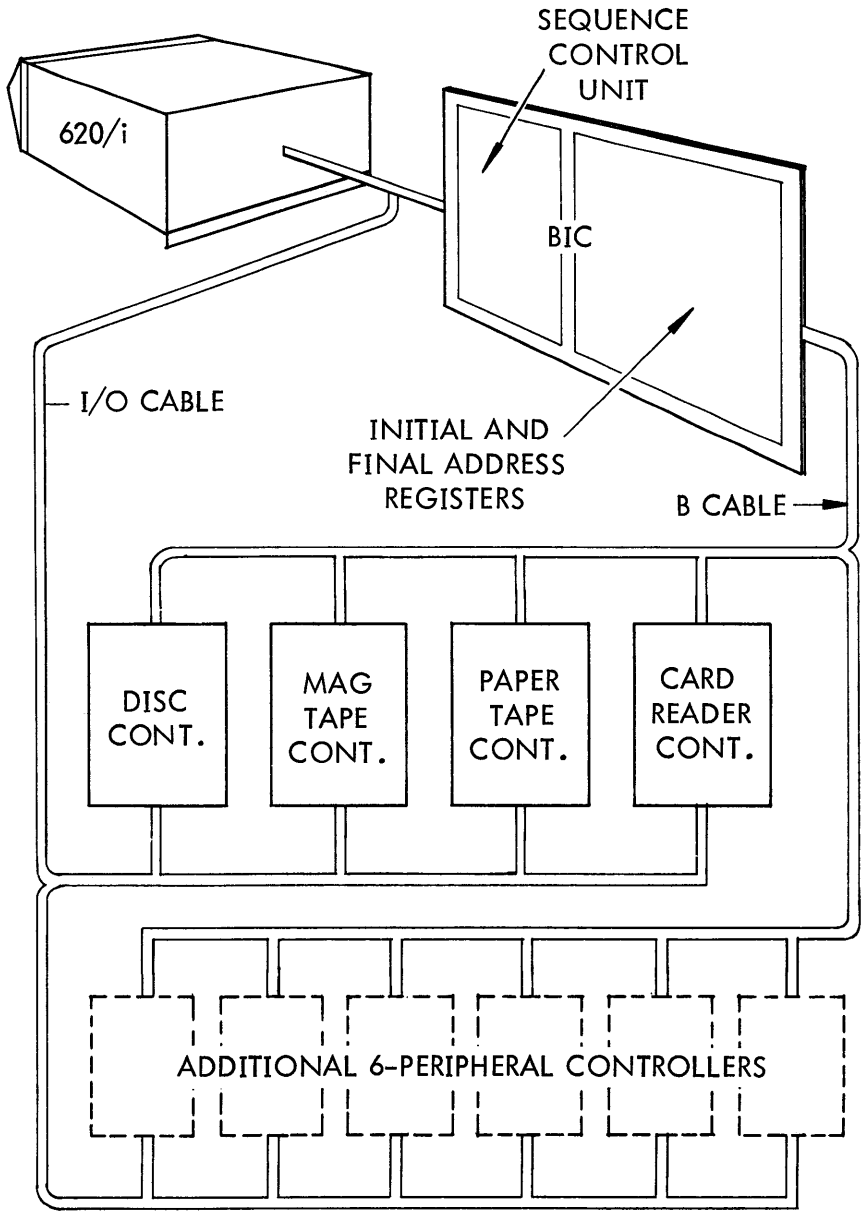


FIGURE 1-1. DATA 620/i CONFIGURATION USING BIC

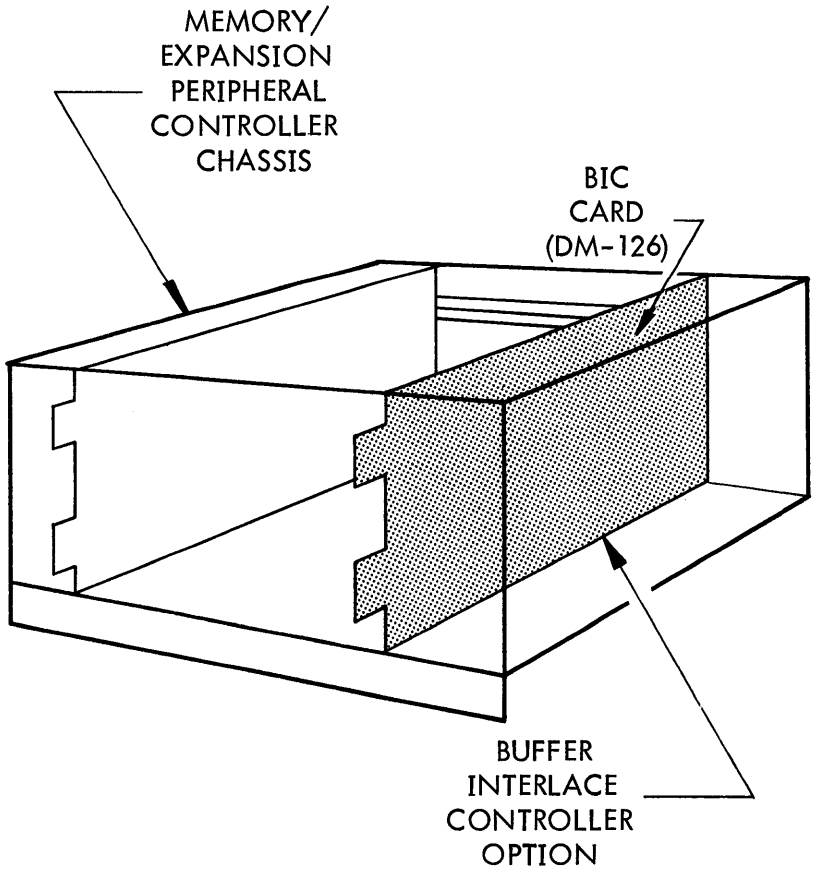


FIGURE 1-2. BIC OPTION INSTALLATION

1.2 SPECIFICATIONS

The following tables list the principal specifications for the BIC:

Table 1-1
BIC Functional Specifications

Specification	Characteristic
Organization	Contains input receivers and output drivers, two 15-bit address registers and a sequence control unit.
Control Capability	Up to ten device controllers
I/O Capability	Two external control commands (EXC) Eleven transfer commands Two sense commands (SEN)
I/O Transfer Rate	Synchronized to peripheral device rate. Maximum 202,000 words-per-second.
I/O Signal Limits (rise/fall)	Minimum 10 nanoseconds - maximum 100 nanoseconds
Logic Levels	
I/O and B cables	Negative logic: True = 0.0 to +0.5 vdc False = +2.5 to +3.7 vdc
Internal	Positive logic: True = +2.5 to +5.0 vdc False = 0.0 to 0.5 vdc

Table 1-2
BIC Physical and Electrical Specifications

Specification	Characteristic
Size	One 7-3/4 inch by 12 inch etched circuit card.
Interconnection	Interface with 620/i I/O cable through backplane connector. Connects to peripheral controllers through B cable.

Table 1-2
BIC Physical and Electrical Specifications (cont'd.)

Specification	Characteristic
Connectors	One 122-terminal card-edge connector (mates with 122-terminal female connector at backplane) and two 44-terminal card-edge connectors (mates with 44-terminal connector (VDM model 620/i-92-8) on B cable).
Input Power Requirements	+5 vdc.
Operational Environment	+10° to 45°C, 10-90% relative humidity

1.3 FUNCTIONAL OPERATION

Control of data transfer by the BIC is established by the program loaded in the 620/i computer. At the appropriate point in the program, the BIC "not busy" status is sensed and a BIC INITIALIZE command is placed on the I/O cable by the computer. This signal prepares the BIC to receive initial and final addresses for the block of data to be transferred. The computer, acting under program control, then senses the "not busy" status of the selected peripheral device, loads the BIC initial and final address registers, places a BIC ACTIVATE ENABLE signal on the I/O cable, and starts the peripheral controller.

At this point the BIC assumes control of the data transaction, freeing the computer operational registers for other use if desired by the program. Data transfer is accomplished, under BIC control, directly between the device controller and the computer memory, via the E bus in the I/O cable. Note that the data being transferred is not routed through the BIC. The BIC counts the data words transferred, and upon determining that the data block transfer is complete, disconnects the peripheral controller, and assumes a "not busy" state until again selected by the computer. Data transfer termination may be requested by the device controller in the event of illegal stops, or in situations where the number of words to be transferred is not previously known by the program. In this event, the action taken by the BIC is the same as that described above.

SECTION 2
PROGRAMMING

2.1 INTRODUCTION

There are no operating controls on the BIC; all its functions are directed by the computer program.

When preparing a program for use with the BIC, the programmer should select and initialize the desired peripheral controller and initialize the BIC. Then the status of both devices should be sensed. After a not busy response is received from both controllers, the BIC address registers should be loaded with the intital and final memory addresses of the block of data to be transferred, a BIC ACTIVATE ENABLE instruction placed on the I/O cable, and the transfer started. Although the program requires loops for use with SENSE instructions and to handle abnormal conditions, transfer of the data block is accomplished by the BIC without further program instructions.

2.2 DESCRIPTION OF COMMANDS

A list of command codes applicable to the BIC is contained in table 2-1.

Table 2-1
Address/Instruction Codes Reserved for BIC

A. External Control		
EXC 020	100020	Active Enable
EXC 021	100021	Initialize
B. Transfer		
ØAR 020	103120	Load Initial Register from A
ØBR 020	103220	Load Initial Register from B
ØME 020	103020	Load Initial Register from Memory
ØAR 021	103121	Load Final Register from A
ØBR 021	103221	Load Final Register from B
ØME 021	103021	Load Final Register from Memory

Table 2-1
Address/Instruction Codes Reserved for BIC (cont'd.)

B. Transfer		
INA 020	102120	Read Initial Register into A
INB 020	102220	Read Initial Register into B
IME 020	102020	Read Initial Register into Memory
CIA 020	102520	Read Initial Register into Cleared A
CIB 020	102620	Read Initial Register into Cleared B
C. Sense		
SEN 020	101020	Sense BIC Not Busy
SEN 021	101021	Sense Abnormal Device Stop

2.3 TYPICAL PROGRAM

The typical program in table 2-2 shows a teletype punch operation under BIC control. Using DAS symbols with corresponding machine language octal codes, the program covers memory locations 1000_8 through 1033_8.

Once the program is loaded, the operator must insert the initial punch buffer address into the A register and the final address into the B register for each run. The program, when started, will initialize the BIC and teletype punch, initiate the transfer, read the contents of the BIC initial register into the A register at completion of the transfer, set the overflow indicator if the termination was abnormal, and then halt. The punch buffer must contain only ASCII characters, the first character must be 0222 (punch on), and the last character must be 0224 (punch off).

Table 2-2.
Sample BIC Teletype Punch Program

Memory Location	Octal Code	Label	Operation	Variable Field	Comments
001000			,ORG	,01000	
001000	100401		,EXC	,0401	INIT-TTY
001001	100021		,EXC	,021	INIT BIC
001002	101020	BICØ	,SEN	,020,BIC1	CK BIC NOT BUSY
001003	001007 R				
001004	005000		,NOP	,	
001005	001000		,JMP	,*-3	
001006	001002 R				
001007	101101	BIC1	,SEN	,0101,BIC2	CK TTY WRITE READY
001010	001014 R				
001011	005000		,NOP	,	
001012	001000		,JMP	,*-3	
001013	001007 R				
001014	103120	BIC2	,OAR	,020	SET BIC I-REG
001015	103221		,OBR	,021	SET BIC F-REG
001016	100101		,EXC	,0101	CONNECT WRITE REG
001017	101020		,SEN	,020,BIC3	CK BIC NOT BUSY
001020	001024 R				
001021	005000		,NOP	,	
001022	001000		,JMP	,*-3	
001023	001017 R				
001024	101021	BIC3	,SEN	,021, BIC5	CK ABN STOP
001025	001031 R				
001026	007400		,ROF	,	
001027	102520	BIC4	,CIA	,020	INPUT BIC I-REG
001030	000000		,HLT	,	
001031	007401	BIC5	,SOF	,	SET ABN FLAG
001032	001000		,JMP	,BIC4	
001033	001027 R				
	000000		,END	,	

SECTION 3
INSTALLATION

3.1 GENERAL

Installation of the Buffer Interlace Controller option is normally accomplished by Varian Data Machines Customer Service Engineers. Logic digrams, assembly layout and wiring information are provided at the time of purchase. The following installation data is provided for planning information.

3.2 PRE-INSTALLATION REQUIREMENTS

Prior to installation of the BIC, proper operation of the computer should be assured through use of the diagnostic test routines described in Chapter 9 of the 620/i Maintenance Manual. A model 620/i-01 Memory Expansion/Peripheral Controller chassis must be installed in close proximity to the computer and connected to the I/O cable by means of an I/O extender cable (Varian Model 620/i-92-1). This cable is available in lengths up to 20 feet to facilitate installation of the expansion chassis.

A model 620/i-12 Direct Memory Access option must be installed in slot 21 of the computer main frame prior to installation of the BIC.

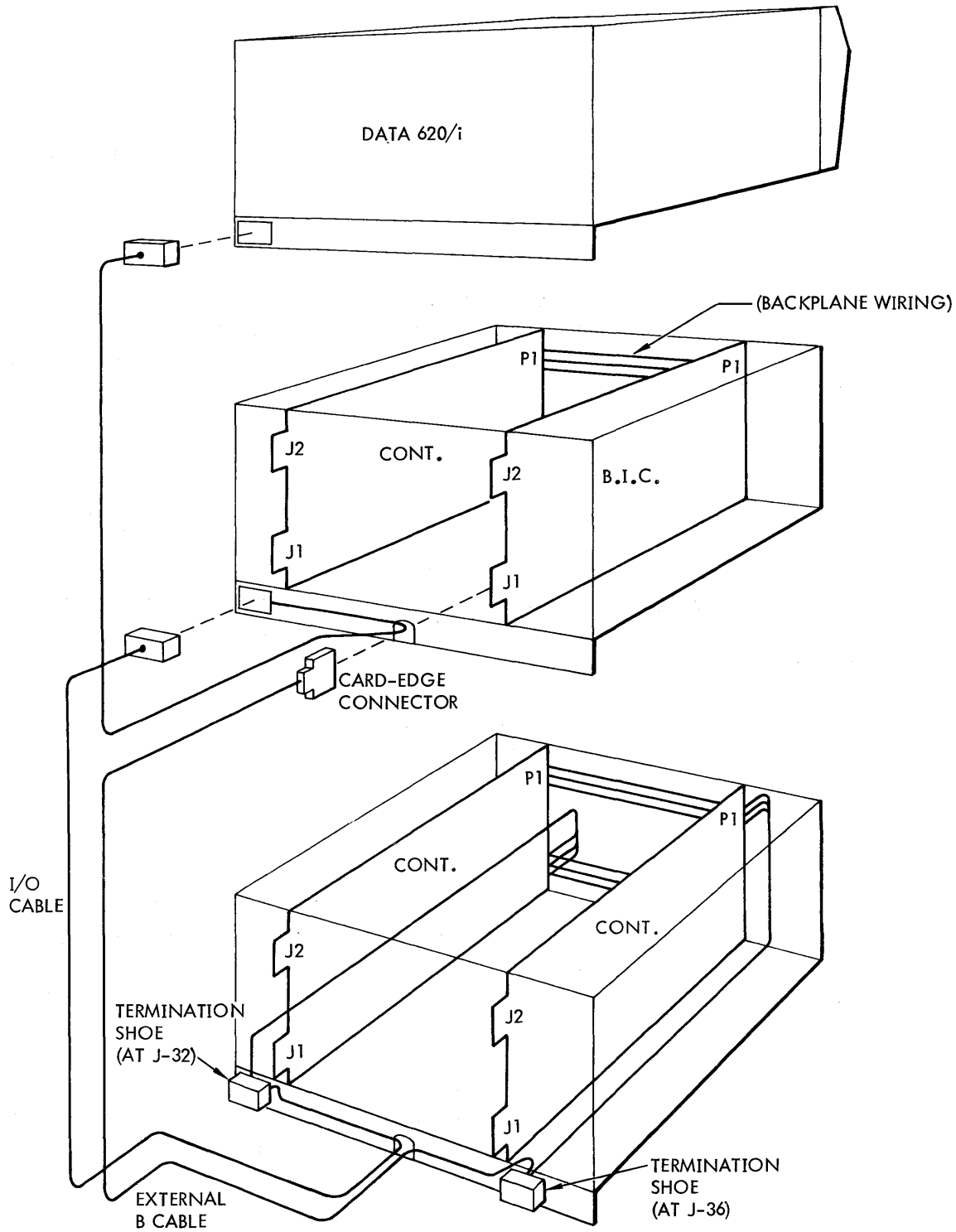
3.3 INSTALLATION

The BIC option (DM-126) is installed in the expansion chassis in a slot designated for peripheral controllers. Installation is accomplished by inserting the card into the mounting guides with the component side of the card on the installer's left when standing at the rear of the expansion chassis. Moderate pressure should be applied to the card forcing the 122-terminal card-edge connector to firmly seat in its mating connector on the expansion chassis backplane.

Care must be taken to insure that equal pressure is applied to both the upper and lower halves of the card during insertion to prevent damage to the backplane connector or to the nylon guides. An etched circuit card puller (Titchener #1731 or similar) is recommended for removing the card from its mounting when required.

3.4 INTERCONNECTION

Connection to the I/O cable, and to peripheral controllers installed in the same expansion chassis, is hardwired through the expansion chassis backplane. Peripheral controllers installed in a different expansion chassis must be connected to the BIC by means of an external B cable. The B cable is fabricated to meet the needs of each installation, using eight twisted pairs which are terminated on one end in a Varian 620/i-92-8 card-edge connector (for connection to the BIC). The other end of the cable is hardwired to the destination expansion chassis. An illustration of such an installation is shown in figure 3-1.



NOTE: B CABLE NOT REQUIRED WHEN BUFFER INTERLACE CONTROLLER IS NOT USED.

Figure 3-1 Typical External B Cable Installation

An external B cable so installed must have each active signal pair terminated as shown in figure 3-2, to prevent noise generation due to reflected signals. A plug/connector designed for use in construction of a termination shoe is available for customer purchase if desired.

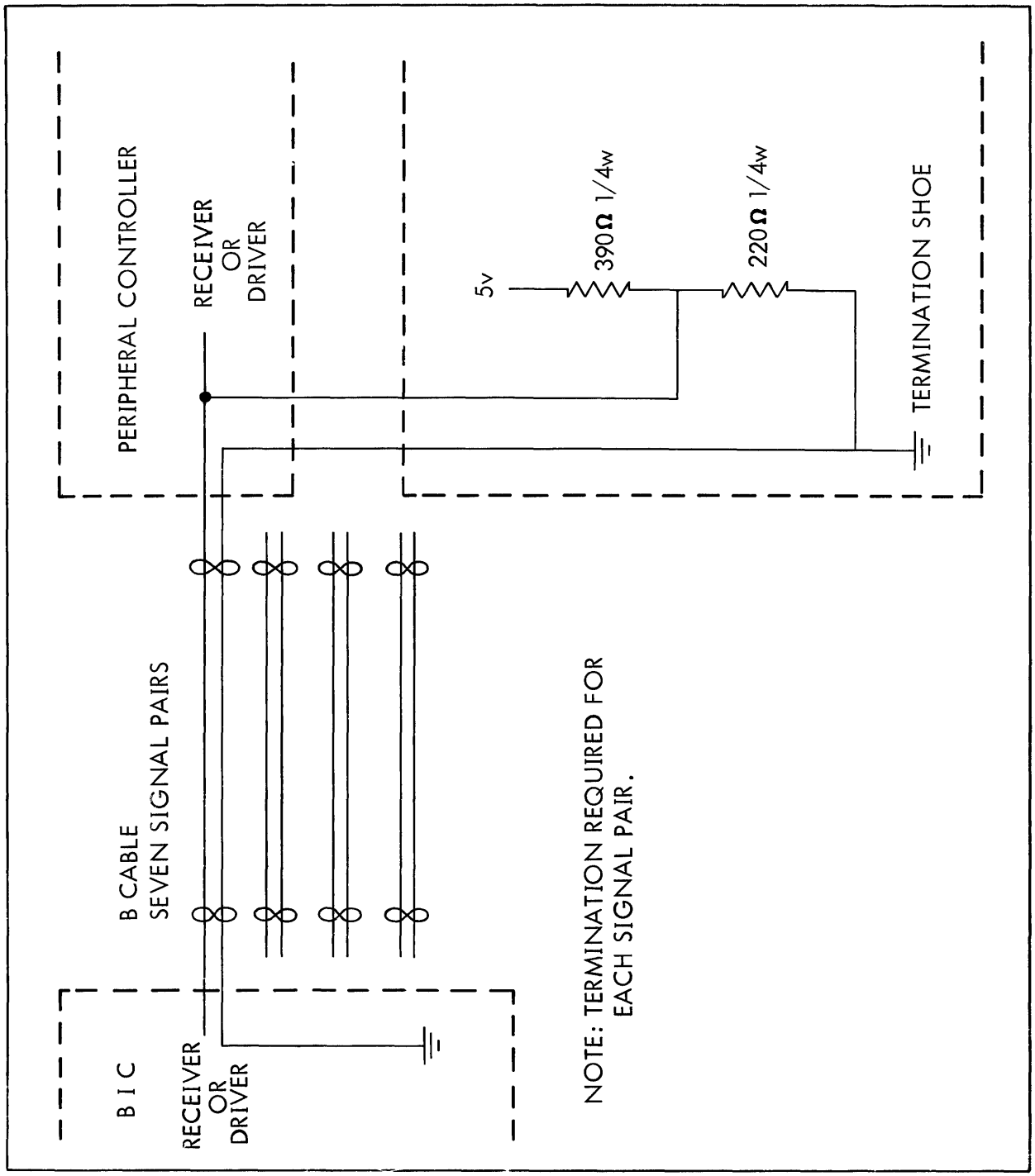


Figure 3-2 Typical Termination for B Cable Pair

SECTION 4
INTERFACE DATA

4.1 GENERAL

All signals enter or leave the BIC through receiver or driver stages which provide buffering between internal circuits and external lines. Details of the interface between the CPU and peripheral controllers connected to the I/O cable are contained in the 620/i Interface Reference Manual, along with general timing information. Logic diagrams, a wire list and an assembly drawing are provided at the time of purchase. The following information is provided as a convenience to the customer, for possible use in design of additional interface connections, and to provide a more complete understanding of the system.

4.2 CONTROL SIGNALS

Input/Output signals exchanged between the central processor and the BIC are summarized in tables 4-1 and 4-2. Signals which are exchanged between the BIC and peripheral device controllers are summarized in tables 4-3 and 4-4.

Table 4-1
I/O Cable Control Signals from Central Processor to BIC

Mnemonic	Name	Description
FRYX-I	Function ready	Indicates the E bus contains address information. The type of address depends upon the state of IUAX-I: When IUAX-I is true, a memory address is on the E bus from the I register of the BIC. When IUAX-I is false, a device address with an associated function code is on the E bus from the central processor.
DRYX-I	Data ready	Indicates the E bus contains a word of data.
IUAX-I	Interrupt acknowledge	Indicates the BIC trap request (TPIX-I or TPØX-I) is acknowledged. The address contained in the I register is placed on the E bus and remains until the trailing edge of FRYX-I.

Table 4-1
I/O Cable Control Signals from Central Processor to BIC (cont'd.)

Mnemonic	Name	Description
IUCX-I	Interrupt clock	A 1.1-MHz clock to provide timing synchronization of the functions within the BIC. This clock is held continuously in a true state when IUAX-I is true.
SYRT-I	System reset	Sets DSTX flip-flop and resets the following flip-flops: TPDX, TCØX, TAØX, LIXX, LFXX, RIXX, and IFMX.

Table 4-2
Control Signals from BIC to Central Processor

Mnemonic	Name	Description
SERX-I	Sense response	Indicates status of a line designated by the device address and function code on the E bus. The BIC provides two responses to sense (SEN) instructions: BIC not busy Abnormal device stop
TPØX-I	Trap output	Indicates BIC is ready to initiate a data transfer from the memory. Signal remains true until completion of transfer sequence when IUAX-I makes a true-to-false transition.
TPIX-I	Trap input	Indicates BIC is ready to initiate a data transfer into memory. Signal remains true until completion of transfer sequence when IUAX-I makes a true-to-false transition.

Table 4-3
B Cable Control Signals from BIC to Peripheral Controller

Mnemonic	Name	Description
DCEX-B	Device connect	A level output from the BIC which indicates the BIC has been activated by the CPU and is ready for connection to the peripheral controller. DCEX-B remains true until CDCX-B is received from the device, indicating the selection operation has been accomplished.
DESX-B	Device stop	A 0.9 to 3.6 microsecond pulse which causes the connected peripheral controller to initiate a stop-and-disconnect sequence. This pulse indicates one of the following signal conditions is present. IEFX+ Indicating the addressed memory block has been filled. BCDX+ Indicating the peripheral controller will not continue to issue transfer requests. INIT+ Indicating the EXC command BIC INITIALIZE has been executed.
TAKX-B	Transfer	A 2.7 microsecond pulse indicating the following conditions: The trap request has been acknowledged by the central processor. The requesting peripheral controller is enabled to execute the transfer operating sequence.

Table 4-4
B Cable Control Signals from Peripheral Controller to BIC.

Mnemonic	Name	Description
CDCX-B	Controlled device connected	A level input indicating the central processor has addressed the peripheral device to be controlled by the BIC. BIC DCEX-B output then makes a true-to-false transition which connects the BIC to the addressed peripheral device until the BIC generates a true DESX-B pulse.
BCDX-B	Buffer Controller deactivate	A level input indicating the connected peripheral device is independently initiating a stop sequence. This causes the BIC to generate a true DESX-B pulse.
TRØX-B	Transfer out	A level input which defines the direction of data transfer. When TRØX-B is true, data is transferred from the central processor to the peripheral device. When TRØX-B is false, data is transferred from the peripheral device to the central processor.
TRQX-B	Transfer request	A level input indicating the connected peripheral device is ready to transfer data. This signal is maintained until the BIC generates TAKX-B and the data transfer operation has been completed.

4.3 BIC ADDRESS ASSIGNMENTS

Two addresses are assigned to each BIC to differentiate between functions directed by the I/O instruction. Addresses 020_8 through 027_8 are reserved for Buffer Interlace Controllers. Address/Instruction Codes listed in table 2-1 have been prepared for the first BIC in a system. If additional BIC's are installed, the addresses shown should be incremented by two for each additional BIC. (i.e., second BIC addresses should be 022 and 023, etc.)

4.4 PRIORITY ASSIGNMENTS

Peripheral controllers capable of initiating interrupt or trap requests are assigned a priority level, to insure that only one such controller at a time will be initiating an automatic request. Priorities are not normally assigned to device controllers; their priority is that of the BIC to which they are connected.

Priorities are determined by controller electrical placement on the I/O bus. This is graphically shown in figures 4-1 and 4-2. It should be noted that although only four controllers are shown, up to ten controllers may be connected to this loop. A complete discussion of the priority system is contained in the Varian Data 620/i Interface Reference Manual.

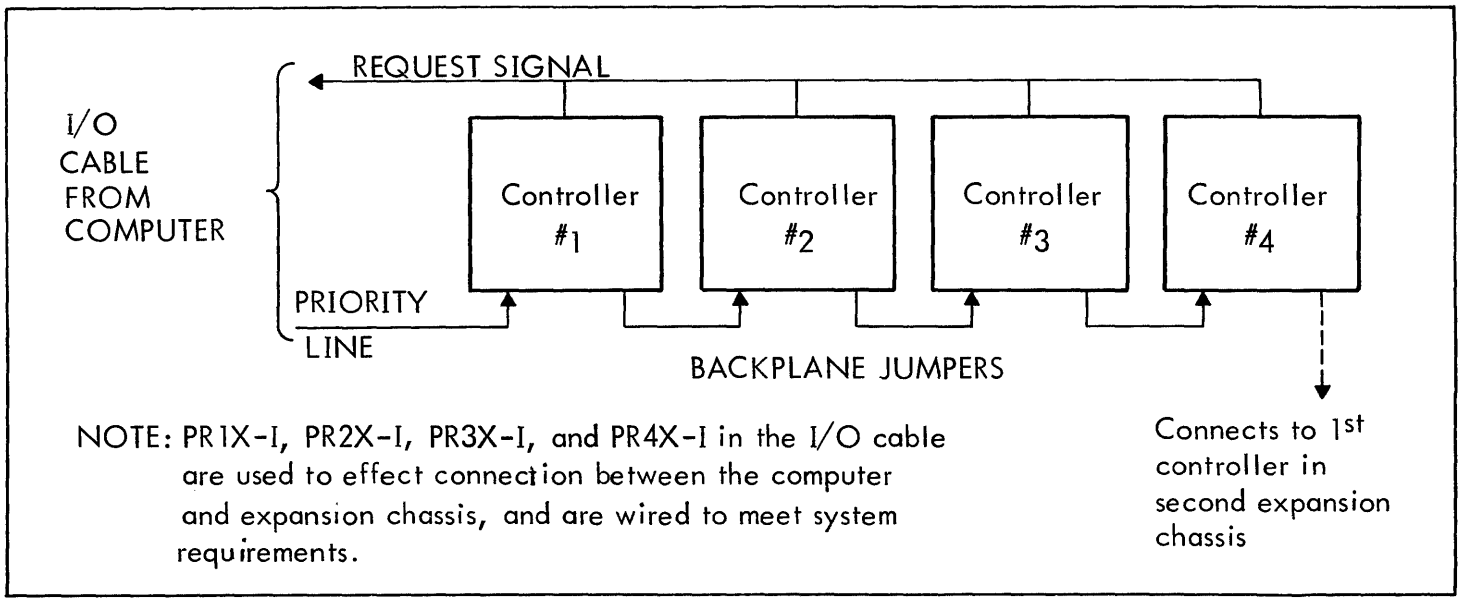


Figure 4-1. Priority scheme for controllers installed in the same expansion chassis.

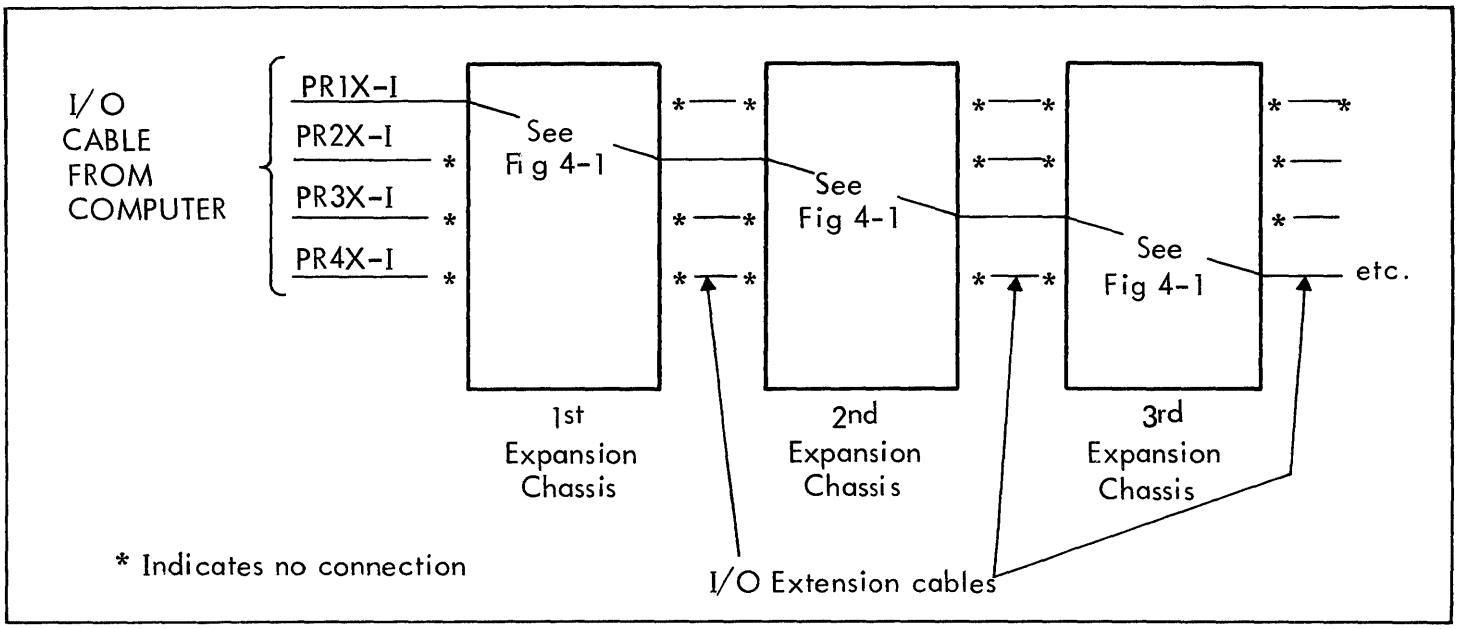


Figure 4-2. Priority Line Connection when more than one expansion chassis is installed.

4.5 PERIPHERAL CONTROLLER INTERFACE

A peripheral controller contains the logic required to enable an I/O device to operate under control of the central processor, or under a Buffer Interlace Controller. Although a device controller may be connected for BIC control, it does not lose its capability to function under the control of standard I/O instructions. Figure 4-3 is a general block diagram showing peripheral device controllers connected to a computer system. Note that some of the device controllers are connected to operate under BIC control. Figure 4-4 shows a BIC/Peripheral Device Controller interconnection with typical interface logic shown in figure 4-5.

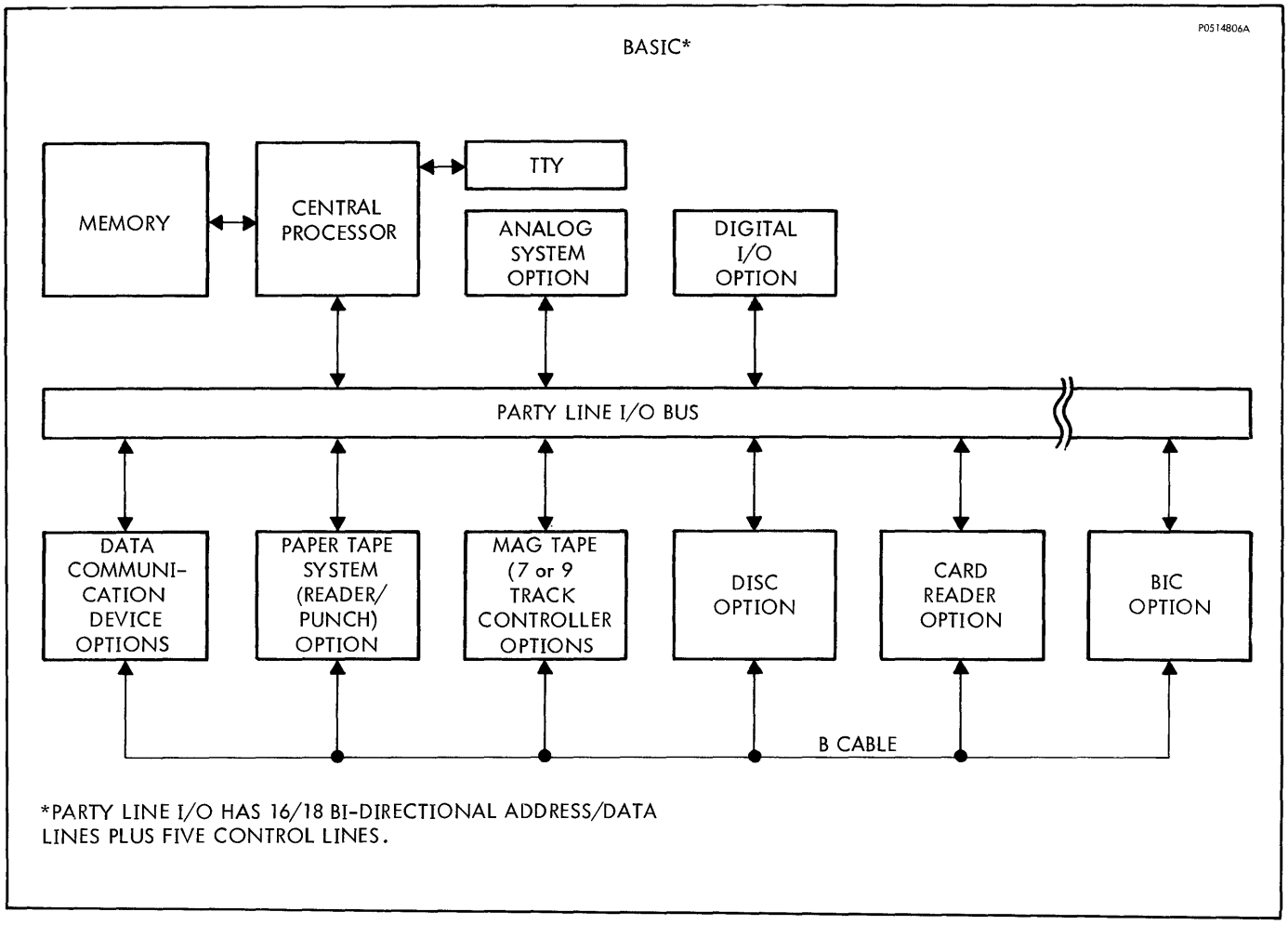


Figure 4-3. DATA 620/i Interface for Peripheral Device Operation With and Without BIC

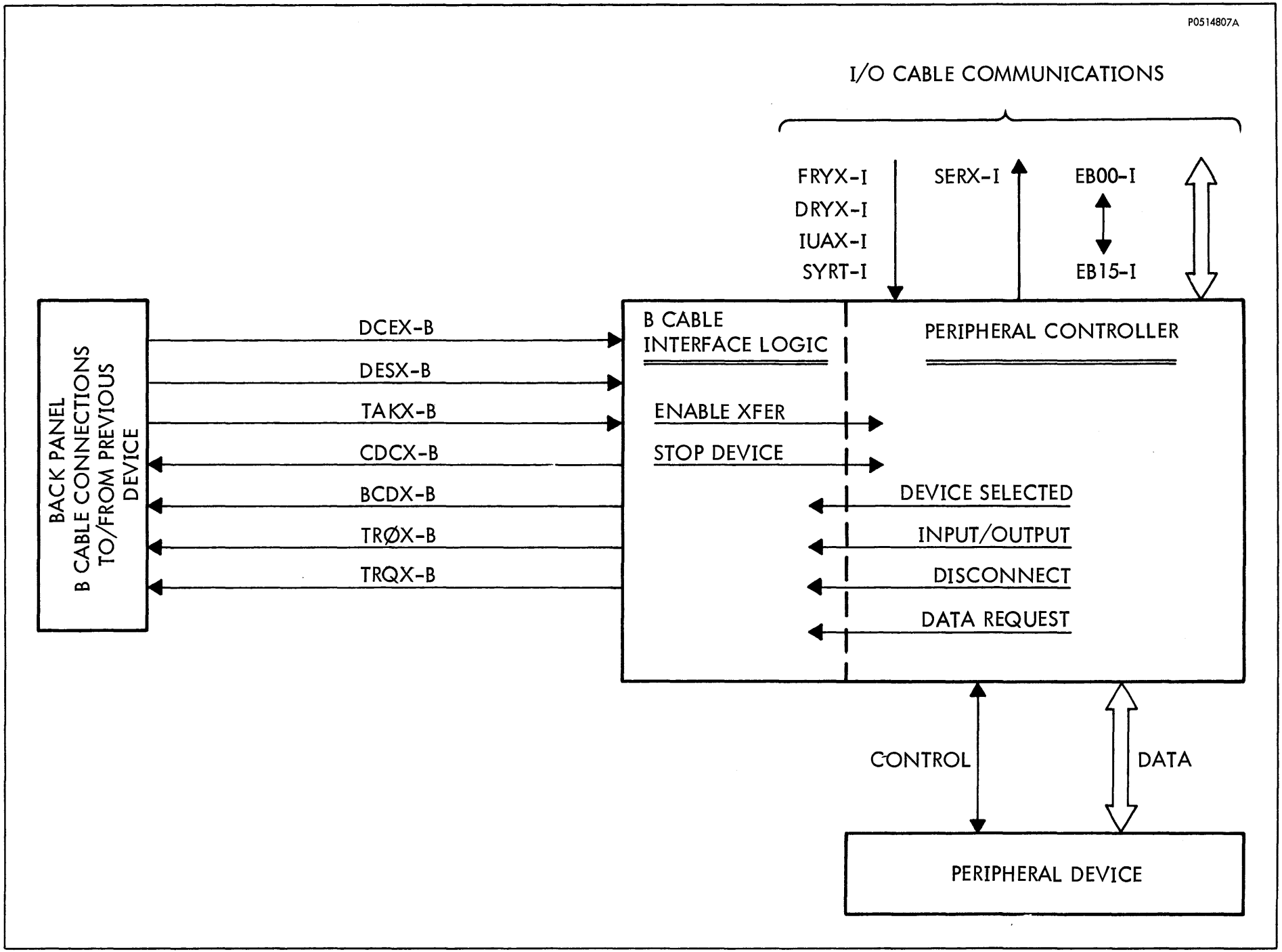


Figure 4-4. BIC/Peripheral Controller Interface

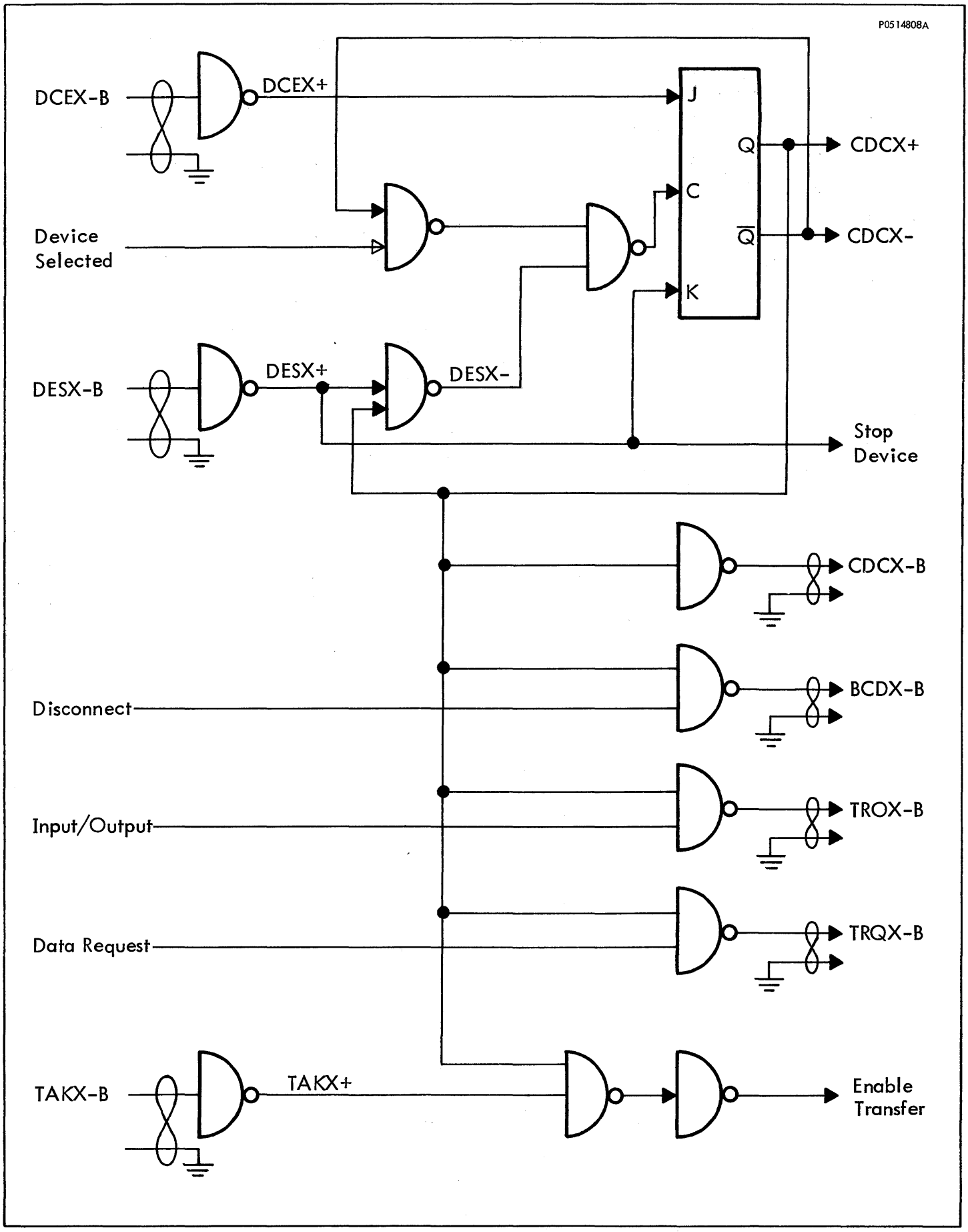


Figure 4-5. Typical B-Cable Interface Logic

4.6 INPUT/OUTPUT TIMING

Figure 4-6 shows the BIC trap timing sequence, as related to signals on the I/O cable and the B cable.

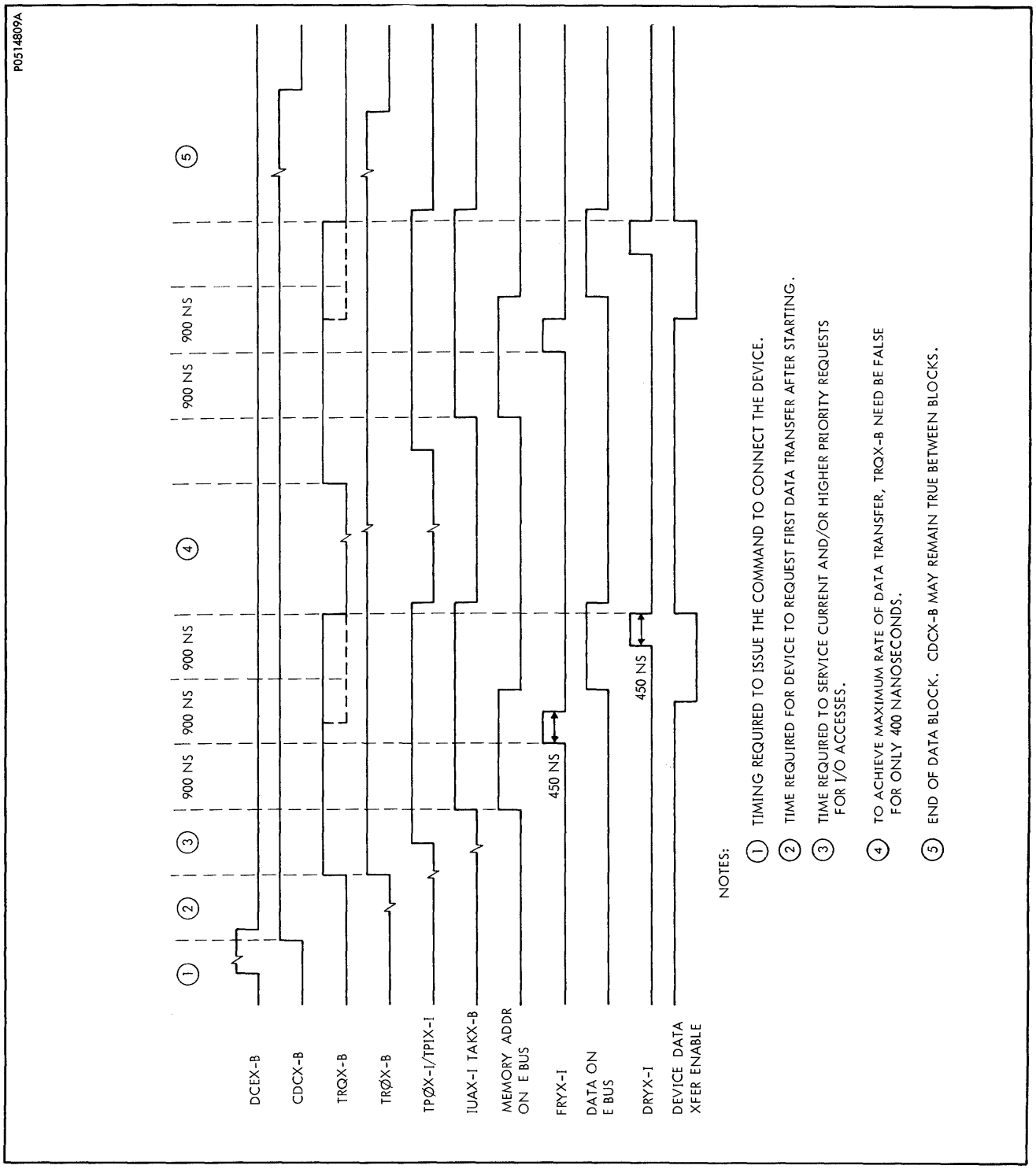


Figure 4-6. BIC Trap Sequence Timing