TELETYPE CONTROLLER

an option for the
Varian Data Machines 620/L
Computer System

Specifications Subject to Change Without Notice

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1.1 SYSTEM OVERVIEW

The **Model 620/L-06-A Teletype Controller** (**TC**) is a mainframe option for the Varian Data Machines 620/L computer system. The TC controls the command and information transfer between the computer and a Varian-modified Teletype (TTY).

One circuit card (part number 44D0013) contains the entire TC. The TC card plugs into the mainframe of the computer. Each TC can control one TTY. If more are required, the additional circuit card plugs into an expansion chassis.

Memory access for the TC can be controlled directly by the central processing unit (CPU) or indirectly through the I/O bus or the buffer interlace controller (BIC). If a system requires more than one TTY, the additional TC is indirectly controlled. A single or the first system TTY/TC is directly controlled by the CPU. A TTY buffer board (assembly 01A0688-000) is required for TTY/TCs 2 through 8 to be indirectly controlled by the CPU through the I/O bus. If the BIC is installed in the system, the CPU is free to perform other program functions during data transfers.

The Varian-modified TTY controlled by the TC can be a model 33 ASR, 35 ASR, or 35 KSR. The ASR models have automatic send and receive facilities and include a paper tape reader and punch; the KSR model uses only keyboard-entered instructions and data.

1.2 FUNCTIONAL DESCRIPTION

The TC is functionally divided into seven sections: input and output registers, input and output timing controls, TC/CPU interface, TC/TTY interface, and BIC control (figure 1-1).

1.2.1 Input Register

The input or read (R) register stores eight bits of data from the TTY. When the CPU generates an input data instruction, the R register places data on the A bus. Note that, in this manual, R refers to a register located in the TC, and not to a similarly designated register in the CPU.

NOTE

In this manual, numbers beginning with a digit other than zero are decimal numbers, and numbers with a leading zero are octal.

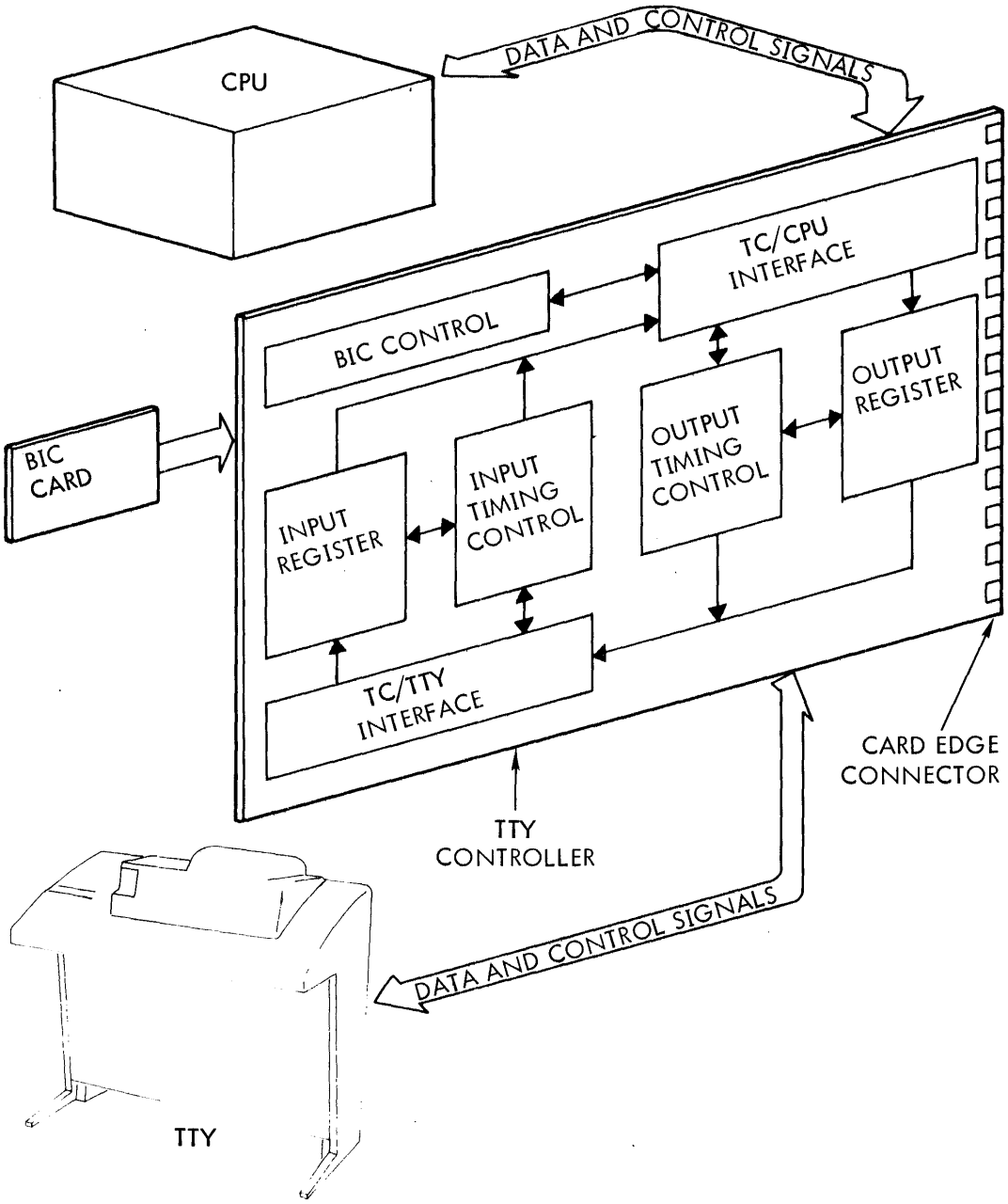

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Figure 1-1. Teletype Controller Functions

1.2.2 Output Register

The output or write (W) register stores eight bits of data from the CPU. When the CPU generates an output data instruction, the W register is loaded from the C bus. Note that, in this manual, W refers to a register located in the TC, and not to a similarly designated register in the CPU.

1.2.3 Input Timing Control

The input timing control section provides event storage, gating, and a 4.55-millisecond clock to regulate three input sequences. These sequences are: start data input, load the R register with input data from the TTY, and transfer data to the CPU.

1.2.4 Output Timing Control

The output timing control section provides event storage, gating, and a 9.1-millisecond clock to regulate two output sequences after the TC is ready to write. These sequences are: load the W register with output data from the CPU and transmit data to the TTY.

1.2.5 TC/CPU Interface

The TC/CPU interface section provides A bus and C bus drivers for the respective R and W registers. This circuit also includes gating logic for control signals to and from the CPU.

1.2.6 TC/TTY Interface

The TC/TTY interface section provides two relays to transmit and receive serial data signals to and from the TTY. This section also includes cabling between the TTY and the TC. Operation between the TC and the TTY is full-duplex, serial, and asynchronous. Appendix A lists the TTY ASCII codes.

1.2.7 BIC Control

The BIC control section is in operation only when the BIC is in the system. The output and input functions to and from the TTY remain unchanged. The TC/CPU interface circuit communicates with the BIC through the BIC control section, rather than with the CPU. This section provides the necessary interface.

1.3 SPECIFICATIONS

The physical, electrical, and operating specifications of the TC are listed in table 1-1.

Table 1-1. Teletype Controller Specifications

Parameter	Description
Organization	Contains input and output registers, timing control circuitry for simultaneous two-way transmission, and CPU/TTY interface logic
Peripheral Device	A Varian-modified TTY model 33 ASR, 35 ASR, or 35 KSR, including cable
Speed	The data rate through the TC is controlled by TTY speed -- ten characters per second (or 100 milliseconds per character) at either random or sustained rate
Modes	Input: from keyboard or paper tape Output: to typewriter or paper tape
Device Address	TC 001 (additional TCs, 002 through 007)
Sense Responses	Ready to read Ready to write
Memory Access Control	By CPU directly By CPU indirectly (requires TTY buffer board) By BIC
Interrupt Types	Write ready and read ready interrupts available to a priority interrupt module (PIM)
Logic Levels	Positive logic True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc

Table 1-1. Teletype Controller Specifications *(continued)*

Parameter	Description
Size	One 7-3/4-by-12-inch (19.7 x 30.3 cm) etched-circuit card
Interconnection	Interfaces with CPU, I/O bus or BIC, and TTY through mainframe backplane connector
Connectors	One 122-terminal card-edge connector (inserts in female connector on mainframe backplane); TTY connects to a three-terminal connector at rear of mainframe
Input Power	+5V dc
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation

SECTION 1
INTRODUCTION

2.1 PHYSICAL DESCRIPTION

The TC is on a 7-3/4-by-12-inch (19.7 x 30.3 cm) etched-circuit card (part number 44D0013). Circuit elements are integrated circuits and discrete components (figure 2-1). All connections to the TC are made through the 122-terminal card-edge connector, which mates with the corresponding backplane connector in the computer chassis.

2.2 SYSTEM LAYOUT AND PLANNING

The TC circuit card is located in card slot 17 of the computer mainframe. The card slots in the mainframe are numbered 1 through 26 from left to right when viewed from the computer front panel. If more than one TC is used in a system, the additional circuit cards are installed in the I/O section of the mainframe or in an expansion chassis and require a special TTY buffer card.

2.3 SYSTEM INTERCONNECTION

The TC circuit card is inserted into the mounting guides of slot 17 with the component side of the card on the installer's left as he faces the rear of the mainframe.

Apply moderate pressure to seat the 122-pin card-edge connector firmly into the mating connector on the chassis backplane. To prevent damage to the backplane connector or to the nylon guides, take care to apply even pressure across the upper and lower halves of the card during insertion. A Titchener 1731 circuit card puller or equivalent is recommended for circuit card removal.

Three wires lead from push-on terminals on pins 112, 113, and 114 of card slot 17 to connector J31 located at the rear of the computer mainframe. The TTY is connected by a 20-foot-long, three-wire cable to connector J31.

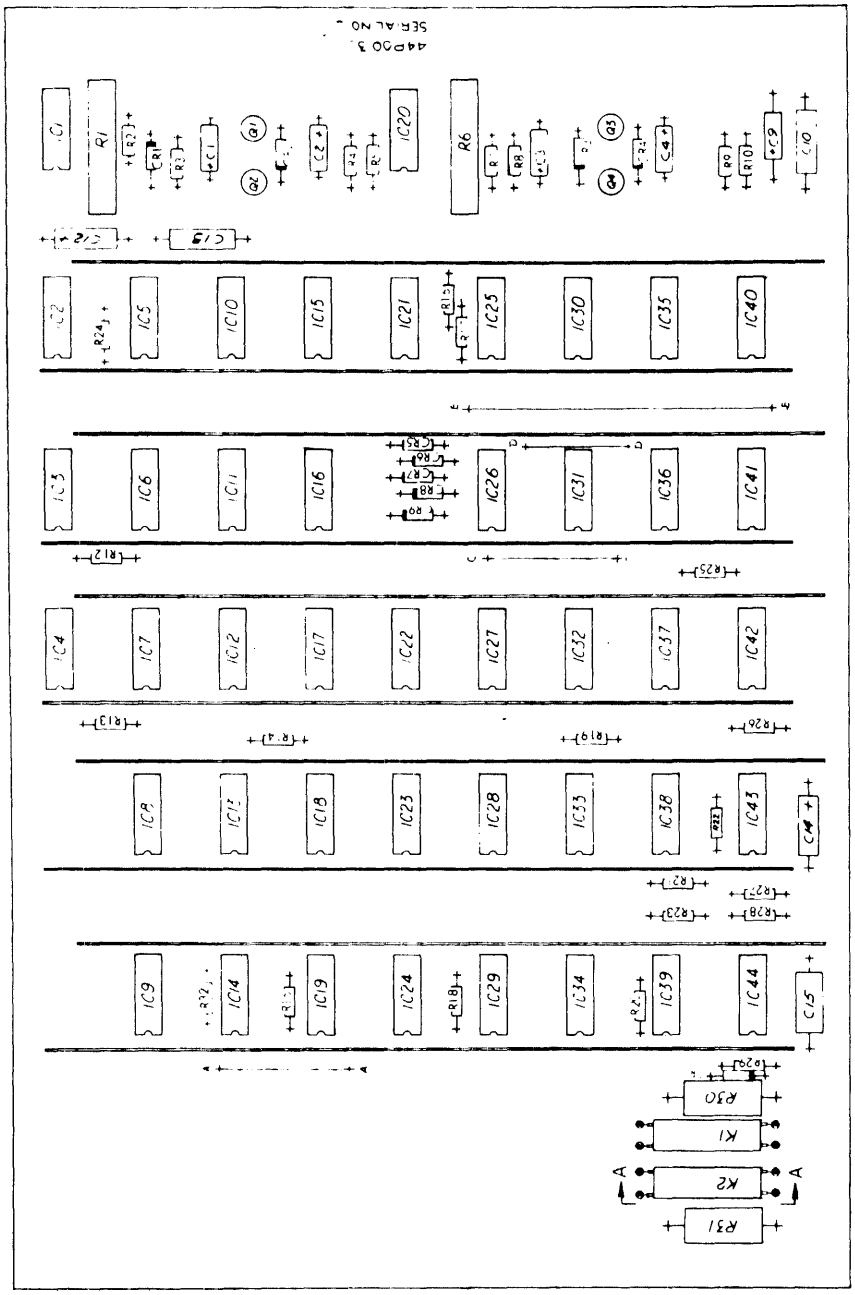

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Figure 2-1. TC Component Layout Assembly

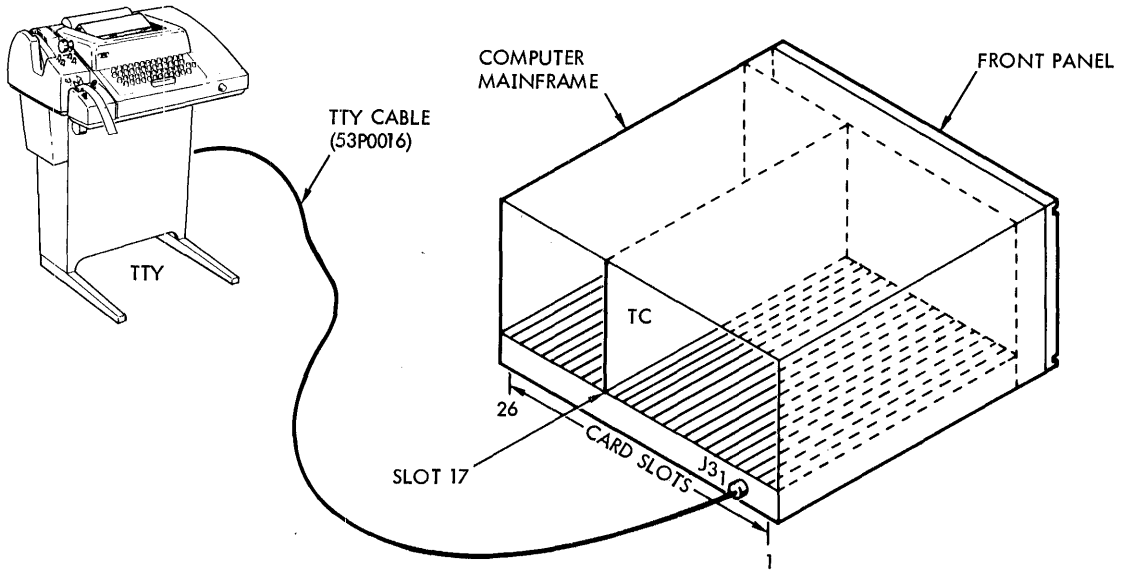

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Figure 2-2. TC Card Location

2.4 SIGNAL INTERFACES

The TC interfaces with the basic computer and a Varian-modified TTY. No other options are required; however, the TC can interface with a BIC and a PIM. This section describes the BIC and PIM, interfaces in a general manner. Refer to the manuals and reference material supplied with the equipment for specific information.

2.4.1 TTY Interface

The TTY units are modified by Varian Data Machines prior to delivery to the customer. Modification of the model 33 ASR teletype consists of the following steps:

a. Setting the teletype for 20-milliampere operation. This includes adding a wire which enables the TTY to supply current for the send and receive data loops to the TC (the TTY becomes the current source for the TC relay drivers).

b. Setting the TTY for full-duplex operation.

c. Disabling the WRU contacts.

d. Disabling parity on the keyboard.

e. Modifying the answer-back drum.

f. Installing the 180801 function lever.

Model 35 modification is similar.

Both models are electrically interfaced and cabled to the TC in almost the same manner, although they are physically quite different in appearance and in their internal operation.

The cable used for the TC/TTY interface for the 33 ASR runs from the S connector plugs in the TTY to J31 at the rear of the CPU. The S connector is labled 2 and located at the right rear, top row, second connector from the right on the TTY unit. The cable is normally 20 feet long with three leads in a cable.

The TTY end of the cable (P2) includes two other wires. Pins 7, 4, and 5 are connected to tie internal TTY leads brought into the S connector plug as part of the TTY wiring. Note that both ends of the cable are keyed to ensure proper mating.

The cable between the model 35 TTY and the TC runs from J31 to a power terminal block (TB) in the TTY. This terminal block is located at the right lower rear of the cabinet behind the TTY printing mechanism.

TC Pin	J31 End	P2 End (-33)	TB End (-35)	Function
113	1	9	Terminal 4	Return
112	2	6	Terminal 5	Receive
114	3	8	Terminal 7	Send

NOTE

The TTY cable is normally installed by Varian Data Machines before customer delivery.

The model 33 TTY requires about 3 amperes of ac power.

The model 35 TTY requires about 6 amperes of ac power.

2.4.1.1 TTY Design

The 33 ASR is designed for light to medium use. Normally, it is the basic computer system input/output device and is the most widely used unit for this purpose. Its full-duplex operating mode allows simultaneous input and output.

The 35 ASR performs the same function as the 33 ASR, but it is designed for heavy, sustained use.

The 35 KSR is used for keyboard send/receive only and lacks the paper tape punch (PTP) and paper tape reader (PTR) capability of the ASR models. The operating characteristics are similar to model 33 keyboard operation. This unit is also designed for heavy, sustained use.

2.4.1.2 TTY INPUT METHODS

TTY input can be via keyboard or the PTR. At the keyboard, the operator types at a random rate not greater than 10 characters per second (cps), the maximum rate for TTY input. Standard eight-level paper tapes are read by the PTR at a random rate or at a rate of 10 cps.

2.4.1.3 TTY OUTPUT METHODS

TTY output is either printed (typed) or punched on paper tape. For the printer or the PTP, the TC sends control codes or data at a random rate or at the maximum output rate of 10 cps. Data are printed, or control functions (such as line feed or carriage return) are performed on the printer. Similarly, control codes regulate the operation of the PTP, and data are punched into eight-level paper tape.

2.4.1.4 TTY SWITCHES

The ON/OFF switch controls the motor. The power supply for TC relay drivers remains on, independent of this switch.

NOTE

> If the TTY motor switch is in the ON position when the computer power switch is off, an open circuit or run command will be transmitted to the teletype. In this case, the teletype motor switch should be placed in the OFF position.

The line switch controls the TC/TTY interface. In the ON-LINE position, the interface is complete, and the TTY is under CPU control. In the OFF-LINE position, the TTY is independent of the TC, and can be used for printing or preparing tapes.

The following switches control the tape and are not on the 35 KSR. The START/STOP/FREE switch on the PTR causes the tape to move in START, to stop in STOP, and to be released from the sprocket drive wheel in FREE. Pressing BSP on the PTP backspaces the tape one character. Pressing REL on the PTP removes pressure from the tape. Pressing LOCK ON locks the punch on (prevents change of punch status). Pressing UNLOCK on the PTP unlocks the punch and enables punch status change by the TC or from the keyboard.

The 35 ASR mode switch mechanism enables the following operating modes.

Position	Keyboard	Reader	Printer	Punch
K	On line	Disabled	On line	Off line
KT	On line	On line	On line	On line
T	Off line	On line	On line	Off line
TTS	Off line	On line	Disabled	Off line
TTR	Off line	Disabled	Disabled	On line

2.4.1.5 TTY FUNCTION CODES

The TTY receives control codes from the TC that cause it to perform specific functions. These codes are listed below. An enable code must follow a disable code. Codes R, T, Q, and S are not applicable to the 35 KSR.

Code	Bit Format	Function
Control A	10000001	Enable printer
Control D	10000011	Disable printer
Control R	10010010	Enable punch
Control T	10010100	Disable punch
Control Q	10010001	Enable reader
Control S	10010011	Disable reader

2.4.1.6 RELAY ISOLATION

Relays K1 and K2 in the TC perform the actual interface between the TC and the TTY. The relays electrically isolate the two units.

K1, the receiving relay, is driven by the TTY. K2, the sending relay, is driven by the TC. The relays are used to switch approximately 20 milliamperes of current on or off the line. This interface method is called " make-break". Each relay can be said to drive or to be driven by a current loop. When current flows through a relay coil, the relay contacts and the current loop are closed. The line is then in the make condition (also referred to as the mark condition). When no current flows through the relay coil, the relay contacts and the current loop are open. The line is then in the break condition (also referred to as the space condition). The steady state of the loops is the mark condition when both the computer and TTY power are on, and both K1 and K2 are energized. When either the computer or TTY power is off, the steady state of the loops is in the break condition, and neither K1 nor K2 is energized.

Except for the difference in switching control location, the send and receive loops have identical functions. The loops are shown in full-duplex configuration in figure 2-3. The Varian-modified system is full-duplex to provide simultaneous transmission of data in both directions.

The current source for the two loops originates in the TTY and is sometimes referred to as " battery" . The CPU and TC use no loop source current, since they are isolated by the K1 and K2 relay contacts. Typical current in a Varian-modified TTY interface loop is 20 milliamperes.

This relay-controlled current loop interface method enables the CPU-TC and the TTY to be placed far apart without noise interference, ground loops, etc., affecting the system. Normally, the TTY cable is 20 feet long.

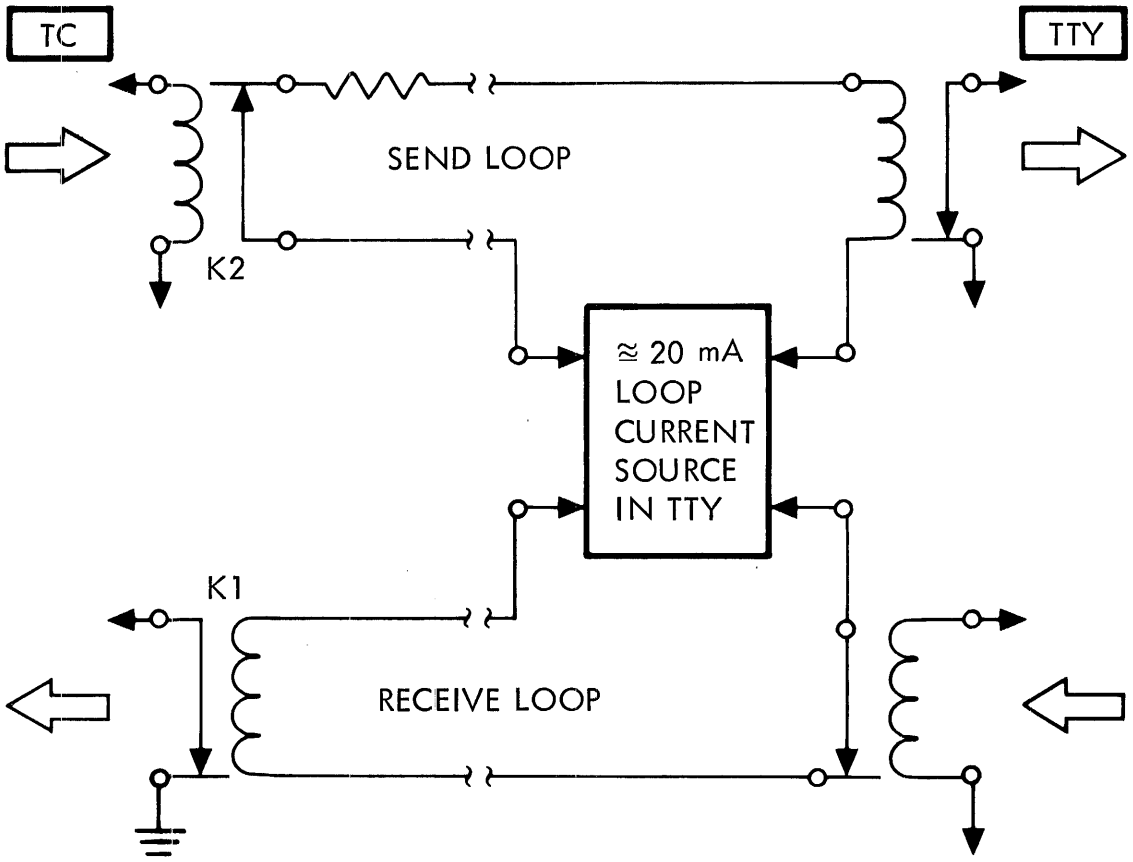
When either the TTY or the TC sends data, K1 or K2 operate (make or break) to conform to the character pattern being sent. The maximum relay switching rate is 9.1 milliseconds per bit. Characters are sent or received serially by the current loop.

2.4.1.7 TTY CHARACTER BIT FORMAT

Each TTY character or command is serial and is divided into 11 periods or bits consisting of one start bit, eight data bits (the eight bit is always mark), and two stop bits (figure 2-4).

The bit pattern for the character shown in figure 2-4 is 10101011. The bit length is 9.1 milliseconds and the bit rate is 110 bits per second (bps). The character length is 100 milliseconds, and the character rate is 10 cps. The start bit is always a space = zero bit = no current in loop = loop open. Data bits are either mark or space. A mark = one bit = current in loop = loop closed.

The eighth data bit is always mark. It might be used by the TTY as an even parity bit on an optional basis. The start and stop bits in the character bracket the data bits. This simplifies the design and operation of the TC receiving circuitry.



NOTE: Equivalent, not actual, circuit with two independent current loops for full-duplex operation. The current loops may have a single common current source and return wire. Isolation is achieved by relays.

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Figure 2-3. Relay Isolation for TC/TTY Interface

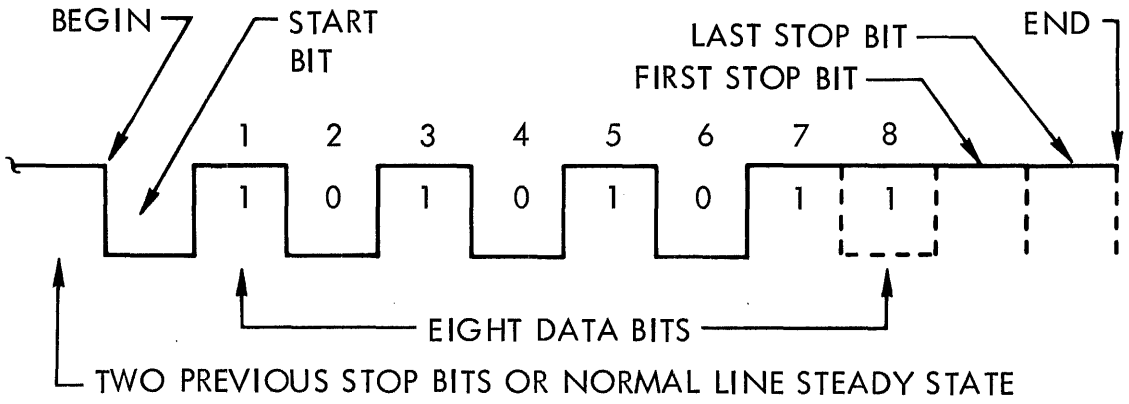

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Figure 2-4. Typical TTY Character

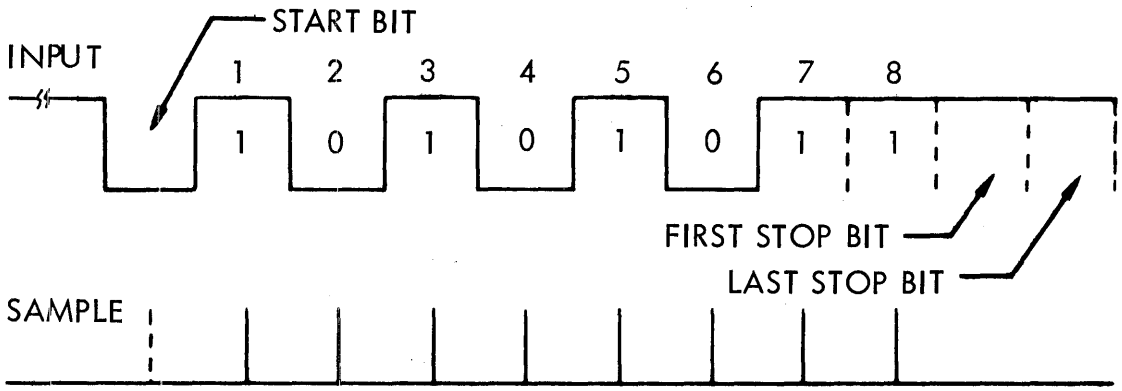

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Figure 2-5. Input Character Sampling

NOTE

The expression " the TTY is running open" means the send loop to the TTY lacks current = steady spacing condition. This occurs if K2 remains open, if the loop current source fails, or if the send loop opens at any point.

2.4.1.8 TTY INPUT CHARACTER

The receiving circuitry synchronizes itself at start-bit time. The TC receiving oscillator (4.55-millisecond clock) normally begins to run at the leading edge of the start bit. Sampling and shifting of the bit pattern then occurs in the center of the start bit and continues at the center of each data bit through the eighth data bit. Normally, each sampled bit is shifted into a register. When the last data bit has been sampled and shifted, the character is ready for transfer to permanent storage (e.g., the computer). The TC enables transfer to the CPU at the beginning of the last stop bit. The stop bit period is used for the transfer of the character to the CPU; therefore, these bits are not sampled. Typically, the TC receiving oscillator stops after the data bits and the first stop bit are transferred and will not start again until a new start bit is received (figure 2-5).

To keep the receiving unit synchronized with the sending TTY, the receiving oscillator or equivalent timing circuit must stop and restart when the start bit for the next character occurs. If the sending device outputs a new start bit before the receiving oscillator has time to stop and recover, the two units are out of synchronization and erroneous data result. The next new character start bit can occur immediately after the stop bit or may not occur for an indefinite time interval. This is typical of asynchronous transmission. The receiving unit must be able to receive and synchronize to new data at any time.

2.4.1.9 TTY OUTPUT CHARACTER

The TTY is assumed ready to receive data at any time. The TC output sequence is as follows.

A character is loaded into the output register. An oscillator circuit starts and sends a start bit. All bit times (start, data, and stop) are equal, and each bit takes one oscillator period. The oscillator enables shifting of the succeeding bits through the output register. The last stage in the register drives the TC send circuitry (K2). The oscillator continues to run until all eight data bits are shifted out.

When the last data bit is sent, the TC obtains a new character from the CPU in preparation for the next character transmission. The oscillator in the TC continues to run during the stop bit. Typically, the TC obtains a new character during the last stop bit. If there are no more output characters, the TC oscillator stops and places a steady one-bit level on the output line. The TTY can then await a new start bit, which occurs on the next output character.

2.4.1.10 ASYNCHRONOUS TRANSMISSION

The previous subsections detail basic TTY input and output. Several points should be stressed.

a. The sending unit transmits at a full or random rate at any time.

b. The receiving unit must accept data at any time at a full or random rate.

c. Receiving unit must resynchronize with every new start bit (every character) to maintain proper synchronization. The oscillator used for this purpose is called a start-stop or gated synchronizable oscillator.

d. The length of the output character must be carefully maintained. The receiving circuit can normally tolerate some distortion (less than 1/2 bit per total character). If the length of output characters is short or long and cannot be corrected, the receiving sampling circuitry can sometimes be adjusted to compensate. The waveforms of figure 2-6 illustrate an example of proper output character length but misadjusted input timing.

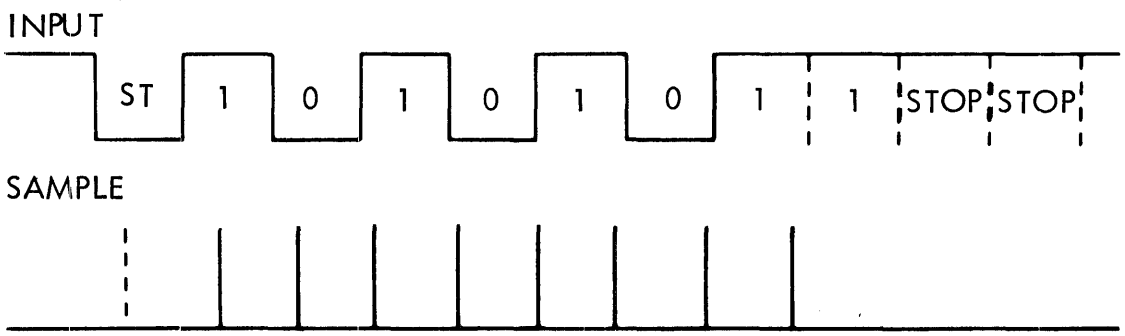

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Figure 2-6. Misadjusted Input Clock

2.4.2 BIC Interface

The TC can be operated under optional BIC control. In this mode of operation, the start and stop addresses of data are placed in the BIC. Command and data transfers are under supervision of the BIC, freeing the computer to do other tasks while data transfer is in progress.

The wiring for the BIC card slot is modified for BIC operation. The modified wiring connects BIC drive signals to the TC. The computer must be equipped with the BIC to use these drive signals.

2.4.3 PIM Interface

The PIM drivers are wired from the TC to the computer PIM logic and generate interrupt requests, saving computer time. The computer must be equipped with the PIM to use these drivers.

2.4.4 Interface Signals

The TC interfaces with the computer and the TTY via the control and data lines listed in table 2-1. A circuit-card pin number follows each signal mnemonic. For definitions of the mnemonics, refer to section 4.

Table 2-1. TC Inputs and Outputs

Input Signals	Output Signals
CB00 - 99,106	AB00 - 28
CB01 - 16,97	AB01 - 26
CB02 - 14,95	AB02 - 32
CB03 - 25	AB03 - 30
CB04 - 18	AB04 - 98
CB05 - 27	AB05 - 96
CB06 - 31	AB06 - 92
CB07 - 23	AB07 - 94
CB08 - 8	CDCX - 11
CB11 - 7	DAXX - 100
CB13 - 102	DIEX - 10
CB14 - 103	DOEX - 15
DCEX - 9	INZX - 110
DESX - 4	IUAA - 21
DRYX - 3	IUBB - 19
EBDX - 107	ONE - 93
EBRX - 29	RRDY - 101
FRYX - 5	RSCX - 91
IUAX - 24	SERX - 2
ONE - 108,109	TROX - 13
SYRT - 6	TRQX - 12
TAKX - 17	TTRX - 112
WCKX - 35	TTSR - 113
	TTXX - 114
	WCKX - 35
	WRDY - 33

SECTION 3
OPERATION

There are no operating controls or indicators on the TC card. Data and control between the TC and TTY are under CPU software control. The SYSTEM RESET switch on the CPU initializes the TC to prepare it to accept CPU instructions and monitor incoming data from the TTY.

The theory of operation is described as a series of sequences that exercise the TC. Refer to logic diagram 91D0005 for the DM113 (section 6). Three digit numbers in parentheses indicate the location of circuit elements on the diagram. The first number locates the sheet, the following letter and number indicate the area on that sheet. Circuit elements that are not on the DM113 are followed by their circuit board number in parentheses.

Signal mnemonic levels referred to in the theory of operation are the levels of the signals at their point of origin or their entry into the TC. Stages of inversion are disregarded for the purpose of clarity. Signals resulting from the outputs of flip-flops are designated FF set and FF reset if they are high when the flip-flop is set or reset, respectively.

4.1 INITIALIZATION

When computer power is first turned on, the TC and CPU circuitry may be in an undefined state. Pressing SYSTEM RESET on the computer control panel initializes the TC (and the computer) to perform under program control. Basically, this enables the TC to monitor the TTY for input characters and to accept output characters from the CPU to the TTY. When initialized, the TC also transmits a steady mark to the TTY by keeping K2 energized.

NOTE

An initialization instruction performs the same function as pressing SYSTEM RESET.

Either SYRT high or CB08 and EXCX high generate INZX high (1A6). INZX high verifies that the following flip-flops are initialized to the state shown.

Set	Reset
RECX	RRDY
WRDY	RDDX
RSCX	DTOX
W00X	DTIX
TR0X	RRCX
	CDCX

As a result, both the 9.1-millisecond clock (1D3) and the 4.55-millisecond clock (1C3) are off.

Note that with the exception of W00X, the R and W register flip-flops are not cleared initially. A low FF reset (W00X) energizes K2, assuring that a mark is on the send loop to the TTY. If TTY power is on, the TTY energizes K1, and the TC receives a steady mark. The TC is then in a line-monitoring state.

4.2 TC/CPU INTERFACE

The CPU commands the TC via the C bus with signals such as FRYX and DRYX (DM112). When any such instruction is issued, the following device address sequence occurs.

DAXX is high while EBDX is high if the proper address (01) is on the C bus. EBDX high enables DAXX high (1D7) during the address setup portion of all instructions. DAXX high enables the instruction-generation gates.

The C bus signals function as follows. CB00 through CB05 enable device address signal DAXX (1D7). CB06 enables the output ready sense response. CB07 enables the input ready sense response. CB08 enables the initialization sequence. CB11 enables the execution sequence. CB13 enables the input instruction sequence. CB14 enables the output instruction sequence.

The CPU can issue several instructions. All are accompanied by the device address, and some are also accompanied by FRYX and DRYX. The input and output timing diagrams (sections 4.4.1 and 4.6.2) illustrate the sequence that results when FRYX and DRYX are present.

Sense write ready (CB06)	No FRYX nor DRYX
Sense read ready (CB07 and CB13)	No FRYX nor DRYX
Execute (initialize) (CB08 and CB11)	FRYX only
Output (load/write register) (CB13)	FRYX and DRYX
Input (read/read register) (CB13)	FRYX and DRYX

If a sense condition is met, SERX goes low. The CPU normally issues a sense instruction before input or output. SERX low is enabled by FF set RRDY high or FF set WRDY high (1B7). These two signals signify that the TC has an input character or can accept an output character, respectively.

When initialized, WRDY sets to enable immediate output under CPU control. RRDY does not set until the TTY has loaded a complete character into the R register.

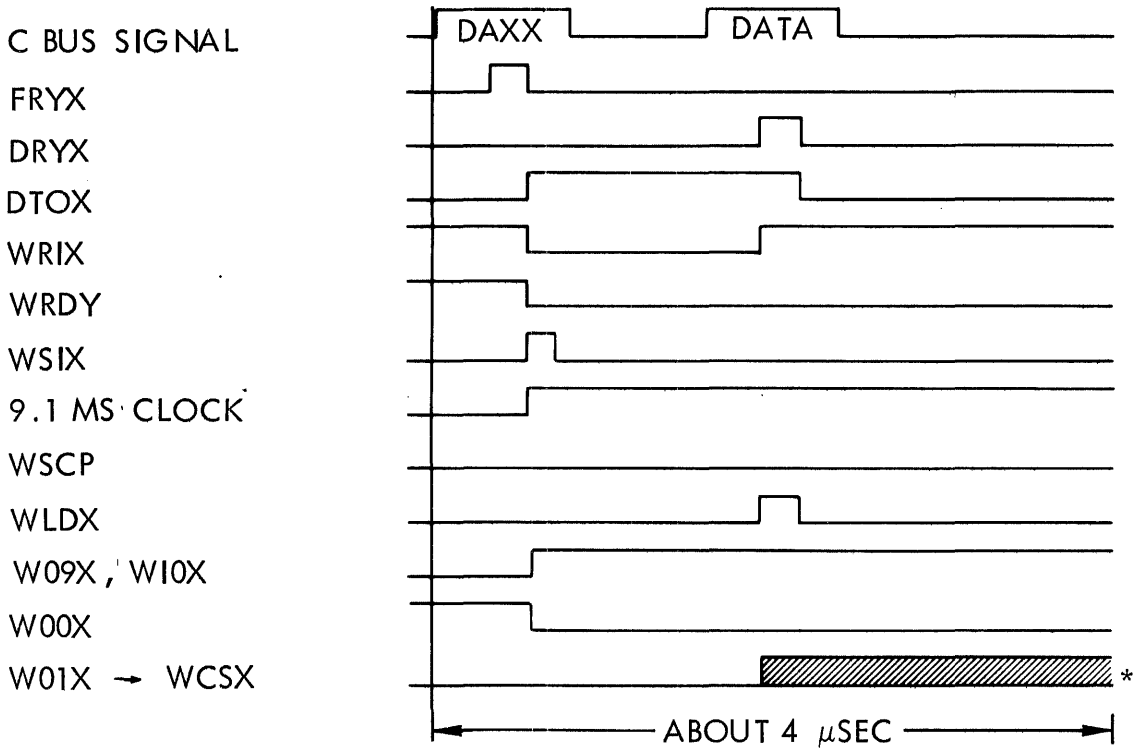
When the CPU issues an output instruction, a FRYX-DRYX sequence sets and resets DTOX. When the CPU issues an input instruction a FRYX-DRYX sequence sets and resets DTIX.

4.3 TC OUTPUT (WRITE)

The TC output circuits include portions of the TC/CPU, output timing control, output register, and portions of the TC/TTY interface. Circuit elements are control flip-flops, a group of gates enabled by the C bus, a 9.1-millisecond oscillator, an 11-bit write register, and an output relay to the TTY with associated drive circuitry. The data and control output waveforms illustrate the loading of output from the CPU to the TTY (figures 4-1 and 4-2). For these waveforms, assume that the TC has been initialized; the CPU has sensed write ready and issued an output command; and the output character is 01010101.

4.3.1 Load Output Register

The CPU issues a sense write buffer ready instruction. If the TC is ready to write, SERX is enabled. The CPU then issues a load/write register instruction, and the following sequence of events occurs (figure 4-1).



*The W register (W01X-W08X)
accepts the C bus bit pattern at WLDX time.

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Figure 4-1. Output from the CPU to the TC Timing

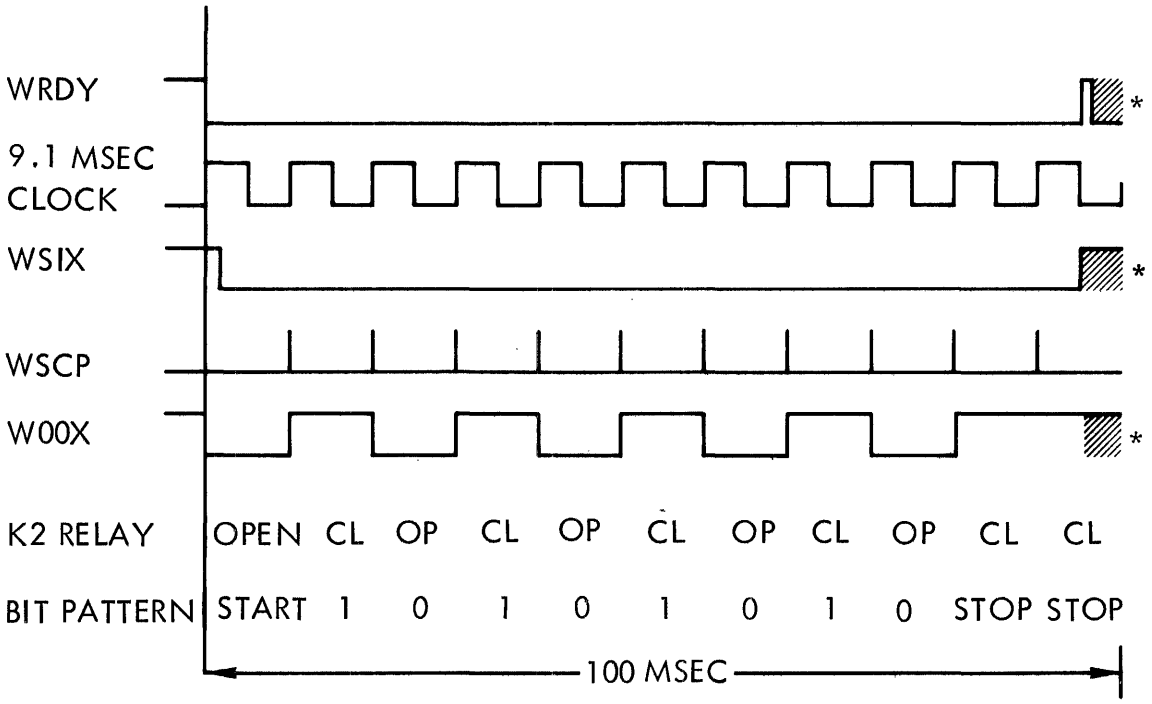
C bus signals enable DAXX high (1D7), and FRYX (1B8) goes high. At the trailing edge of FRYX, DTOX (1C6) sets. WRIX (1C4) goes low, resetting WRDY (1D4) and setting W09X and W10X (2C7). These two W register flip-flops hold the stop bits of the output character. WRIX low also resets the rest of the W register (W00X through W08X). FF reset W00X high deenergizes K2 (2B2). This causes the start bit to be sent to the TTY for 9.1 milliseconds. FF set WRDY low starts the 9.1-millisecond clock (1D3) and sets WSIX (1C2). FF reset WSIX low disables clock signal WSCP (1D1), preventing the W register from shifting, and disables K2. WSIX resets 80 nanoseconds after the 9.1-millisecond clock starts and remains reset until after the next sequence.

DRYX (1B8) going high enables WRIX and WLDX (1C4) to go high. WLDX (2D7), which remains high for 200 nanoseconds, gates the contents of the C bus into W01X through W08X.

The output bit pattern from the CPU on the C bus is loaded in the W register for output under TC timing control. No further computer action is necessary until the next output character. The TC does not require a new output character for 95 to 100 milliseconds. When WSIX is reset, WSCP and K2 are enabled. The TTY detects the start bit and begins its receive sequence. The foregoing sequence takes about 300 nanoseconds.

4.3.2 Output to TTY

The 9.1-millisecond clock (1D3) continues to run. At the end of the first 9.1-millisecond clock period, the following sequence of events occurs (figure 4-2).



*WRDY enables sense response logic. The computer may then respond at any time. The output sequence restarts as above, except actual line output of new character does not begin until the 9.1 msec clock recovers.
WSIX heeps relay K2 energized after W00X is reset and until the 9.1 msec clock restarts.

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Figure 4-2. Output from the TC to the TTY Timing

The first WSCP (80 nanoseconds wide) shifts W register right one place. The least significant bit (W01X) is shifted into W00X (2C2). K2 (2B1) responds to the bit in W00X; the relay energizes for a one and remains deenergized for a zero. WSCP is generated at the start of each clock period. K2 follows the bit pattern originally loaded into the W register. At the start of the tenth clock period, WSCP shifts the last stop bit into W00X. K2 is then energized by the two stop bits, W01X through W10X are reset, and the end-of-character sequence is enabled.

The state of W register flip-flops partially enables the clock input gate for WRDY (1D4). When the clock is midway through its 11th period, the gate is fully enabled and WRDY is set. The TC is thus ready to accept another output character from the CPU. The computer is normally sensing for a write ready (output buffer ready) condition and can now issue another output instruction. Note that a new clock period will not start until the current clock period ends.

NOTE

WRDY becomes true at T = 95.45 milliseconds (of the 100-milliseconds character), which gives the CPU 4.55 milliseconds to load a new output character and maintain a full rate of 100-millisecond per character.

4.3.3 CPU Response

If the CPU responds within 4.55 milliseconds, the load/write register sequence occurs. The 9.1-millisecond clock does not restart until the previous 100-millisecond character period has elapsed; hence, WSIX remains set, and the TC keeps K2 energized, forcing the end of the last stop bit. When the clock recovers, WSIX resets, and the output proceeds as for the previous character.

If the CPU responds after 4.55 milliseconds, the load/write register sequence proceeds as described in the preceding paragraphs. W00X is set, keeping a mark on the line to the TTY through K2. The CPU may not respond; in this case, the above condition remains until a CPU response occurs. In any case, the TTY remains ready to accept a new (start bit) character.

4.4 TC INPUT (READ)

The TC input circuits include portions of the TC/TTY interface, input timing control, input register, and portions of the TC/CPU interface. Circuit elements are control flip-flops, a group of gates to enable the A bus, a 4.55-millisecond oscillator, a 10-bit read register, and an input relay from the TTY. The data and control input waveforms illustrate the loading of input from the TTY to the CPU (figures 4-3, 4-4, and 4-5). For these waveforms, assume that the TC has been initialized, the TTY has just begun to transmit a character, and K1 is beginning to deenergize. During the start bit, the input is controlled by the following sequence (figure 4-3).

The TTY begins to send the start bit of an input character. The start bit deenergizes K1. When K1 drops out, TTRX (2B7) goes low. TTRX low (1C4) sets RDDX, which starts the 4.55-millisecond clock (1C3). This clock enables a delay network causing pin 6 of IC42 (1C2) to go high for 80 nanoseconds. The trailing edge of this pulse sets RRCX (1B3). FF set RRCX high enables RRCP (1B1), which remains low for 80 nanoseconds and sets the R register (R01X through R09X).

The 4.55-millisecond clock continues to run, at the end of its first period (T = 4.55 milliseconds), pin 6 of IC42 goes high for 80 nanoseconds. The trailing edge of this pulse resets RSCX (1C1), causing RSCP (1B1) to go high for 80 nanoseconds. RSCP going low shifts the start bit into R09X (2B7). This shift occurs in the middle of the start bit. At the end of the second clock period (T = 9.1 milliseconds), pin 6 of IC42 again goes high for 80 nanoseconds. The trailing edge of this pulse sets RSCX. The TTY then begins to transmit the first data bit of the character (figure 4-4).

The waveforms shown in figure 4-4 occur after the sequence shown in figure 4-3. These waveforms include the complete character. Input to the CPU is enabled during the last stop bit. This last stop bit is shown extended for clarity.

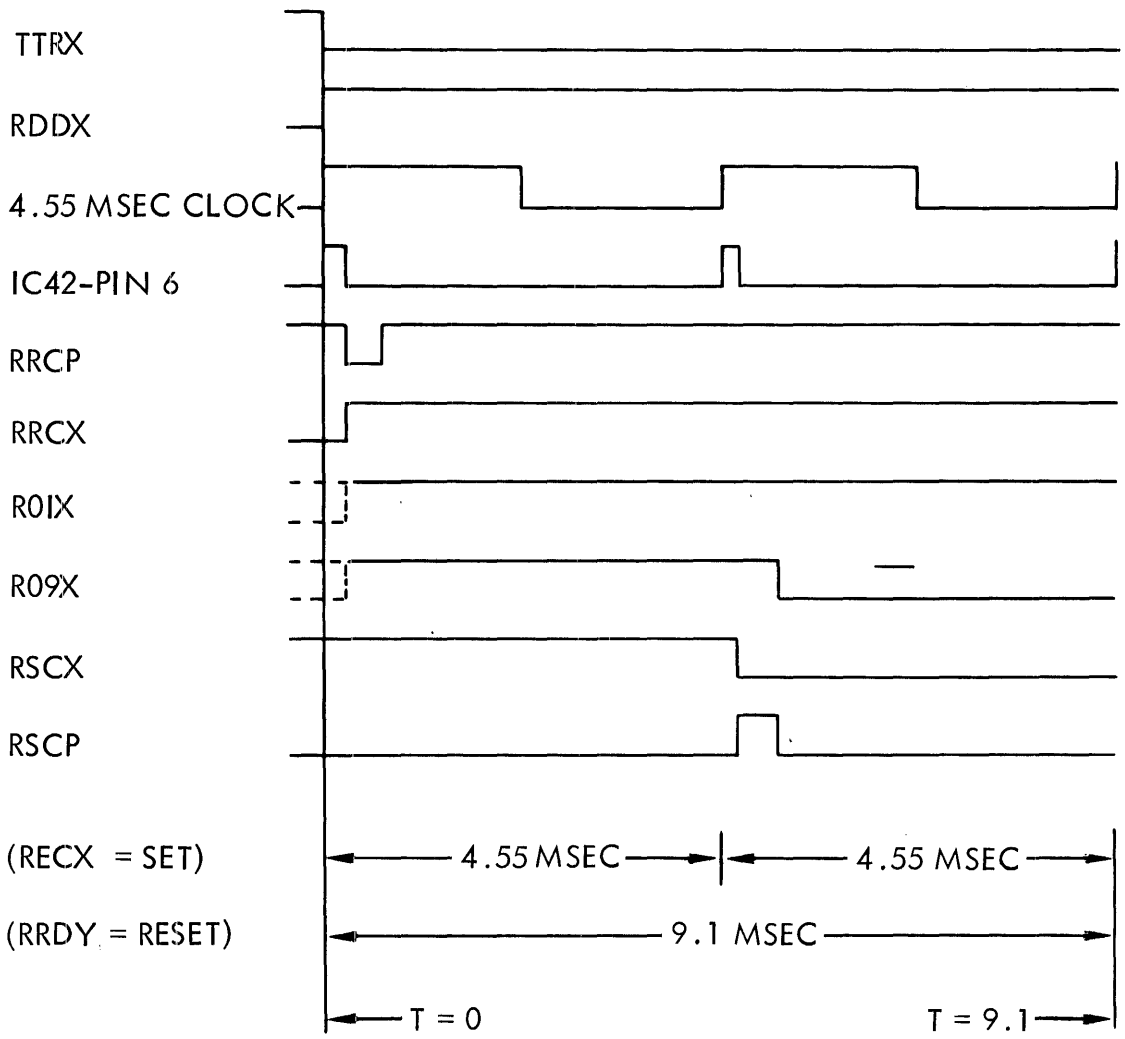

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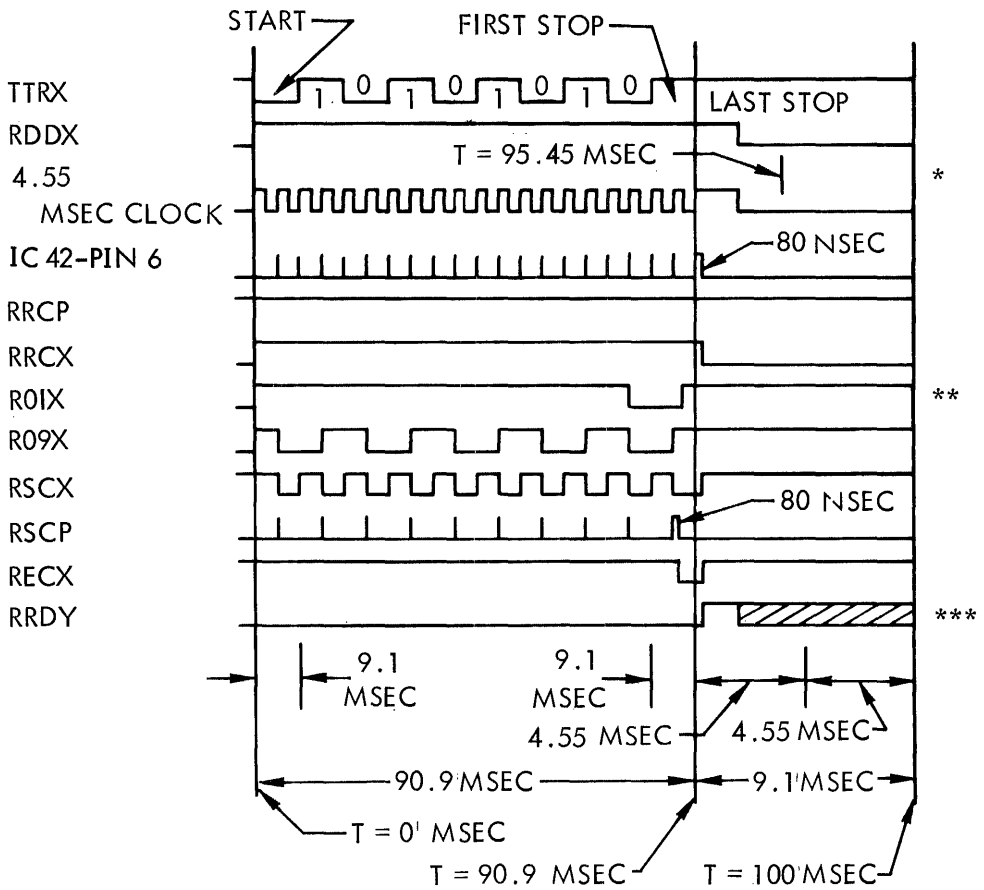
Figure 4-3. Input Start Bit Timing



*The 4.55 msec clock may be restarted and synchronization established any time after T = 95.45 msec.

**R01X is set if lsb is a one bit, reset if lsb is a zero bit.

***RRDY is set (enabling sense response) until the central processor issues an input command. The central processor must respond before a new start bit is transferred through the TC or the input character is lost.

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Figure 4-4. Input from the TTY to the TC Timing

4.4.1 Load Input Register

At the end of the start bit sequence, the TTY transmits the first data bit. The TC has shifted the start bit into R09X and is ready to receive the eight data bits. At the end of the third 4.55-millisecond clock pulse, the signal at pin 6 of IC42 resets RSCX, enabling RSCP, which shifts the first data bit into R09X and the start bit into R08X.

This two-clock period, is repeated for each data bit. RSCX is triggered every 4.55 milliseconds, enabling RSCP in the center of each bit so that sampling and shifting can occur.

When the eighth data bit is accepted, an end-of-character sequence begins in the center of the bit. When the last data bit is shifted into R09X, the start bit resets R01X. Two clock periods later, in the center of the first stop bit, RSCP resets RECX. This pulse also shifts the start bit out of R01X and the first stop bit into R09X. At this time, the complete character is in the R register, the TC is preparing to enable character transfer to the CPU, and the TTY is transmitting the second half of the first stop bit.

At the end of the clock period in which the first stop bit ends (T = 90.9 milliseconds), a signal at pin 6 of IC42 (1C2) and FF reset signal RECX high (1A4) reset RRCX (1B3). RECX is set by FF reset signal RRCX high. FF set RRCX low partially enables reset of RDDX (1C4), which stops the 4.55-millisecond clock. Before RRDX can reset, FF reset RECX high sets RRDY (1C4), enabling a read/read sense response to the CPU. The clock continues to run for one more period. Halfway through this period, RRDX resets, removing the clock start enable.

NOTE

> The 4.55-millisecond clock does not recover until T = 95.45 milliseconds. Prior to this time it cannot be accurately restarted with a new start bit from the TTY. If a new start bit from the TTY occurs before T = 95.45 milliseconds, the resulting out-of-sync condition causes erroneous data sampling and errors.

4.4.2 Input to CPU

At the end of the first stop bit (T = 90.9 milliseconds), RRDY sets to enable a sense-ready-to-read response in the CPU (figure 4-5). The waveforms shown in figure 4-5 occur after the sequence shown in figure 4-4. With these waveforms, assume that data bits of the character have been shifted into the R register, the TC is receiving the last stop bit, and the CPU issues an input instruction. The time from T = 90.9 milliseconds to T = 93.175 milliseconds is shown extended for clarity.

NOTE

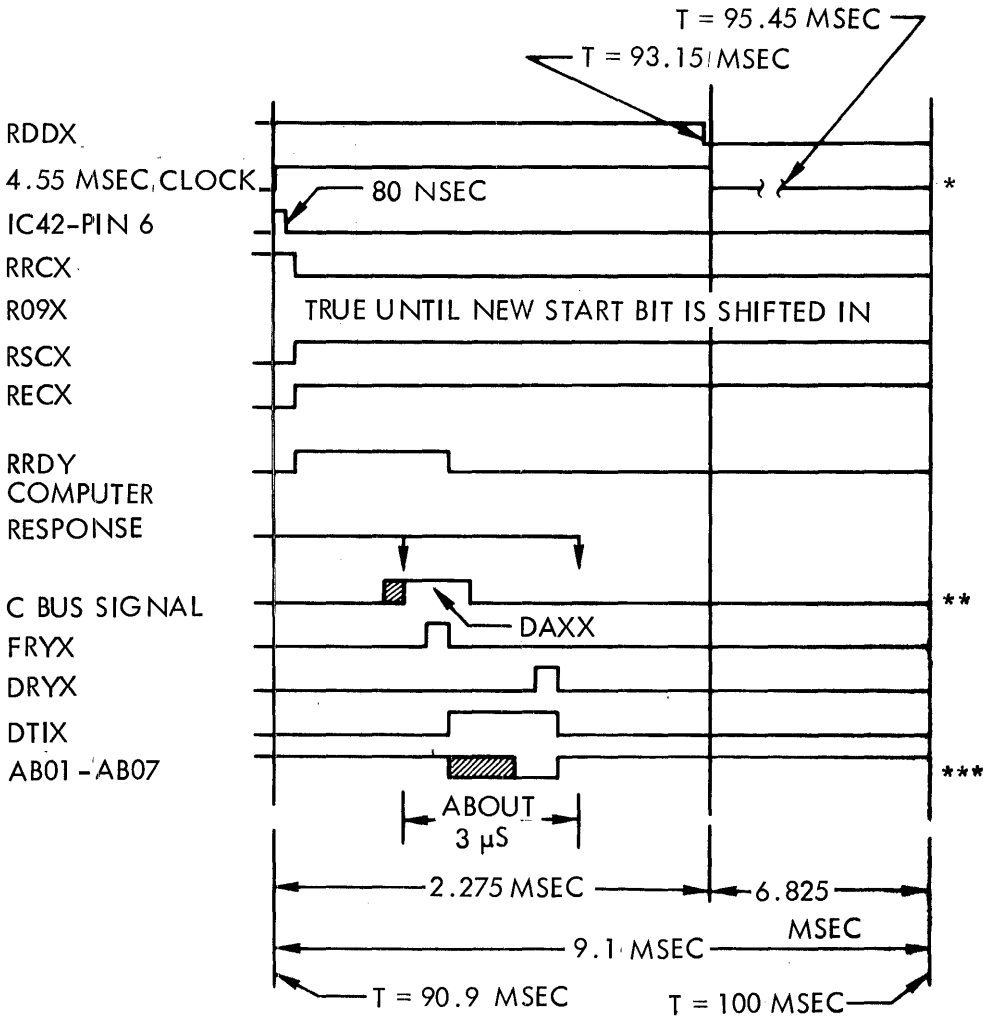
> At a continuous 10 cps (100 milliseconds per character) rate, the CPU has less than 9.1 milliseconds to read the character out of the R register. If an input data instruction is not issued before 9.1 milliseconds, the character is lost. The start bit of the next character resets RRDY, preparing the R register for a new character.

The CPU issues an input data instruction after sensing the read-ready condition. With DAXX high (1D7) at the end of FRYX (1B8), DTIX (1C6) sets, and RRDY (1C4) resets. The CPU causes EBRX (2B7) to go high. EBRX high and FF set DTIX high enable the A bus gates driven by the R register flip-flops. The character is on the A bus lines to the CPU when DRYX (1B8) occurs. When DRYX goes low, DTIX resets, and input to the CPU is complete.

Character transfer to the CPU must occur before the start bit of a new character to avoid losing the character. The TC waits for a new start bit. Until a new start bit occurs, K1 remains energized, and the 4.55-millisecond clock and RDDX remain off.

4.5 BIC CONTROL

Optionally, the TC can be operated under BIC control. In this mode of operation, the start and stop addresses of data are placed in the BIC. Instruction and data transfer is under supervision of the BIC. The information transfer between the TC and the TTY is unchanged. The information transfer between the TC and the CPU is changed (from the previous descriptions) as follows.



*New start bit can occur any time after T = 95.45 msec, and synchronization with the teletype is maintained. Data transfer to the central processor must occur before a new start bit or the character in the receive register is lost. If a new start bit occurs before T = 95.45, clock synchronization with the teletype will be lost.

** C bus signals are for device address (normally device 01).

*** The AB00-AB07 lines are enabled by EBRX from the central processor.

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Figure 4-5. Input from the TC to the CPU Timing

For output to the TC, the computer with BIC sets TR0X (3B6) and CDCX (3D6). This enables CDCX low and TR0X to the BIC. When WRDY is set, TRQX to the BIC (3B5) is enabled. The BIC responds by generating TAKX low (3D6), which enables DOEX low (3C5). DOEX low (1B6) sets DTOX, and the output character is taken from the C bus. Output to the TTY then proceeds under TC control.

For input to the CPU, the computer with BIC sets CDCX and resets TR0X. This enables CDCX to the BIC. When RRDY sets, TRQX to the BIC (3B5) is enabled. The BIC responds by generating TAKX low (3D6), which enables DIEX low (3C5). DIEX low (1C7) sets DTIX, and the input character is transferred to the A bus.

4.6 MNEMONICS

The mnemonics used in the TC are listed alphabetically in table 4-1. A brief description of each signal's function is given. Except where noted, the source column list the location on drawing 91D0005 at which the signal originates.

Table 4-1. Mnemonic Definitions

Mnemonic	Source	Description
AB00 to AB07	2B	Data or instruction from the TTY to the CPU
CB00 to CB08 CB11 CB13 to CB14	All	Data or instruction from the CPU to the TTY
CDCX	3D5	Stores the TC/BIC connection

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DAXX	1D7	Decodes the device address from the C bus
DCEX	3D8	Enables BIC control of the TC
DESX	3C8	Disables TC when controlled by BIC
DIEX	3C5	Sets the DTIX flip-flop under BIC control
DOEX	3C5	Sets the DTOX flip-flop under BIC control
DRYX	1B8	Gates data in and out of the TC
DTIX	1D6	Stores an input instruction from the CPU and gates data to the A bus
DTOX	1C5	Stores an output instruction from the CPU
EBDX	1D8	Enables the device address signal
EBRX	2B7	Gates the contents of the R register to the A bus
EXCX	1A6	Enables initialization and BIC control
FRYX	1B8	Enables data transfers to and from the TC
INZX	1A5	Initializes the TC flip-flops
IUAA	1D3	Generates interrupt requests in the PIM during a write ready signal

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
IUAX	1C8	Interrupt acknowledgement
IUBB	1B1	Generates interrupt requests in the PIM during a read ready signal
RDDX	1B4	Stores the start of a TTY transmittal and enables input timing
RECX	1A4	Stores the end of a TTY character transmittal
RRCP	1B1	Sets the R register flip-flops prior to input
RRCX	1B2	Stores the activation of the R register
RRDY	1B2	Indicates that the R register is loaded
RSCP	1B1	Controls the shifting of input characters into the R register
RSCX	1C1	Stores the end of each 4.55-millisecond clock and generates read shift clock pulses
R01X to R09X	2	R register flip-flops that store input data or control information
SERX	1B7	Indicates that the TC is ready to respond to CPU input or output instructions
TAKX	3D6	Indicates that the BIC controls the TC
TROX	3C5	Stores the need for CPU input or output under BIC control

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
TRQX	3B5	Trap request generated under BIC control by either RRDY or WRDY
TTRX	2B7	TTY output
TTSR	2B8	Return for TTY input and output
TTXX	2B1	Input to TTY
WCKX	1D2	Output of 9.1-millisecond clock for test
WLDX	1C4	Gates C bus contents to the W register
WRDY	1D3	Stores TC readiness to accept an output character and enables output timing
WRIX	1C4	Clears the W register flip-flops prior to output
WSCP	1D1	Controls the shifting of output characters into the W register
WSIX	1C1	Stores the start of a load W register sequence
W00X to W10X	2	W register flip-flops that stores output data or control information

4.7 PROGRAMMING

The user writes the programs that use the TC. The TC can be programmed directly by CPU control (with or without using interrupts) or indirectly through a BIC.

The TC can supply interrupts to the PIM when this option is used in the computer. This frees the computer, since programmed delay and sense loops are unnecessary. With this feature, the program running in the CPU is interrupted at the proper time.

4.7.1 Operation Without BIC

The software initializes the TC (as does pressing the SYSTEM RESET switch on the computer control panel). The TC is then ready to accept output from the CPU and is also capable of accepting an input character from the TTY. The software normally issues a sense instruction and, if a sense-ready condition exists, follows it with a read (input) or load (output) instruction to enable the transfer of one character between the TC and the CPU.

Except for interrupts, the TC operates within the following general timing restrictions.

a. **Output:** Maximum data transfer rate is 10 characters per second (cps). There is no minimum rate. The CPU can output a single character, discontinue output for an indefinite period (longer than 100 milliseconds) and then output another character without loss of data or synchronization.

b. **Input:** Maximum data transfer rate is 10 cps (100 milliseconds per character). The CPU must read the input character transferred from the TTY by the TC during the last 9.1-millisecond stop-bit period. If the CPU fails to read the character input during this time and before the TTY inputs again, the character will be lost.

4.7.2 Operation with BIC

The TC uses two additional instructions when used with the BIC. After initializing the TC, the program sets up the TC input or output buffer areas in the BIC and issues the connect read register or the connect write register instruction to the BIC. The TC is then under BIC control. This sequence occurs only once for each new message area.

NOTE

The TC, even though physically cabled to the BIC, can still be operated under direct control from the CPU.

4.7.3 Description of Commands

The TC and the TTY respond to the instructions listed in table 4-2. Two of the external controls are reserved for use with the BIC. Appendix A lists the American Standard Code for Information Interchange (ASCII) and the corresponding TTY symbols.

The initialization instruction performs the same function as the SYSTEM RESET switch on the computer console. The TC is prepared to accept CPU output and to monitor TTY input. This instruction should not be issued while the TC is communicating with the TTY.

The sense instructions are sense ready to read and sense ready to write. They enable the CPU to determine TC status. If the sense condition is met, a data transfer can proceed. If the sense condition is not met, the CPU must wait to perform data transfer. A sense instruction can be issued at any time and normally precedes any data transfer instruction.

The data transfer instructions are the read (input) and load (output). They cause the transfer of data between the CPU and the TC through the read and write registers. Issuing a read or load instruction at the wrong time results in incorrect data transfer.

Table 4-2. TC and TTY Instructions

Mnemonic	Code	Description
External Control		
EXC 0101	0100101	Connect the write register to the BIC
EXC 0201	0100201	Connect the read register to the BIC
EXC 0401	0100401	Initialize the TTY
Data Transfer		
OAR 01	0103101	Transfer the A register to the W register
OBR 01	0103201	Transfer the B register to the W register
OME 01	0103001	Transfer memory to the W register
INA 01	0102101	Transfer the R register to the A register
INB 01	0102201	Transfer the R register to the A register
IME 01	0102001	Transfer the R register to memory
CIA 01	0102501	Transfer the R register to the cleared A register
CIB 01	0102601	Transfer the R register to the cleared B register

Table 4-2. TC and TTY Instructions *(continued)*

Mnemonic	Code	Description
Sense		
SEN 0101	0101101	W register ready
SEN 0201	0101201	R register ready

NOTES

1. W register = TC write register.
2. R register = TC read register.
3. The TC device address is assumed to be 01.

TTY Command Codes

Function	Symbol	Code	Typed as:
Print enable	SOM	0201	CONTROL and A
Print suppress	EOT	0204	CONTROL and D
Reader on	XON	0221	CONTROL and Q
Punch on	TAPE	0222	CONTROL and R
Reader off	XOFF	0223	CONTROL and S
Punch off	TAPE OFF	0224	CONTROL and T

TC maintenance consists of test programs, troubleshooting, and making repairs if required. If repair is indicated, it is recommended that the entire TC circuit card be replaced. The test programs are described in the 620 Test Program Manual (document number 98 A 9908 960). Troubleshooting is facilitated by familiarization with the operation of the TC and use of the logic diagram. This section provides troubleshooting data, program tests, and a list of reference documents to be used as maintenance aids.

5.1 TEST EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the TC.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM115 Extender Card, part number 44D0015

5.2 TEST PROGRAMS

The condition of the TTY unit should be periodically checked using test programs. These tests for TC and TTY are provided as part of the regular diagnostic package for the computer.

NOTE

One section of the TTY diagnostic for ASR models includes a print suppression test. The 33 ASR does not perform this function, so this diagnostic test should be bypassed when testing the 33 ASR. Refer to the 620 Test Programs Manual (document number 98 A 9908 960).

The TTY is a good diagnostic aid because the data being sent are printed out and can be analyzed. Also, known input patterns can be generated (via keyboard or paper tape) and data can be analyzed in the computer or returned to the TTY for printed analysis. If for some reason, such as PTR failure, the test program tapes cannot be read, a simple input/output program for verification and troubleshooting of the TTY-TC operation can be entered through the computer control panel. This program (table 5-1) tests keyboard input and printer output as follows:

a. Enter the program through the control panel.

b. Turn the TTY to ON-LINE.

c. Start the program at address 00000.

d. Input any character from the TTY to be transferred back to the TTY as an output from the CPU-TC almost immediately. Various character patterns and functions of the TTY can be checked by this echo method.

Table 5-1. Basic Input/Output Test Program

Location	Command	Description
00000	0101201	Sense read ready
00001	000004	If yes, jump to 00004
00002	001000	Jump back to 00000
00003	000000	
00004	0102501	Clear and input a TTY character to the A register
00005	0101101	Sense write ready
00006	000011	If yes, jump to 00011
00007	001000	Jump back to 00005
00010	000005	
00011	0103101	Output the A register (to TC)
00012	001000	Jump back to 00000
00013	000000	

5.3 CLOCK ADJUSTMENTS

The time settings of the 4.55-millisecond (receive) clock and the 9.1-millisecond (transmit) clock should be periodically checked and adjusted. The time period of the clocks can be monitored and adjusted (if required) while running TTY tests or using the following procedure:

a. Place the computer in the step mode.

b. Extend the TC circuit board if the presence of other computer option boards prevents direct access to the oscillator circuitry.

c. Set the TTY motor ON/OFF switch to OFF.

5.3.1 Input Clock Adjustment

Temporarily jumper the 4.55-millisecond clock input to ground (at pin 8 of IC26). The clock runs until SYSTEM RESET on the control panel is pressed.

Oscilloscope setup:	Set TIME to 1 or 2 msec/cm Set SYNC to positive internal Set voltage amplitude to (0.2) 2 or (0.5) 5 V/cm

Place the oscilloscope probe at the junction of pins 6, 9, and 10 of IC20. Adjust the oscilloscope to obtain one full square-wave period. This should have a duration of 4.55 milliseconds. If it does not, adjust potentiometer R6 until the correct period is obtained; then switch the scope to observe 22 periods (exactly 100 milliseconds). This allows fine timing adjustment (figure 5-1). After completing adjustment, the 4.55-millisecond clock can be stopped by removing the temporary jumper and pressing SYSTEM RESET.

5.3.2 Output Clock Adjustment

Temporarily jumper the 9.1-millisecond clock input to ground (at pin 9 of IC10). The clock runs until SYSTEM RESET is pressed.

Oscilloscope setup:	Set TIME to 1, 2, 5, or 10 msec/cm. Set SYNC to positive internal. Set voltage amplitude to (0.2) 2 or (0.5) 5 V/cm.

Place the oscilloscope probe at the junction of pins 2, 6, and 9 of IC1. Adjust the oscilloscope to obtain one full square-wave period. This should have a duration of 9.1 milliseconds. If it does not, adjust potentiometer R1 until the correct period is obtained; then switch the scope time base to observe 11 periods (exactly 100 milliseconds).

SECTION 5
MAINTENANCE

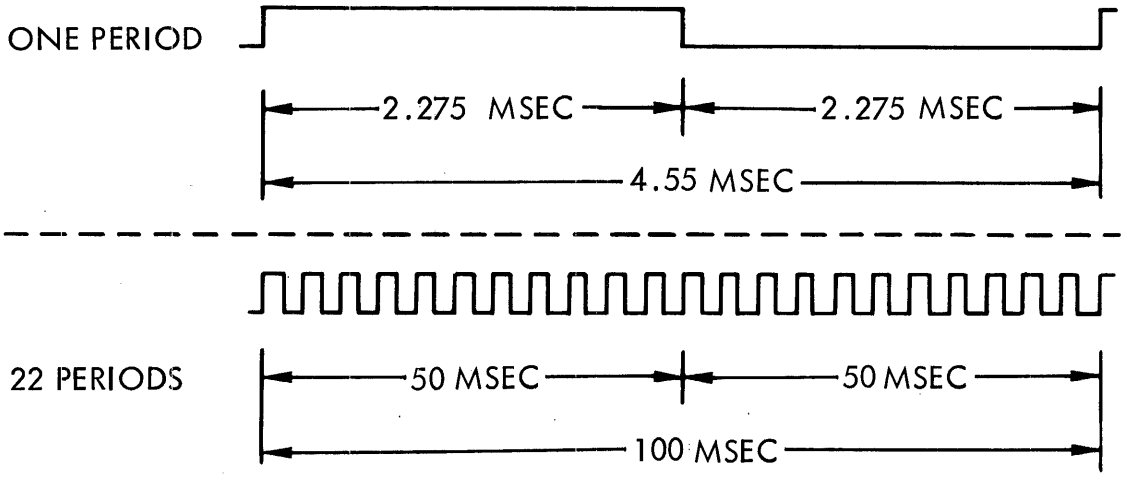

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Figure 5-1. Waveforms for Receive Clock Adjustment

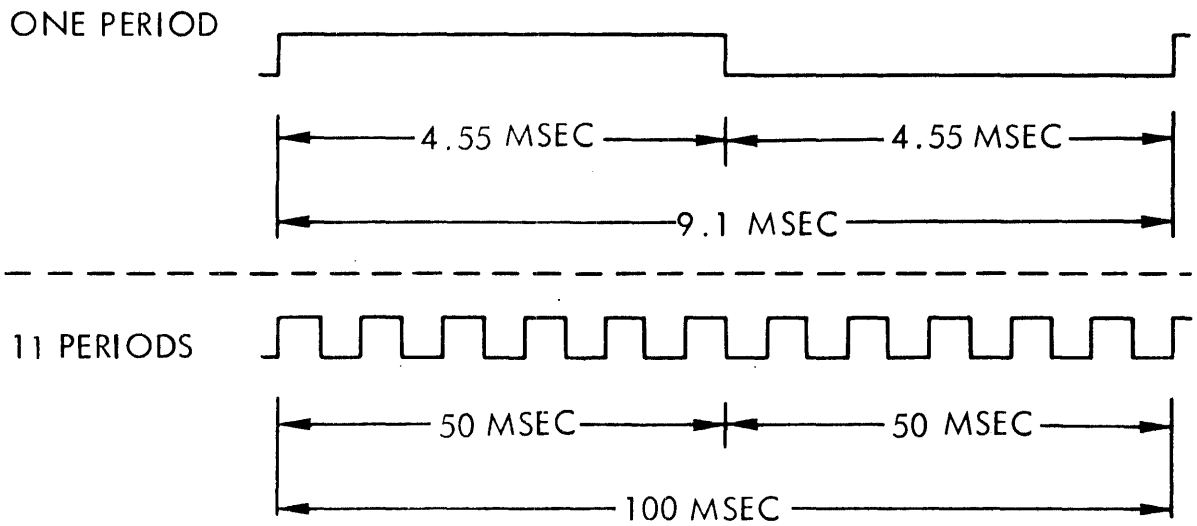

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Figure 5-2. Waveforms for Transmit Clock Adjustment

Switch the scope to observe 22 periods (exactly 200 milliseconds). Adjustment of the 9.1-millisecond clock is critical; observing a large number of periods allows the adjustment to be more accurately timed (figure 5-2). After adjustment, the clock can be stopped by removing the enabling jumper and pressing SYSTEM RESET.

5.4 TC/TTY TROUBLESHOOTING

The TTY units are normally trouble-free and require little attention; however, if operation is faulty, the following troubleshooting procedures are suggested. Visually inspect for broken belts, loose cams or components, loose or poorly seated connectors, blown fuses, or burned-out components.

NOTE

The TTY casework is cast and, therefore, somewhat fragile. Care should be taken when removing and reinstalling it.

5.4.1 Garbling

The following are possible sources of intermittent character change (printing or sending wrong characters).

TTY	Incorrect power supply output.
TTY	Incorrect motor speed.
TTY	Incorrect range adjustment.
TC	Incorrect 9.1- or 4.55-millisecond clock frequency.
TTY/TC	Incorrect loop current (too low or too high).

5.4.2 Motor Speed Check

The TTY character output rate must be 100 milliseconds per character. The motor speed, which is not adjustable, can be checked as follows.

a. Check RDDX (IC26, pin 9) with an oscilloscope. Set the oscilloscope SYNC to positive internal and the scope time to 10 or 20 msec/cm.

b. Hold down the RUBOUT and REPEAT keys on the TTY keyboard. Adjust the oscilloscope to observe the RDDX waveform. RDDX should set on every start bit and remain set until stop bit time, resetting on each new start bit. The time from set to set should be exactly 100 milliseconds. Switch the oscilloscope to observe that 10 characters occur each second. If the single character time is off by more than 2 milliseconds, the TTY motor may require change, overhaul, readjustment, or other maintenance.

5.4.3 Range Adjustment

The TTY receive section has a compensating RANGE knob (model 35) or lever (model 33) that may require occasional adjustment to compensate for receive loop distortion and to position the receiving loop mechanism for optimum sampling of the incoming signal. Before attempting range adjustment, verify proper TC output character length.

Full range adjustment is from 0 to 120. The Varian-modified 33 ASR optimum range adjustment is at or near the center, normally 60 to 65. If range adjustment is required, send an alternate pattern such as period. . .from the CPU. Loosen the RANGE set screw (model 33) or pull out RANGE knob (model 35) and slowly vary the setting of the knob or lever while observing the pattern being printed. When the characters begin to change (garble), one end of the effective range has been reached. Note the location of this point on the adjustment knob or lever. Move the adjustment clear up and then begin to garble when the other end of the range is reached.

Note the position of this point on the adjustment knob or lever, and position the range knob or lever midway between the observed range limit points. Tighten set screws, if applicable.

Range adjustment and motor speed should be checked if intermittent failures occur or after any major overhaul is performed on the TTY.

5.4.4 Signal Checks

The TC/TTY interface signals can be checked at slot 17 of the CPU groundplane with an oscilloscope. To check receive relay K1 when the TC is receiving from the TTY, connect the oscilloscope common to pin 113 and the oscilloscope probe to pin 112. To check send relay K2 when the TC is sending to the TTY, connect the oscilloscope common to pin 113 and the oscilloscope probe to pin 114. In each case, the bit pattern on the oscilloscope should be essentially rectangular and free from distortion. These signals can also be checked with a voltmeter at slot 17 (table 5-2).

Table 5-2. TC/TTY Interface Voltages

Setup Conditions		DC Meter Connections to TTY Card DM113		
Computer Power	**TTY Mode**	**Common**	**Hot**	**Approximate dc Voltage**
ON	On-line	Pin 113	Pin 114	0
(K2 relay contacts closed)		Pin 113	Pin 112	45
	Off-line	Pin 113	Pin 112	35
OFF	On-line (TTY running open)	Pin 113	Pin 114	0-2
(K2 relay contacts open)				
		Pin 113	Pin 112	42
	Off-line	Pin 113	Pin 112	42

5.4.5 Test Points

Table 5-3 lists some common test points on the TC. When signal synchronization is required, the following points can be used.

a. For output to the TTY, the start bit of the output character begins when WSIX goes high.

   Sync positive on IC10-13.

b. For input from the TTY, the start bit of the input character begins when RDDX goes high.

   Sync positive on IC26-9.

c. For input to the CPU, the input character sequence can begin any time after RRDY goes high.

   Sync negative on pin 101.

d. For output from the CPU, the output loading can begin any time after WRDY goes high.

   Sync positive on pin 33.

Table 5-3. Common TC Test Points

Circuit	Signal	Test Point
Output	WRDY (9.1-msec clock)	Pin 33
	WCKX (9.1-msec clock)	Pin 35
	WSCP	IC25-8
	Output to TTY	IC44-8 or K2-2
	Output to TTY	Across pins 114 and 113
	WLDX	IC39-8
	WSIX	IC10-13 or IC43-5
	W00X	IC26-6
	WRIX	IC40-6

Table 5-3. Common TC Test Points *(continued)*

Signal	Test Point
DAXX	Pin 100
FRYX	Pin 5
DRYX	Pin 3
SERX	Pin 2
DROX	IC41-9
DTIX	IC41-12
EXCX	IC4-6
EBRX	Pin 29
RRDY (4.55-msec clock)	Pin 101
RSCP	IC25-6
RRCP	IC40-8
RECX	IC36-9
RDDX	IC26-9
RRCX	IC31-9
TTRX (TTY input data)	IC43-11
Input from TTY	K1-4
Input from TTY	Across pins 113 and 112

Troubleshooting Check List

; and TTY are not operating:

Check voltages.

Check cable connections and board seating.

Check that the 9.1- and 4.55-millisecond clock oscillators start and stop.

d. Check that relays K1 and K2 are energized in normal static nonoperating condition. If not, the source of the problem can be the TTY, the relay loop supply, or a relay.

If the TC and TTY have intermittent problems:

a. Check voltages.

b. Check cable connections and board seating.

c. Remove and inspect the TC board for loose components, poor solder connections, and wrong-value components.

d. Check the 9.1- and 4.55-millisecond clock timing and, if necessary adjust it.

e. Observe the send and receive signals across the TTY relay lines.

NOTE

The K1 and K2 relays occasionally fail. Symptoms are excessive contact bounce and degraded make-break characteristics. Loop current provided by the TTY can be too high or too low. Loop current should be checked and should be about 20 mA.

5.5 REFERENCE DOCUMENTS

The documents listed below are useful as aids to understanding and maintaining the TC.

a. 620/L Reference Handbook (98 A 9905 000)

b. 620/L Maintenance Manual, Volume I (98 A 9905 051)

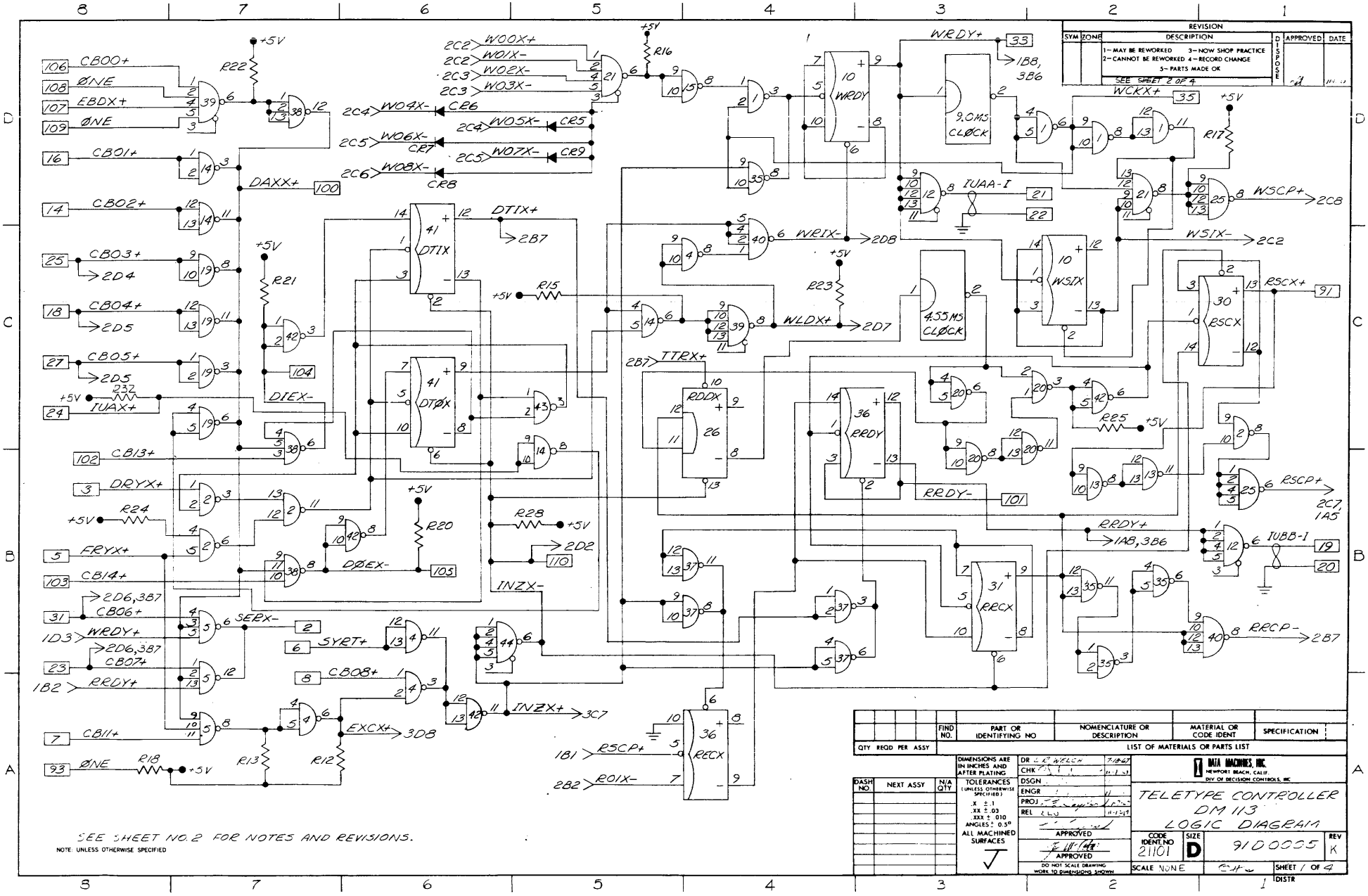
c. 620 Test Programs Manual (98 A 9952 160)

d. TC Board Logic Diagram (91D0005)

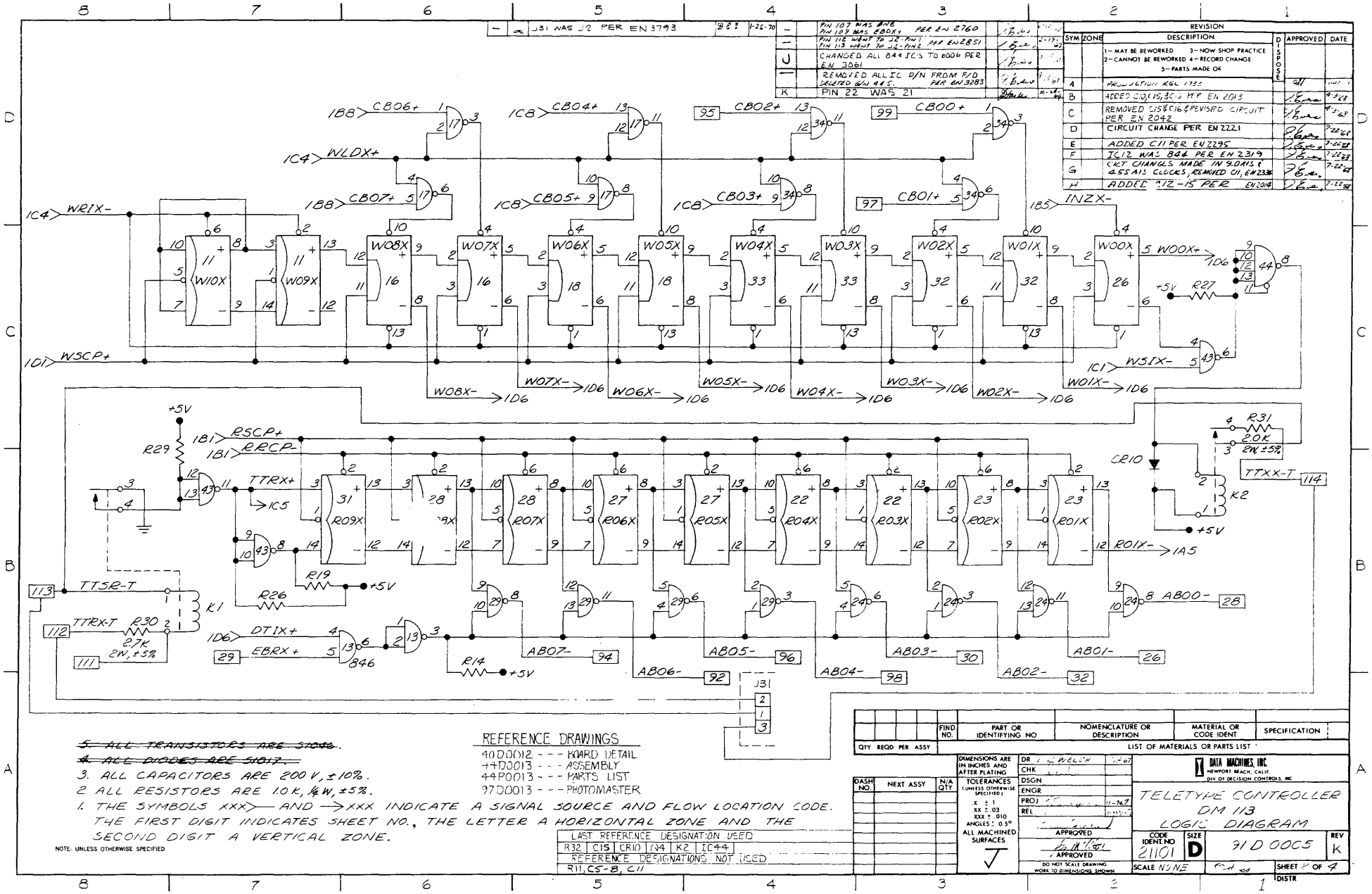
e. TC Board Assembly Drawing (44D0013)

SECTION 6
DRAWINGS AND PARTS LIST

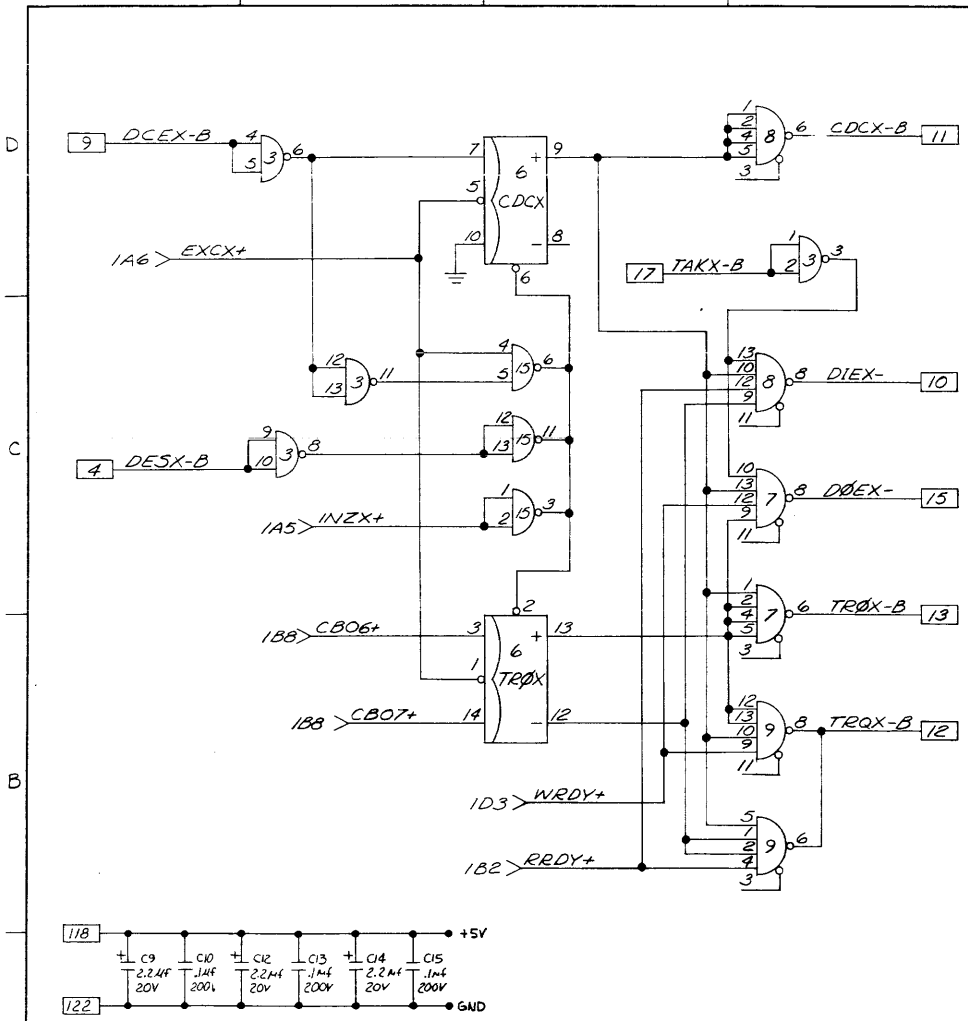
This section contains logic schematics and parts information for the TC circuitry.



REVISION
SYM ZONE DESCRIPTION DISPOSE APPROVED DATE
1- MAY BE REWORKED 3- NOW SHOP PRACTICE
2- CANNOT BE REWORKED 4- RECORD CHANGE
5- PARTS MADE OK
SEE SHEET 2 OF 4
CB00+
ØNE
EBDX+
ØNE
CB01+
CB02+
CB03+
2D4
CB04+
2D5
CB05+
2D5
IUAX+
CB13+
DRYX+
FRYX+
CB14+
2D6,3B7
CB06+
WRDY+
2D6,3B7
CB07+
RRDY+
CB11+
ØNE
DAXX+
DIEX-
DØEX-
SERX-
SYRT+
CB08+
EXCX+
3D8
INZX+
3C7
INZX-
DTIX+
2B7
DTIX
DTØX
WRDY+
1B8, 3B6
9.0MS CLØCK
WCKX+
IUAA-I
WSCP+
2C8
WRIX-
2D8
WSIX-
2C2
WLDX+
2D7
4.55MS CLØCK
RSCX+
TTRX+
RDDX
RRDY
RRDY-
RSCP+
2C7, 1A5
RRDY+
1A8,3B6
IUBB-I
RRCX
RRCP-
2B7
RSCP+
R01X-
RECX
SEE SHEET NO. 2 FOR NOTES AND REVISIONS.
NOTE: UNLESS OTHERWISE SPECIFIED
FIND NO. PART OR IDENTIFYING NO NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT SPECIFICATION
QTY REQD PER ASSY
LIST OF MATERIALS OR PARTS LIST
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES
DASH NO. NEXT ASSY N/A QTY
DR L R WELCH 7-18-67
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS SHOWN
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV OF DECISION CONTROLS, INC
TELETYPE CONTROLLER
DM 113
LOGIC DIAGRAM
CODE IDENT NO 21101
SIZE D
91D0005
REV K
SCALE NONE
SHEET 1 OF 4
DISTR



J31 WAS J2 PER EN 3793
PIN 107 WAS BNE PIN 109 WAS EBOX+ PER EN 2760
PIN 112 WENT TO J2-PIN 1 PIN 113 WENT TO J2-PIN 2 PER EN 2851
CHANGED ALL 844 IC'S TO 6006 PER EN 3061
REMOVED ALL IC D/N FROM F/D DELETED G/N 445. PER EN 3283
PIN 22 WAS 21
REVISION
SYM ZONE DESCRIPTION DISPOSE APPROVED DATE
1-MAY BE REWORKED 3-NOW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
A PRODUCTION RGL 1733
B ADDED C10, C15, & C16 PER EN 2013
C REMOVED C15 & C16 & REVISED CIRCUIT PER EN 2042
D CIRCUIT CHANGE PER EN 2221
E ADDED C11 PER EN 2295
F IC12 WAS 844 PER EN 2319
G CKT CHANGES MADE IN 9.0 AIS & 455 AIS CLOCKS, REMOVED C11, EN 2336
H ADDED C12-15 PER EN 2014
CB06+ CB04+ CB02+ CB00+
WLDX+
CB07+ CB05+ CB03+ CB01+
WRIX- INZX-
W10X W09X W08X W07X W06X W05X W04X W03X W02X W01X W00X
W00X+ R27 +5V
WSCP+ W5IX-
W08X- W07X- W06X- W05X- W04X- W03X- W02X- W01X-
RSCP+ RRCP-
R29 +5V
TTRX+ IC5
R09X R07X R06X R05X R04X R03X R02X R01X
R31 2.0K 2W, ±5%
CR10 K2 TTXX-T
R01X- 1A5
TTSR-T K1
TTRX-T R30 2.7K 2W, ±5%
R19 R26 +5V
DTIX+ EBRX+ 846
R14 +5V
AB00- AB01- AB02- AB03- AB04- AB05- AB06- AB07-
J31
5. ALL TRANSISTORS ARE S1046.
4. ALL DIODES ARE S1017.
3. ALL CAPACITORS ARE 200 V, ±10%.
2. ALL RESISTORS ARE 1.0 K, 1/4 W, ±5%.
1. THE SYMBOLS XXX>— AND —>XXX INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL ZONE AND THE SECOND DIGIT A VERTICAL ZONE.
NOTE: UNLESS OTHERWISE SPECIFIED
REFERENCE DRAWINGS
40D0012 - - - BOARD DETAIL
44D0013 - - - ASSEMBLY
44P0013 - - - PARTS LIST
97D0013 - - - PHOTOMASTER
LAST REFERENCE DESIGNATION USED
R32 C15 CR10 Q4 K2 IC44
REFERENCE DESIGNATIONS NOT USED
R11, C5-8, C11
FIND NO. PART OR IDENTIFYING NO NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT SPECIFICATION
QTY REQD PER ASSY
LIST OF MATERIALS OR PARTS LIST
DASH NO. NEXT ASSY N/A QTY
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES
DR CHK DSGN ENGR PROJ REL
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS SHOWN
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV OF DECISION CONTROLS, INC
TELETYPE CONTROLLER
DM 113
LOGIC DIAGRAM
CODE IDENT NO 21101
SIZE D
91 D 00C5
REV K
SCALE NONE
SHEET 2 OF 4
DISTR



1	GND
2	SERX-
3	DRYX+
4	DESX-B
5	FRYX+
6	SYRT+
7	CB11+
8	CB08+
9	DCEX-B
10	DIEX-
11	CDCX-B
12	TRQX-B
13	TRØX-B
14	CB02+
15	DØEX-
16	CB01+
17	TAKX-B
18	CB04+
19	IUBB-I
20	
21	IUAA-I
22	
23	CB07+
24	IUAX+
25	CB03+
26	AB01-
27	CB05+
28	AB00-
29	EBRX+
30	AB03-
31	CB06+
32	AB02-
33	WRDY+
34	
35	WCKX+
36	
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87	
88	
89	
90	
91	RSCX+
92	AB06-
93	ØNE
94	AB07-
95	CB02+
96	AB05-
97	CB01+
98	AB04-
99	CB00+
100	DAXX+
101	RRDY-
102	CB13+
103	CB14+
104	DIEX-
105	DØEX-
106	CB00+
107	EBDX+
108	ØNE
109	ØNE
110	INZX-
111	
112	TTRX-T
113	TTSR-T
114	TTXX-T
115	
116	
117	
118	+5V
119	
120	
121	
122	GND

REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1 – MAY BE REWORKED 3 – NOW SHOP PRACTICE 2 – CANNOT BE REWORKED 4 – RECORD CHANGE 5 – PARTS MADE OK			
		SEE SHEET 2 OF 4			

QTY REQD PER ASSY	FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
		LIST OF MATERIALS OR PARTS LIST			

DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR L. R. WELCH 7-18-67
CHK
DSGN
ENGR
PROJ 11-2-67
REL 11-2-67
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS SHOWN

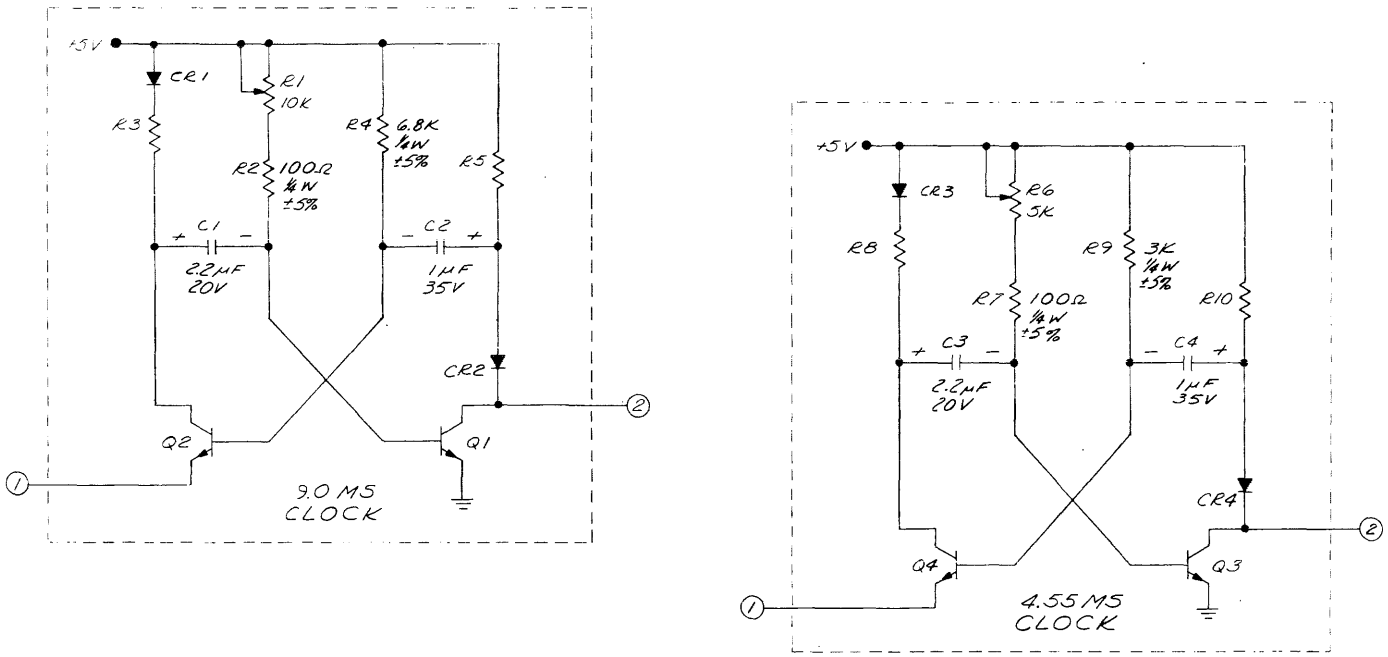
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF DECISION CONTROLS, INC.

TELETYPE CONTROLLER
DM 113
LOGIC DIAGRAM

CODE IDENT NO 21101 | SIZE D | 91D0005 | REV K

SCALE NONE | SHEET 3 OF 4 | DISTR

NOTE: UNLESS OTHERWISE SPECIFIED



REVISION					
SYM	ZONE	DESCRIPTION	DISPOSE	APPROVED	DATE
		1 – MAY BE REWORKED 3 – NOW SHOP PRACTICE 2 – CANNOT BE REWORKED 4 – RECORD CHANGE 5 – PARTS MADE OK			
		SEE SHEET 2 OF 4			

QTY REQD PER ASSY	FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION

LIST OF MATERIALS OR PARTS LIST

DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING

TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR	L.R WELCH	7-18-67
CHK		
DSGN		
ENGR		
PROJ		
REL		

APPROVED

APPROVED

DO NOT SCALE DRAWING
WORK TO DIMENSIONS SHOWN

DATA MACHINES, INC.
NEWPORT BEACH, CALIF
DIV OF DECISION CONTROLS, INC

TELETYPE CONTROLLER
DM 113
LOGIC DIAGRAM

CODE IDENT. NO	SIZE		REV
21101	D	91D0005	K

SCALE NONE

SHEET 4 OF 4

DISTR

NOTE: UNLESS OTHERWISE SPECIFIED

DWG NO. 44P0013

REVISIONS

REV	EN	CHG CODE	DESCRIPTION	DR	APPD
—	84047	--	ADDED REF DWG 98A0025	SJ	9/26/75

NEXT ASSEMBLY
MULTI-USASGE

MODEL NO.
620

varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

DR	KA	11/16/71
CHK	WGD	11/16/71
DSGN		
ENGR		
APPD	EBERLE	8/23/67
APPD		

CODE IDENT NO. 21101

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TITLE PARTS LIST DM 113 TELETYPE CONTROLLER ASSY.

SIZE	DWG NO.	REV
A	44P0013	AA

SHEET 1 OF 3

98A0153 000D

varian data machines
a varian subsidiary

DWG. NO. 44P0013

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				Ref	Ref	Ref	-	44D0013R	Assembly		
				Ref	Ref	Ref	-	91D0005K	Logic Diagram		
				Ref	Ref	Ref	-	97D0013	Photomaster		
				Ref	Ref	Ref	-	97D0645	Soldermask		
				Ref	Ref	Ref	-	97D0646	Silkscreen		
				REF	REF	REF	-	98A0025	TEST SPEC		
				1	1	1	1	40D0012-000P	Board Detail		
				10	10	10	2	53C0000-000	Bus, Power		
				2	2	2	3	71N0350-105	Capacitor	C2, C4	
				23	23	23	4	65N2500-102	Resistor, Fixed	R3,5,8,10,12 THRU 29,32	
				2	2	2	5	65N2500-101	Resistor, Fixed	R2, 7	
							6				
				1	1	1	7	65N2500-682	Resistor, Fixed	R4	
							8				
							9				
				1	1	1	10	65N2500-302	Resistor, Fixed	R9	
				1	1	1	11	65N2010-202	Resistor, Fixed	R31	
				1	1	1	12	65N2010-272	Resistor, Fixed	R30	
				1	1	1	13	64A0000-006	Resistor, Variable	R6	
				1	1	1	14	64A0000-007	Resistor, Variable	R1	
				10	10	10	15	77S1017-000	Diode, Silicon	CR1 - CR10	
				-	4	4	16	76S1072-000	Transistor	Q1-Q4	
							17				
				5	5	5	18	71N0200-225	Capacitor, Tant.	C9, C1, C3, C12, C14	
				1	1	1	19	82A0006-000	4V Form A Reed Relay	K2	
				1	1	1	20	82A0006-003	12V Form A Reed Relay	K1	
				4	4	4	21	0400109-000	Pad, Transistor		
				-	11	11	22	49A0002-000	Integrated Circuit	IC 6,10,11,22,23,27,28,30,31,36,41	

NEXT ASSY Multi-Usage | MODEL NO 620 | APPDC. Eberle 8-23-67

REV	—	Y	Z	—	AA	—	—	
EN NO	80270	80277	80466	80893	81156	82016	82195	
DATE	11/16/71	11/16/72	3/21/72	7/10/72	10/6/72	7/3/73	7/3/73	
DR	KA	KA	GRL	SDH	C.W.	WEB	WEB	
CHK	WGD	WGD	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	

TITLE: PARTS LIST
DM 113
TELETYPE CONTROLLER ASSY.

DWG NO 44P0013 | REV AA

SHEET 2 OF 3

96A0017-0008

varian data machines
a varian subsidiary

DWG. NO. 44P0013

PARTS LIST

CODE IDENT: 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				-	14	14	23	49A0008-000	Integrated Circuit	IC 1,4,13,14,15,17,19,20,24,29, 34,35,37,43	
							24				
				-	3	3	25	49A0007-000	Integrated Circuit	IC 2, 3, 42	
				-	2	2	26	49A0009-000	Integrated Circuit	IC 5, 38	
				-	2	2	27	49A0004-000	Integrated Circuit	IC 25, 40	
				-	5	5	28	49A0012-000	Integrated Circuit	IC 16,18,26,32,33	
				3	3	3	29	71A0006-100	Capacitor	C10, 13, 15	
				0	0	0	30	53A0003-004	Wire, Bus		
				0	0	0	31	54A0001-122	Sleeving, Insul.		
				-	7	7	32	49A0010-000	IC Input High Fan Out Gate	IC 7,8,9,12,21,39,44	
				0	0	-	33	90A0011-000	Humiseal		
				-	8	8	34	58A0131-002	Terminal, Bifurcated		
				11	-	-	35	49A0502-000	Integrated Circuit	IC 6,10,11,22,23,27,28,30,31 36,41	
				14	-	-	36	49A0508-000	Integrated Circuit	IC 1,4,13,14,15,17,19,20,24,29, 34,35,37,43	
				7	-	-	37	49A0510-000	Integrated Circuit	IC 7,8,9,12,21,39,44	
				3	-	-	38	49A0507-000	Integrated Circuit	IC 2,3,42	
				2	-	-	39	49A0509-000	Integrated Circuit	IC 5,38	
				2	-	-	40	49A0504-000	Integrated Circuit	IC 25,40	
				5	-	-	41	49A0512-000	Integrated Circuit	IC 16,18,26,32,33	
				4	-	-	42	76A2369-000	Transistor	Q1 thru Q4	

NOTES:

*REDRAWN

DWG NO 44P0013

REV AA

SHEET 3 OF 3

96A0017-001B

TELETYPEWRITER ASCII CODES

Character	ASCII	Character	ASCII	Character	ASCII
0	260	P	320	.	256
1	261	Q	321	/	257
2	262	R	322	:	272
3	263	S	323	;	273
4	264	T	324	<	274
5	265	U	325	=	275
6	266	V	326	>	276
7	267	W	327	?	277
8	270	X	330	@	300
9	271	Y	331	----	333
A	301	Z	332	----	334
B	302	(blank)	240	----	335
C	303	!	241	----	336
D	304	"	242	----	337
E	305	#	243	RUBOUT	377
F	306	$	244	NUL	200
G	307	%	245	SOM	201
H	310	&	246	EOA	202
I	311	'	247	EOM	203
J	312	(	250	EOT	204
K	313	)	251	WRU	205
L	314	*	252	RU	206
M	315	+	253	BEL	207
N	316	,	254	FE	210
O	317	-	255	H TAB	211

APPENDIX A
TELETYPEWRITER ASCII CODES

Character	ASCII	Character	ASCII	Character	ASCII
LINE FEED	212	TAPE AUX	----	S0	230
V TAB	213	ON	222	S1	231
FORM	214	X-OFF	223	S2	232
RETURN	215	TAPE OFF	----	S3	233
SO	216	AUX	224	S4	234
SI	217	ERROR	225	S5	235
DCO	220	SYNC	226	S6	236
X-ON	221	LEM	227	S7	237