PRIORITY INTERRUPT MODULE

an option for the

Varian Data Machines

Computer Systems

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SECTION 1
GENERAL DESCRIPTION

The Priority Interrupt Module is an I/O option available with Varian 70 series and 620 computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of Operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics, and parts lists are supplied in a System Maintenance Manual. This manual is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the part numbers of other manuals pertinent to the Varian 70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9):

V72 System Handbook	98 A 9906 20x
V73 System Handbook	98 A 9906 01x
V74 System Handbook	98 A 9906 21x
V75 System Supplement	98 A 9906 22x
Processor Manual	98 A 9906 02x
8K Core Memory Manual	98 A 9906 03x
8K Semiconductor Memory Manual	98 A 9906 04x
16K Core Memory Manual (1200 ns)	98 A 9906 24x
16K Core Memory Manual (990 ns)	98 A 9906 25x
Option Board Manual	98 A 9906 05x
Power Supply (Universal) Manual	98 A 9906 06x
V72 Power Supply Manual	98 A 9906 12x
Microprogramming Guide	98 A 9906 07x
Writable Control Store Manual	98 A 9906 08x
Memory Map Manual	98 A 9906 10x
MAINTAIN III Manual	98 A 9952 07x

The priority interrupt module (PIM) provides for the orderly servicing of peripheral-initiated interrupts of a program in progress. It does so by:

a. Establishing up to eight levels of interrupt priority for selected peripheral controllers.

b. Storing interrupt requests originated by associated peripheral controllers and placing the requests on the I/O bus in the order of the established priority.

In effect, the PIM organizes a " priority-within-a-priority" system. Peripheral controllers that cannot normally initiate an interrupt because of their inability to generate memory addresses can do so when connected to the PIM. PIM-controlled priority assignments are prewired at the factory to user specifications.

Table 1-1 lists the PIM specifications.

Table 1-1. PIM Specifications

Parameter	Description
Organization	Contains line synchronization, and mask registers; an interrupt address generator; priority and control logic; and line drivers and receivers
Control Capability	Establishes and implements eight levels of interrupt priority (user-assigned) for system peripheral controllers.
I/O Capability	Five external control and three transfer instructions
Standard Device Address	040 through 043
Interrupt Addresses	First PIM: 0100 through 0117 Second and succeeding PIMs: 0120 through 0177

Table 1-1 PIM Specifications (continued)

System Priority Assignment	Determined by location in the system priority chain (user-selected)
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by-12-inch (19.7 x 30.3 cm) printed circuit board.
Power	5V dc at 0.45A
Operating Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

SECTION 2
INSTALLATION

2.1 INSPECTION

The PIM has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

a. Notify the transportation company.

b. Notify Varian Data Machines.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The PIM circuits are contained on a single printed-circuit (PC) board (p/n 44P0683). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 each contain eight interrupt lines (IL00– through IL07–) that can be connected to selected peripheral controllers. Connector P1 also contains the same eight interrupt lines as well as all I/O bus control signals for the PIM.

2.3 PIM INTERRUPT LINES

The PIM has eight interrupt lines that enable up to eight peripheral controllers to be connected in the desired order of priority. The interrupt lines are designated IL00– through IL07– , where IL00– has the highest priority and IL07– the lowest. For controllers that are installed in the same chassis as the PIM, the interrupt lines are connected at the computer backplane connector that mates with P1 of the PIM board. For controllers in a different chassis, the interrupt lines are contained in either an I/O expansion cable that connects to P1 of the PIM (via computer backplane) or in an interrupt cable that connects to J1 or J2 of the PIM. Pin assignments for the interrupt lines are listed in table 2-1.

Table 2-1. Pin Assignments for Interrupt Lines

Interrupt Lines	P1	J1	J2	Interrupt Lines	P1	J1	J2
IL00–	108	3	3	IL04–	102	11	11
IL01–	114	13	13	IL05–	88	5	5
IL02–	104	9	9	IL06–	112	1	1
IL03–	110	15	15	IL07–	86	7	7

2.4 DEVICE ADDRESS ASSIGNMENT

The device address for each PIM is implemented with jumper wires installed on the computer backplane connector that mates with P1 of the PIM board (figure 2-2). Device addresses 040 through 043 are reserved for PIM. Normally 040 is assigned to the first PIM, 041 to the second, 042 to the third, and 043 to the fourth. Address 044 affects all PIMs simultaneously and is used to enable or disable all PIMs.

2.5 INTERCONNECTION

In the V70 series systems, the PIM is installed in a designated slot of an I/O chassis. Refer to the appropriate Varian 70 Series System Handbook for further installation information.

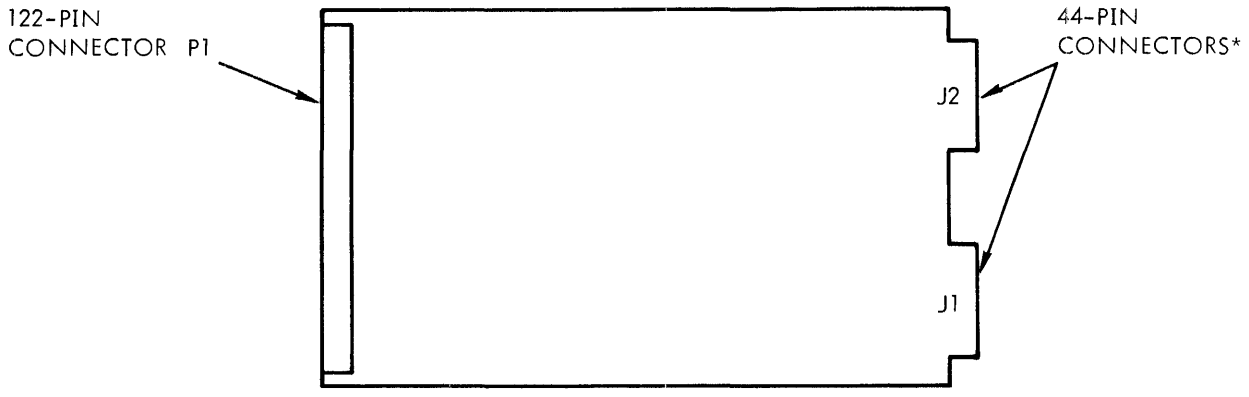

Figure 2-1. PIM Board (Component Side)

The PIM can be installed in designated slots of the mainframe and expansion chassis for 620/L systems, and in designated slots of the memory and I/O expansion chassis for 620/f-100 systems. Further installation information for these computer systems, can be found in the 620/L Maintenance Manual (document number 98 A 9905 15x) and the 620/f-100 Maintenance Manual (document number 98 A 9908 15x).

The pin assignments for the connectors on the PIM board are provided in logic diagram 91D0016.

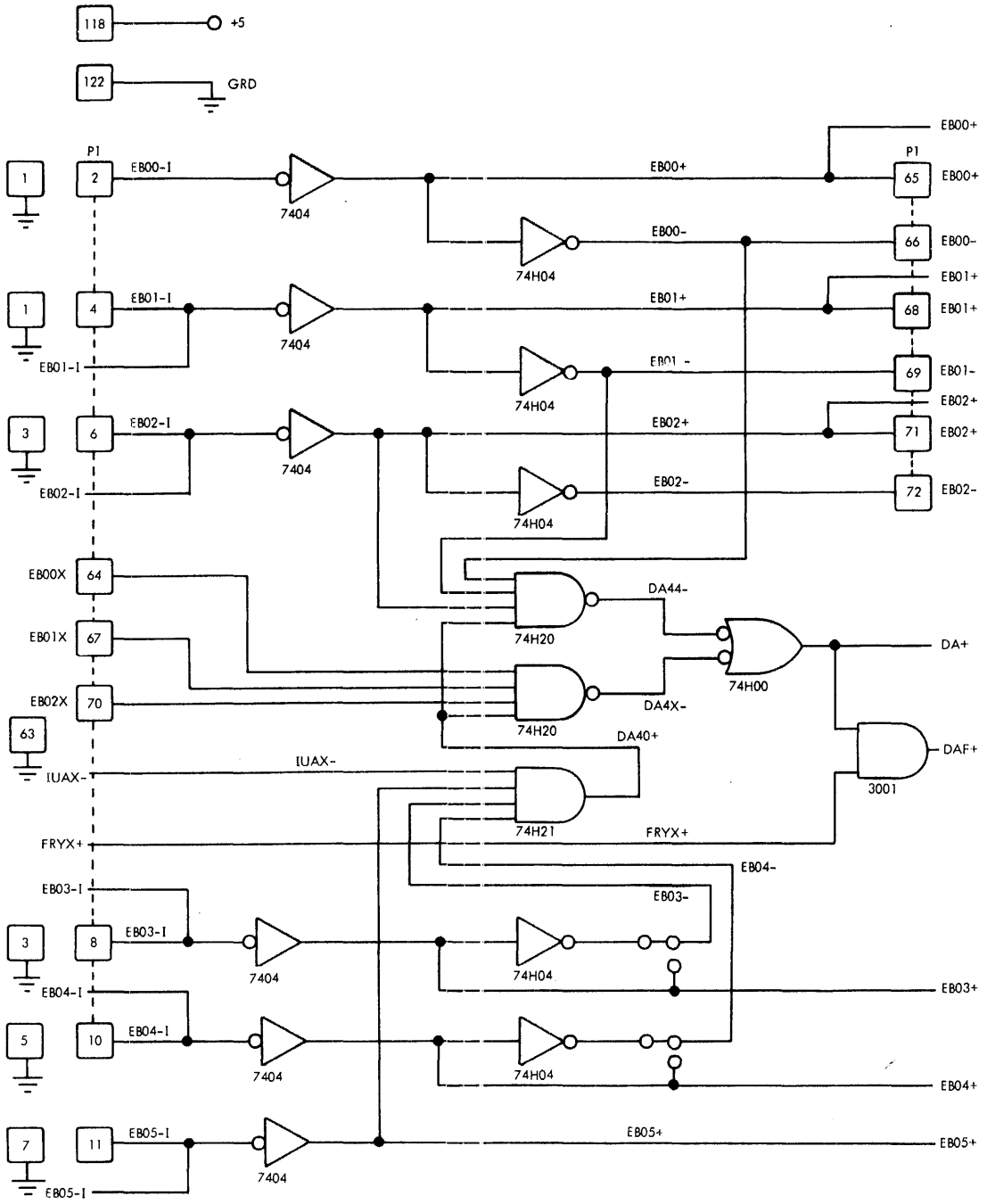

Figure 2-2. Device Address Connections

SECTION 3
OPERATION

The PIM has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The PIM responds to the five external control and three data transfer instructions listed in table 3-1.

loops. Two NOP instructions are required after an external control (EXC) instruction.

For computer systems containing the memory protection (MP) option in addition to the PIM, the MP is disabled everytime an interrupt is serviced. Therefore at the end of the PIM service program, the MP must be enabled again.

Table 3-1. I/O Instructions

Mnemonic	Program Code	Functional Description
External Control		
EXC 014*	10014*	Clear interrupt registers.
EXC 024	10024	Enable PIM.
EXC 0244	100244	Enable all PIMs in system.
EXC 034	10034	Clear interrupt registers and enable PIM.
EXC 044	10044	Disable PIM.
EXC 0444	100444	Disable all PIMs in system.
EXC 054	10054	Clear interrupt registers and disable PIM.
Data Transfer		
OME 04	10304	Transfer contents of memory to mask register.
OAR 04	10314	Transfer contents of A register to mask register.
OBR 04	10324	Transfer contents of B register to mask register.

*** represents the last octal digit of the device address.**

3.2 PROGRAMMING CONSIDERATIONS

When preparing a PIM program, clear the interrupt registers to establish initial conditions. To mask peripheral controllers, write a mask word in the program. The eight least significant bits of the mask word correspond to the eight priority interrupt lines. Setting bit 0 inhibits the highest priority line, setting bit 1 inhibits the second-highest priority line, etc. The mask register must be loaded by the program after any power-up sequence, including the power-up cycle of the power failure/restart (PF/R) feature. System reset does not clear the PIM mask register.

When program loops contain only uninterruptable instructions, interrupts cannot occur. Thus, when recognition of an interrupt is imperative (such as with the PF/R), at least one no-operation (NOP) instruction must be added to such

3.3 UNINTERRUPTABLE INSTRUCTIONS AND CONDITIONS

An interrupt can only be detected during the last cycle of an instruction execution. In V70 and 620/f-100 systems using the memory protection feature, interrupts can be detected immediately following all instructions except:

a. Halt (HLT) instructions

b. Any external control (EXC) I/O instruction

c. Any execution instruction. If the condition is met, interrupts are inhibited between executions of an execution instruction and the instruction at the execution address. If the condition is not met,

interrupts are inhibited between executions of an execution instruction and the instruction following in sequence.

d. Any instruction executed in the step mode.

In Varian 70 series and 620/f-100 systems without the memory protection feature, detection of an interrupt is inhibited during the following types of instructions:

a. Halt (HLT) instructions

b. All shift instructions

c. All I/O instructions

d. All double-word instructions

e. All multiplication or division instructions

f. Any instruction executed in the step mode

In all 620/L systems, detection of an interrupt is inhibited during the following types of instructions and conditions:

a. Halt (HLT) instructions

b. All jump, jump and mark, or execution instructions when the jump condition is met. (When the jump condition is not met these instructions are interruptable).

c. All I/O instructions

d. All shift or rotation instructions

e. All multiplication or division instructions

f. During the processor cycle immediately following an external control (EXC) I/O instruction.

g. During the processor cycle immediately following a shift, rotation, multiplication, or division instruction during which a trap occurred (DMA operation).

h. During the first instruction executed after entering run mode if that instruction is a single-word instruction.

i. During a manual step operation

j. During a halt condition

3.4 PROGRAM EXAMPLE

Table 3-2 shows a typical program using the PIM. In this program, 256 descending binary frames are transferred to the high-speed paper tape punch. Memory locations 01000 to 01023 are used in the program as are computer mnemonic codes with corresponding machine language codes.

Table 3-2. Program Example

Machine Code		Source Code			
Location	**Instruction**	**Label**	**Mnemonic**	**Operand**	**Description**
001000		STRT	.ORG	.01000	
001000	011011		.LDA	.MASK	FETCH INTERRUPT MASK
001001	103140		.OAR	.040	AND STORE IN REGISTER
001002	006010		.LDAI	.0377	INITIALIZE OUTPUT DATA
001003	000377				
001004	103137		.OAR	.037	PRIME INTERRUPT MODULE
001005	100240		.EXC	.0240	ENABLE PIM
001006	005000		.NOP	.	
001007	001000		.JMP	.*-1	DELAY FOR INTERRUPTS
001010	001006				
001011	000376	MASK	.DATA	.0376	
*		INTERRUPT	PROCESSING	SUBR	
001012	000000	INTR	.ENTR	.	
001013	005311		.DAR	.	DECR OUTPUT DATA
001014	103137		.OAR	.037	OUTPUT DATA TO PUNCH
001015	100240		.EXC	.0240	RE-ENABLE PIM
001016	001010		.IAZ	.*+4	
001017	001022				
001020	001000		.JMP*	.INTR	EXIT
001021	101012				
001022	100440		.EXC	.0440	CLEAR PIM
001023	000000		.HLT	.	END OF PROGRAM
		INTERRUPT	ADDRESS		
000100			.ORG	.0100	
000100	002000		.JMPM	.INTR	
000101	001012				
	000000		.END	.	

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

Communication between the PIM and the processor is similar to that of any peripheral controller except that the PIM can request a program interrupt. When the computer acknowledges the interrupt, the PIM specifies the memory location of the instruction to be executed.

The PIM scans the interrupt lines with every cycle of the interrupt clock (IUCX-I). If signals are detected on more than one line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored in the PIM interrupt-line register until acknowledged. The PIM has an eight-bit mask register that selectively inhibits interrupt requests from the interrupt-line register. When a given flip-flop of the mask register is set, corresponding interrupt requests from the interrupt-line register are inhibited. When the mask register flip-flop is reset, the interrupt request is not inhibited. The mask register is unaffected by system reset and must be loaded under program control using data-transfer instructions.

Acknowledgment of an interrupt by the processor causes execution of the instruction located at the memory address specified by the PIM. Any instruction can be executed except an I/O type. An interrupt is thus serviced in one instruction period.

4.2 FUNCTIONAL DESCRIPTION

The following subsections describe the five functional circuits of the PIM (figure 4-1). Refer to the timing waveforms of figure 4-2 and the PIM logic diagram.

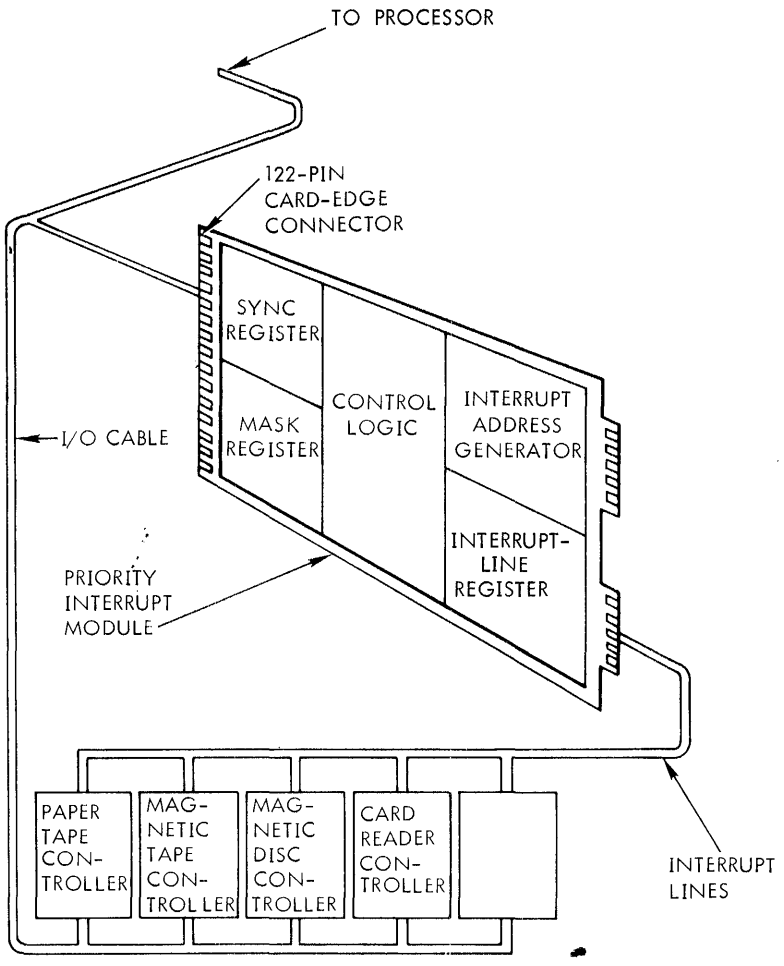

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Figure 4-1. PIM Functional Block Diagram

4.2.1 Control Logic

The control logic circuit directs and sequences the response of the PIM to external control, data transfer, and interrupt operations. When a computer program interrupt is requested, the processor requests the PIM to place the interrupt address on the I/O bus. If the PIM has system priority, the address line drivers are enabled. The PIM interrupt-request signal will remain active until all interrupts stored (but not inhibited) by the PIM have been acknowledged, or until PIM priority is lost.

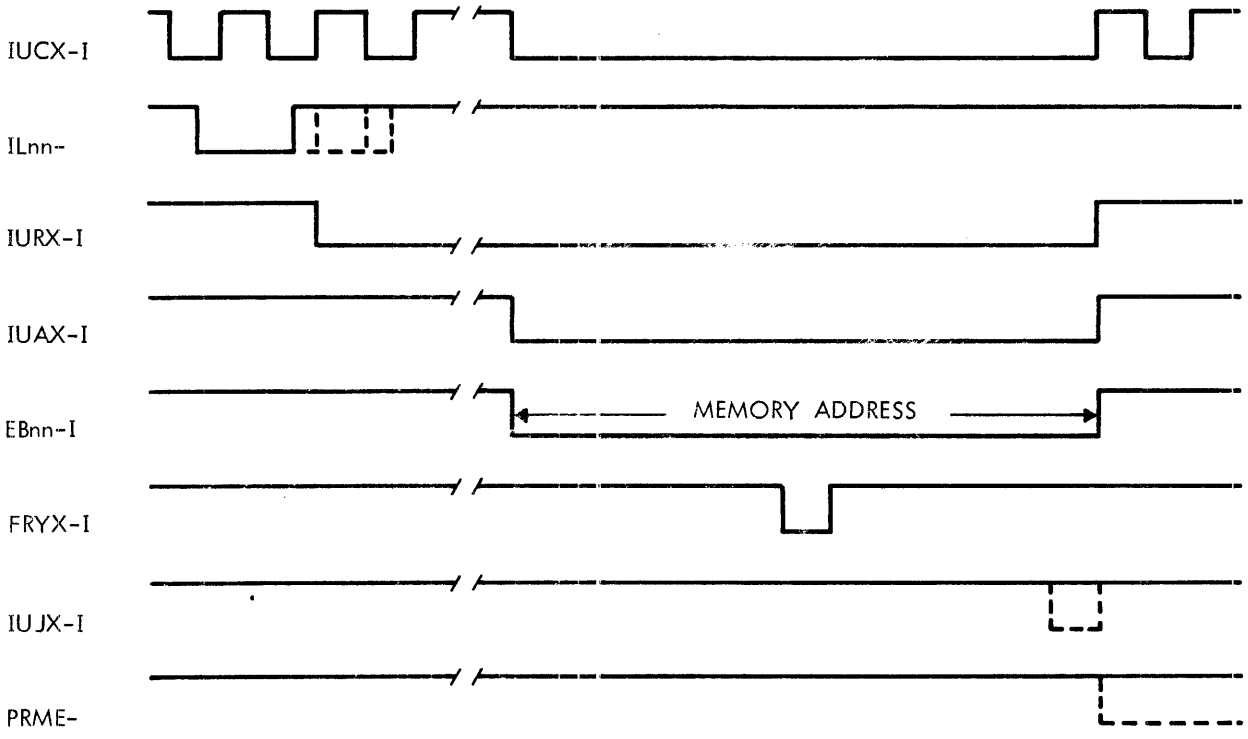
The control logic circuit consists of flip-flops PRME, DTOX, IURM and associated gates. During the execution of an output data transfer command, signals FRYX and DA set DTOX. DTOX+ high and DRYX+ generate SMR1- low, which transfers the mask word from the I/O bus to the mask register. At the end of the transfer, DRYX+ resets flip-flop DTOX. DA, in conjunction with FRYX+, indicates that the central processor is communicating with the PIM.

External control commands for the PIM are indicated by EXCX+ low. EB06+, EB07+, and EB08+ are combined with EXCX+ to actuate the five external control commands.

Flip-flop PRME provides master enable/disable for the entire PIM. When PRME is reset, computer program interrupts cannot be requested by the PIM; however, the PIM continues to receive and store interrupts from external devices. When PRME+ is high, flip-flop IURM is set by INR1+ high, one IUCX-I clock period after an interrupt is clocked into the sync register. IURM+ and PRME+ high plus PRMX-I low generate IURX-I low, requesting an interrupt.

When a computer program interrupt is requested by the PIM, the processor responds with signal IUAX-I low. This signal requests that PIM place the interrupt instruction address on the I/O bus.

If the PIM has system priority, the address line drivers are enabled as long as IUAX-I is low. When IUAX-I goes low, IUCX-I is held low. Interrupt conditions are therefore held static during the time that IUAX-I is low. Flip-flop IURM is cleared when all interrupts received by the PIM have been acknowledged by the central processor.



VTII-347B

Figure 4-2. Timing for Reception and Servicing of a Single Interrupt

4.2.2 Interrupt Address Generator

The interrupt address generator consists of coding logic that generates the binary number of the interrupt line requesting the interrupt. A pair of memory locations is reserved for each interrupt line. The interrupt addresses are normally in memory locations 0100 through 0117. However, the 16 interrupt addresses can be placed anywhere within the first 128 memory locations except 040 through 047, and may be placed at other addresses by special request.

The interrupt address generator consists of three gates that use line priority signals to generate signals A0XX+, A1XX+, and A2XX+. These signals consititute three bits of the address code for the interrupt line to be serviced. They are placed on the I/O bus by IAEX+ low. The least-significant bit of the address code is always low, resulting in an even address. This bit is supplied by the processor when the second word of a double-word interrupt instruction is accessed.

Signal IAEX+ low is generated by signals PRMX-I and IUAX-I low and FF set signal PRME+ and IURM+ high. These four signals indicate, respectively, that: the PIM has priority; the PIM interrupt has been acknowledged; the PIM is activated; and interrupt awaits on one of the interrupt lines.

4.2.3 Interrupt-Line Register

The interrupt-line register consists of eight flip-flops that asynchronously accept interrupt inputs. An interrupt is stored in the register until the interrupt is serviced or until the entire register is cleared by command.

The interrupt-line register consists of flip-flops LR00 through LR07. An interrupt is generated when an interrupt line signal, ILnn−, goes low. IL00− through IL07− are each connected to the clock input of an interrupt-line register flip-flop. ILnn− may remain low for any period of time greater than 0.2 microseconds; a constant low does not produce repetitive interrupts. If the interrupt is serviced, the flip-flop is reset by IUCP+ and a line priority signal, LPnn+. Although IUCP+ is sent to all register flip-flops, only the flip-flop that was serviced is reset.

4.2.4 Sync Register and Line Priority

The sync register consists of eight flip-flops. At each interrupt clock period, the outputs of the interrupt-line register are clocked into the sync register. The sync register, therefore, samples the status of the eight interrupt lines synchronously with the computer interrupt clock. The sync register outputs activate the priority logic used to generate the interrupt address.

If two or more interrupts occur simultaneously, the line with the highest priority is given precedence and all other lines are temporarily inhibited. An interrupt line can request a computer program interrupt only if the line has not been inhibited and a higher-priority line is not active.

The sync register consists of flip-flops IR00 through IR07. IUC1− clocks the contents of the interrupt-line register into the sync register. The outputs of the sync register are fed into a network of gates that determine the priority of each interrupt line signal. The line priority circuit generates signal INR1+, which enables the generation of signal IURX−I. In addition, LP00+ through LP07+ determine the interrupt address and the interrupt-line register flip-flop to be reset after servicing its interrupt. IL00− has the highest priority, and signal IL07− has the lowest.

4.2.5 Mask Register

The mask register inhibits interrupt requests from selected interrupt lines to be disarmed while other lines are permitted to cause a program interrupt. The eight flip-flops of the mask register inhibit corresponding interrupt requests from the interrupt-line register. The mask register must be loaded under program control to establish which interrupts are to be inhibits.
EB00+ through EB07+ are loaded into the mask register when a particular interrupt is to be masked (inhibited). SMR1+ clocks this mask word into the register. The register outputs are fed into the line priority circuit. If one or more interrupts are inhibited by the mask register, the highest-priority unmasked interrupt is serviced.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting PIM troubleshooting. The Varian MAINTAIN III test program system (Test Programs Manual, 98 A 9952 07x) contains a PIM test program used to test various phases of PIM operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommeded for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

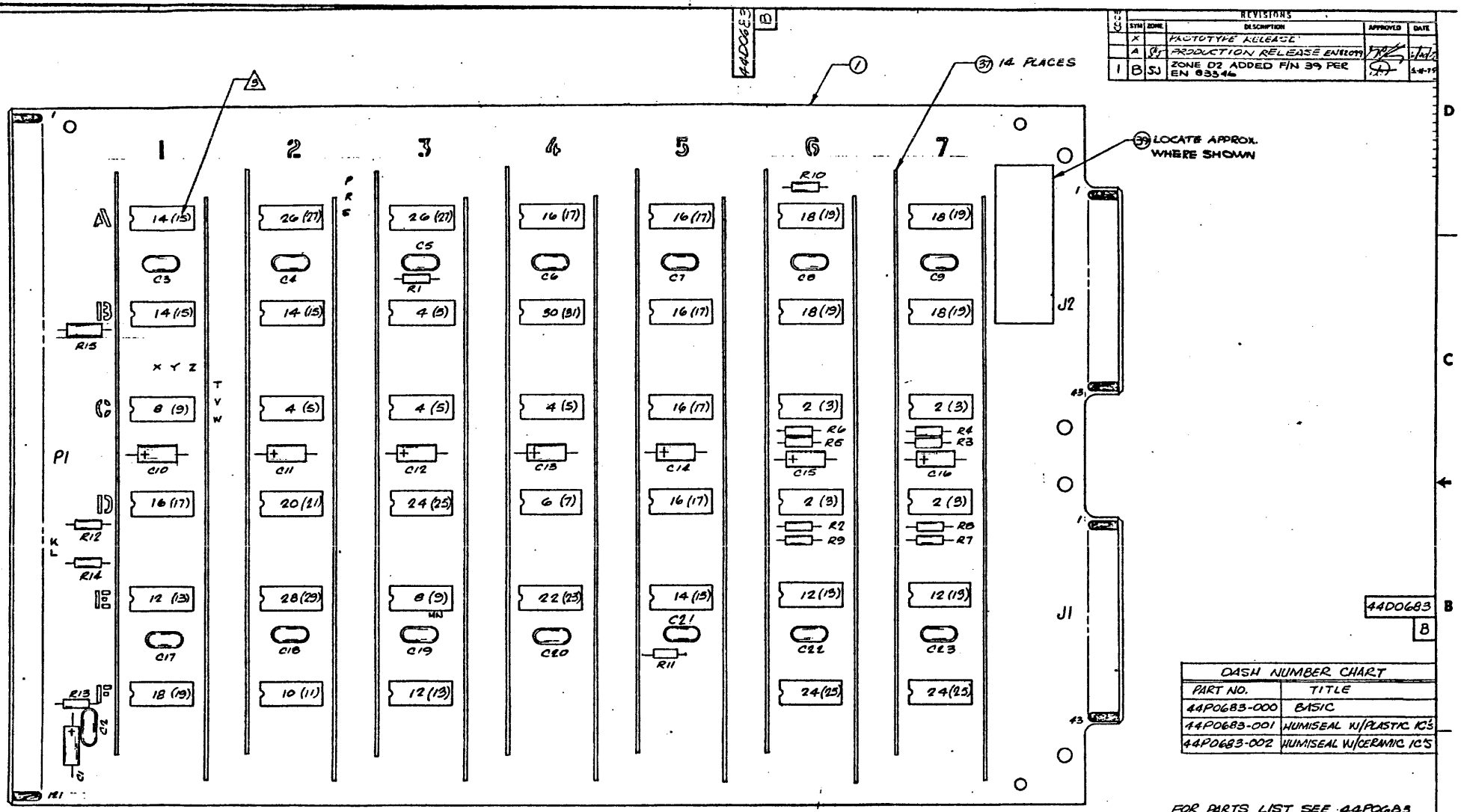
c. Soldering iron, 39-watt pencil type.

5.2 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Mnemonics	Description
AnXX	Address code of device with priority interrupt.
CACR	Clear ac register. Generates signal CILR on receipt of signal EXCX.
CILR	Clear line register. Clears the line and sync registers.
DA	Decoded device address.
DRYX	Data ready pulse that resets flip-flop DTOX; enables signal SMR1.
DTOX	Data transfer out flip-flop. Stores the occurrence of an output command from the processor.
EBnn-I	Address or function code bit from I/O bus.
EXCX	Enables initialization of PIM upon external control command.
FRYX	Function ready pulse that sets flip-flop DTOX.
IAEX	Interrupt address enable. Gates address of interrupt line onto I/O bus.
ILnn	Interrupt line from peripheral controller.
INRn	Interrupt request. Indicates a request from one or more interrupt lines.
IRnn	Sync register outputs. Stores the status of the line register in synchronism with the interrupt clock signal.
IUAX	Interrupt acknowledgment. Enables servicing of PIM interrupts.
IUCP	Interrupt completion resets line register flip-flop after interrupt is serviced.
IUCX	Interrupt clock. Provides timing for servicing of PIM interrupt request.
IUCI	Interrupt clock inverted. Clocks contents of line register into sync register.
IUDX	Interrupt detection. Sets flip-flop IURM.
IUJX	Interrupt jump. Inhibits the PIM after a jump and mark command.
IURM	Interrupt request memory flip-flop. Stores a request for an interrupt from an interrupt line.
IURX-I	Interrupt request. Sent to the processor to request signal IUAX-I.
KPRME	K-input to PRME
LPii	Line priority signals. Indicates the eight PIM priorities.
LRnn	Line register flip-flop outputs. Stores request for an interrupt from a device connected to an interrupt line.
PRME	PIM enabling flip-flop. Stores the activation of the PIM.
PRMX	Priority input. Gives priority to PIM.
PRNX	Priority output. Passes priority to next in line after interrupts are serviced.
SMR1	Clocks mask word into mask register.
SYRT	System reset. Clears flip-flops DTOX and PRME and generates signal CILR when control-panel reset switch is pressed.


44D0683 B
REVISIONS
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A | SJ | PRODUCTION RELEASE EN11099
B | SJ | ZONE D2 ADDED F/N 39 PER EN 03346
(1)
(3) 14 PLACES
(5)
(39) LOCATE APPROX. WHERE SHOWN
1 2 3 4 5 6 7
A B C D
P1
J1
J2
R10
R15
R12
R14
R13
C4
C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23
R1 R11 R2 R3 R4 R5 R6 R7 R8 R9
X Y Z
T V W
K L
14 (15) 26 (27) 26 (27) 16 (17) 16 (17) 18 (19) 18 (19)
14 (15) 14 (15) 4 (5) 50 (51) 16 (17) 18 (19) 18 (19)
8 (9) 4 (5) 4 (5) 4 (5) 16 (17) 2 (3) 2 (3)
16 (17) 20 (21) 24 (25) 6 (7) 16 (17) 2 (3) 2 (3)
12 (13) 28 (29) 8 (9) 22 (23) 14 (15) 12 (13) 12 (13)
18 (19) 10 (11) 12 (13) 24 (25) 24 (25)
44D0683 B
DASH NUMBER CHART
PART NO. | TITLE
44P0683-000 | BASIC
44P0683-001 | HUMISEAL W/PLASTIC IC'S
44P0683-002 | HUMISEAL W/CERAMIC IC'S
FOR PARTS LIST SEE 44P0683
5. NUMBERS IN PARENTHESIS ( ) ARE FOR THE -002 ONLY. -000 & -001 VERSIONS SHOWN
4 AFTER FINAL TEST AND PRIOR TO ACCEPTANCE TEST (-001, -002 ONLY) MASK OFF CONNECTOR CONTACT AREA ON BOTH SIDES OF F/N 1 AND TOTALLY COAT BOTH SIDES OF ASSEMBLY WITH F/N 38.
1 MARK WITH APPROPRIATE DASH NO. AND THE REVISION LETTER OF THE PARTS LIST TO WHICH THE PART WAS MANUFACTURED AND THE SERIAL NO. APPROX WHERE SHOWN. IDENTIFICATION TO BE .12 HIGH CHARACTERS PERMANENT AND LEGIBLE.
NOTE: UNLESS OTHERWISE SPECIFIED
MODEL NO. 620/VT3
NEXT ASSY 01P0094
MATERIAL
FINISH
DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
X ± .1
.XX ± .03
.XXX ± .005
ANGLES ± 0.5°
BREAK ALL SHARP EDGES .005 R APPROX
DO NOT SCALE DRAWING
DR K.Williams 3/21/73
CHK (J.) Brown 4/9/73
DSGN D.Wing 4/9/73
ENGR E.F.Neuman 4/11/73
APPD [illegible] 4/11/73
APPD
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vdm varian data machines
2722 michelson drive / irvine / california / 92665
TITLE
PRIORITY INTERRUPT ASSY DM 398
CODE IDENT NO. 21101
SIZE D
DWG NO 44D0683
REV B
SCALE 2/1
SHEET 1 OF 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4 W, 5%

2. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS: 1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C23	
R15	
P2,	
J2	

REFERENCE DRAWINGS	
40D0617	BOARD DETAIL
44D0683	ASSEMBLY
44P0683	PARTS LIST
97E0863	ARTWORK
97E0864	SILKSCREEN
97E0865	SOLDER MASK

DR C. WARNER	5-17-73	varian data machines /a varian subsidiary 2722 michelson drive / irvine / california / 92664
CHK W. Brown	5-29-73	
DSGN		TITLE: LOGIC DIAGRAM - PRIORITY INTERRUPT MODULE, DM 398
ENGR T. E. Hanson	6/15/73	
APPD [signature]	6/15/73	
APPD		

CODE IDENT NO.	SIZE	DWG NO	REV
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SCALE			SHEET 1.0 OF

REVISIONS					
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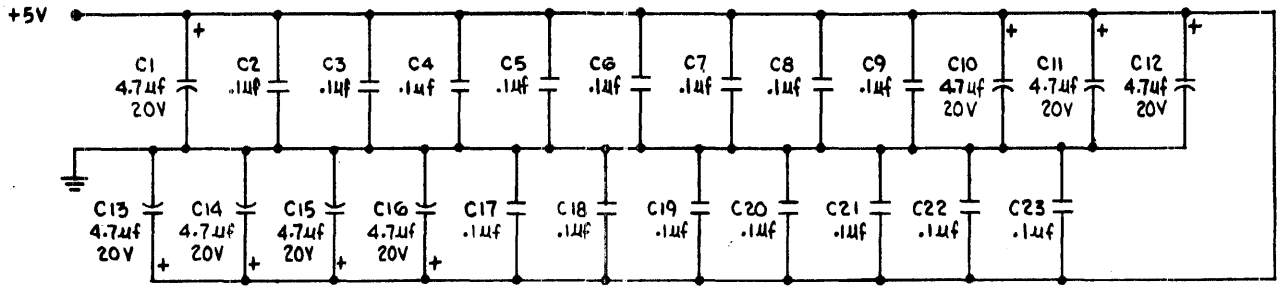
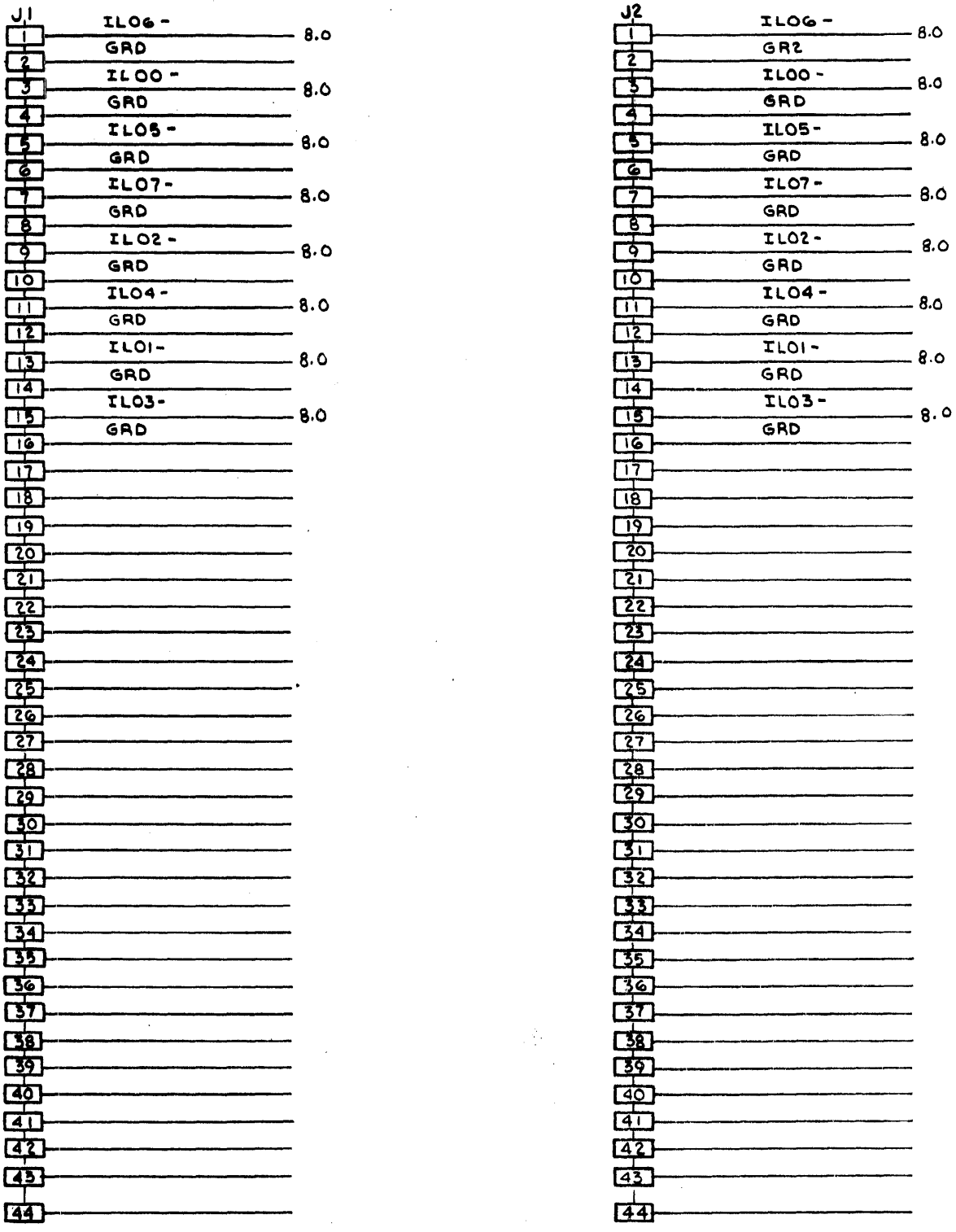
—	A		PRODUCTION RELEASE PER EN 82099		
—	—		ADDED WIRING TABLE & NOTES 1 & 2 TO SHT 5 PER EN 83034		

TABLE OF CONTENTS



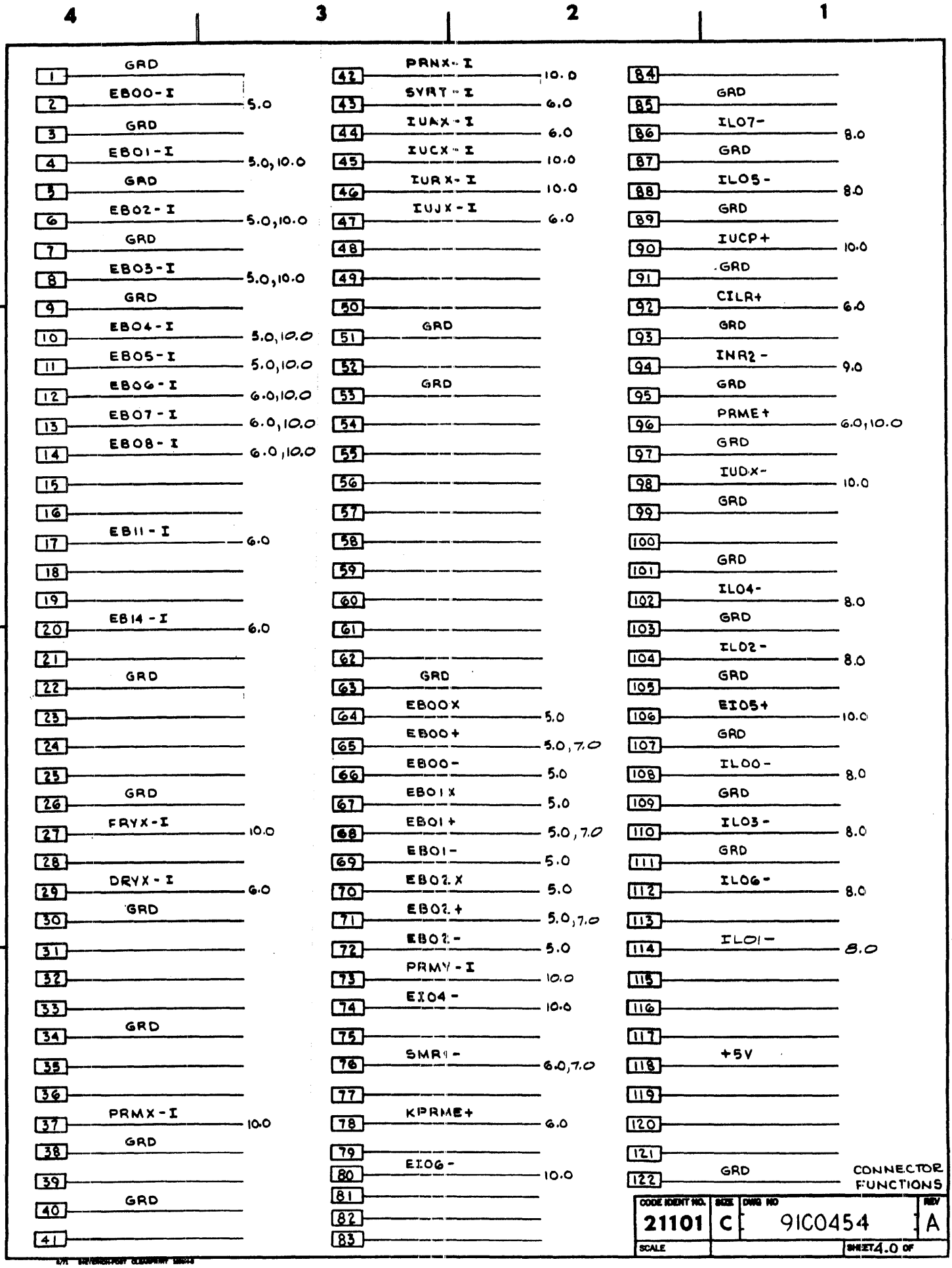
DECOUPLING, TABLE OF CONTENTS, & REVISIONS

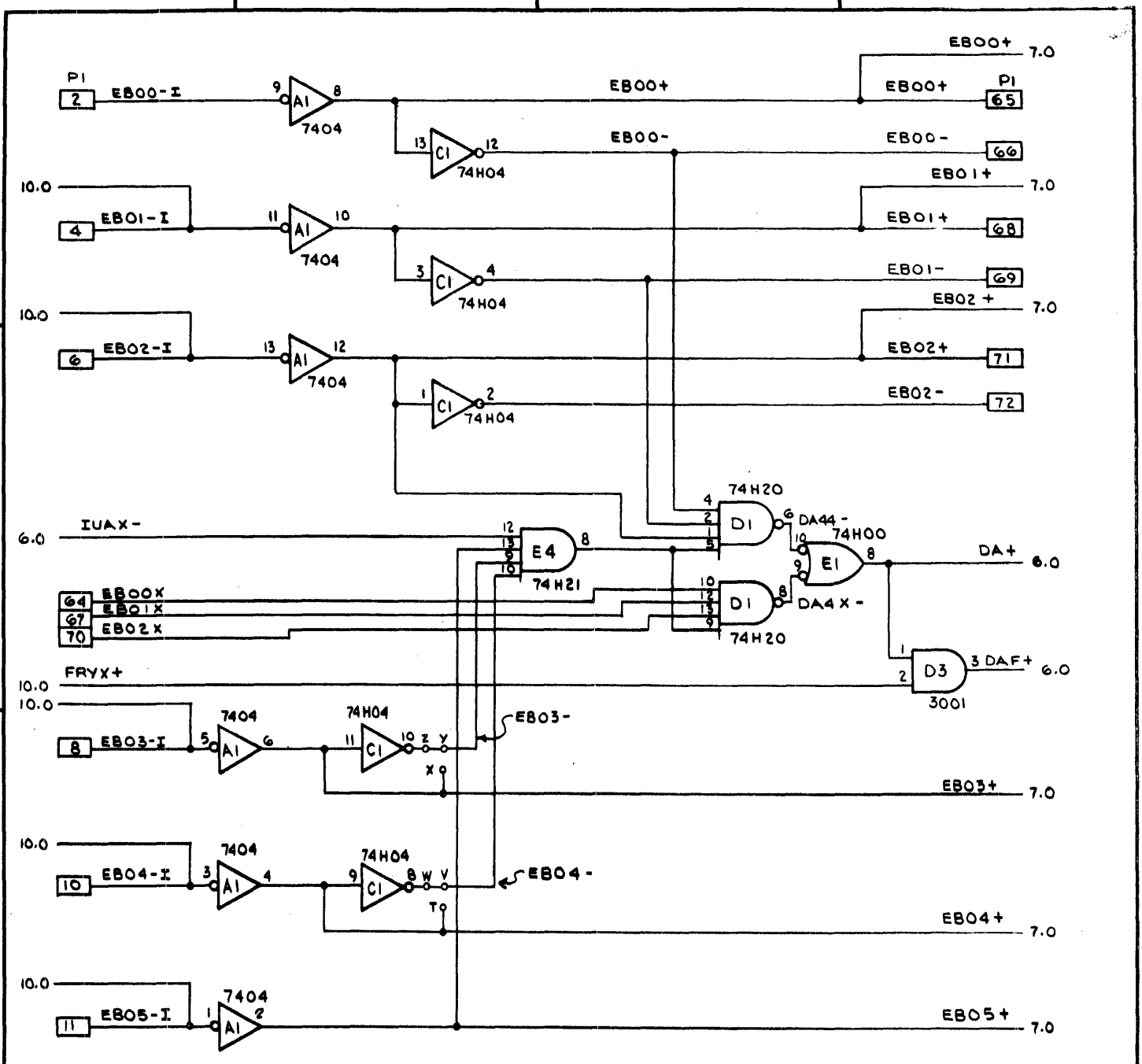
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100454	A
SCALE		SHEET 2.0 OF	



CONNECTOR FUNCTIONS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9100454	A
SCALE		SHEET 3.0 OF	


4
3
2
1
D
C
B
A
1 GRD
2 EB00-I 5.0
3 GRD
4 EB01-I 5.0,10.0
5 GRD
6 EB02-I 5.0,10.0
7 GRD
8 EB03-I 5.0,10.0
9 GRD
10 EB04-I 5.0,10.0
11 EB05-I 5.0,10.0
12 EB06-I 6.0,10.0
13 EB07-I 6.0,10.0
14 EB08-I 6.0,10.0
15
16
17 EB11-I 6.0
18
19
20 EB14-I 6.0
21
22 GRD
23
24
25
26 GRD
27 FRYX-I 10.0
28
29 DRYX-I 6.0
30 GRD
31
32
33
34 GRD
35
36
37 PRMX-I 10.0
38 GRD
39
40 GRD
41
42 PRNX-I 10.0
43 SYRT-I 6.0
44 IUAX-I 6.0
45 IUCX-I 10.0
46 IURX-I 10.0
47 IUJX-I 6.0
48
49
50
51 GRD
52
53 GRD
54
55
56
57
58
59
60
61
62
63 GRD
64 EB00X 5.0
65 EB00+ 5.0,7.0
66 EB00- 5.0
67 EB01X 5.0
68 EB01+ 5.0,7.0
69 EB01- 5.0
70 EB02X 5.0
71 EB02+ 5.0,7.0
72 EB02- 5.0
73 PRMY-I 10.0
74 EI04- 10.0
75
76 SMR1- 6.0,7.0
77
78 KPRME+ 6.0
79
80 EI06- 10.0
81
82
83
84
85 GRD
86 IL07- 8.0
87 GRD
88 IL05- 8.0
89 GRD
90 IUCP+ 10.0
91 GRD
92 CILR+ 6.0
93 GRD
94 INR2- 9.0
95 GRD
96 PRME+ 6.0,10.0
97 GRD
98 IUDX- 10.0
99 GRD
100
101 GRD
102 IL04- 8.0
103 GRD
104 IL02- 8.0
105 GRD
106 EI05+ 10.0
107 GRD
108 IL00- 8.0
109 GRD
110 IL03- 8.0
111 GRD
112 IL06- 8.0
113
114 IL01- 8.0
115
116
117
118 +5V
119
120
121
122 GRD
CONNECTOR FUNCTIONS
CODE IDENT NO. 21101
SIZE C
DWG NO 9100454
REV A
SCALE
SHEET 4.0 OF



DEVICE ADDRESS WIRING TABLE

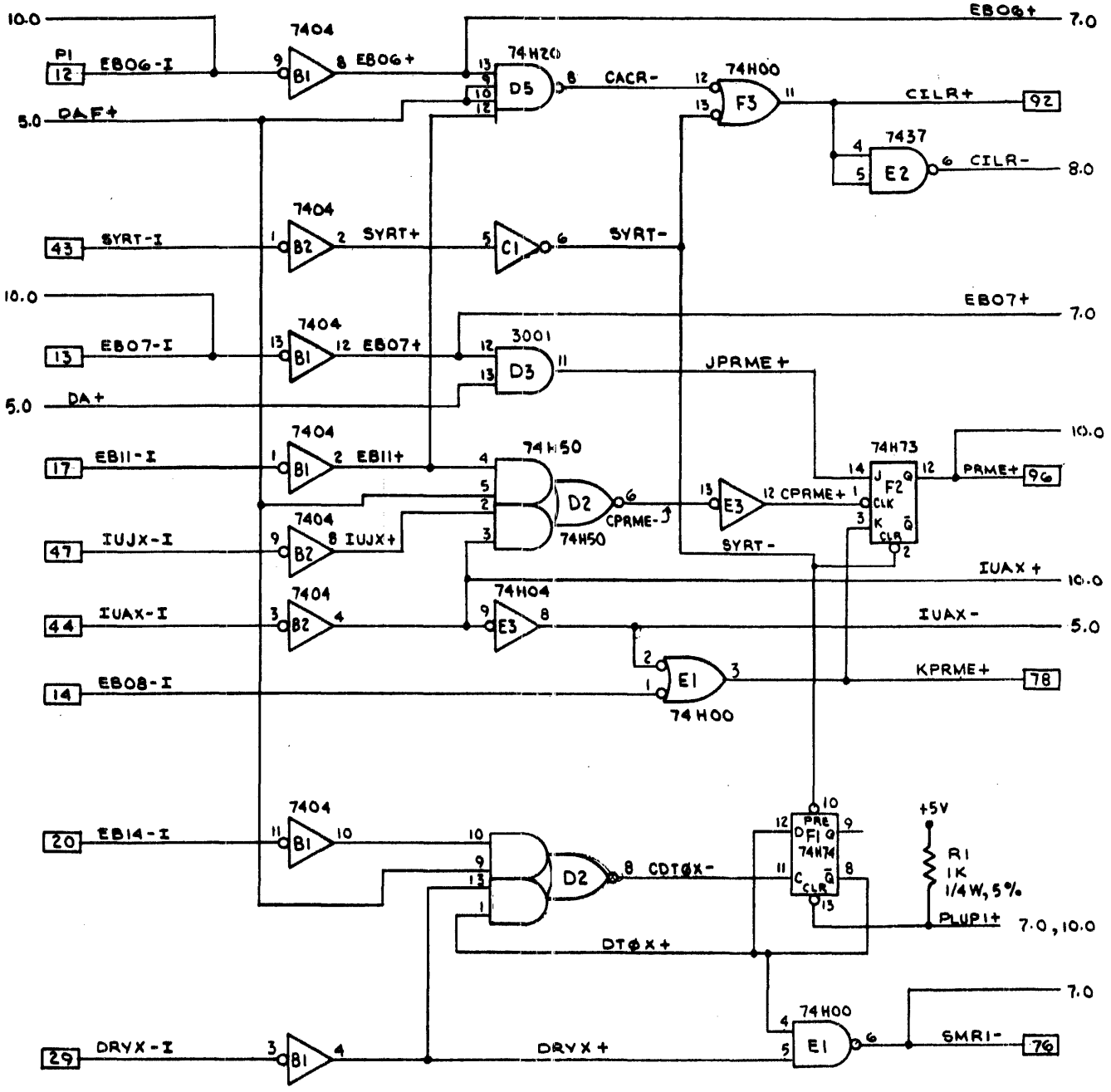
TO SELECT DEVICE ADDRESS	ADD W/W JUMPER FROM P1		
	PIN 64 TO PIN	PIN 67 TO PIN	PIN 70 TO PIN
40	66	69	72
41	68	69	72
42	66	68	72
43	68	68	72
44	66	69	71
45	65	69	71
46	66	68	71
47	65	68	71

2. TO INSTALL A NEW PIM(44P0688) IN PLACE OF AN OLD STYLE PIM(44P0172), REMOVE ENTIRE WIRE WRAP STRING(IF ANY) BETWEEN PIN 68 AND ANY OF THE FOLLOWING PINS: 66, 69 AND 72.

1. MAKE NO CONNECTION TO PIN 68 FOR DEVICE ADDRESSING

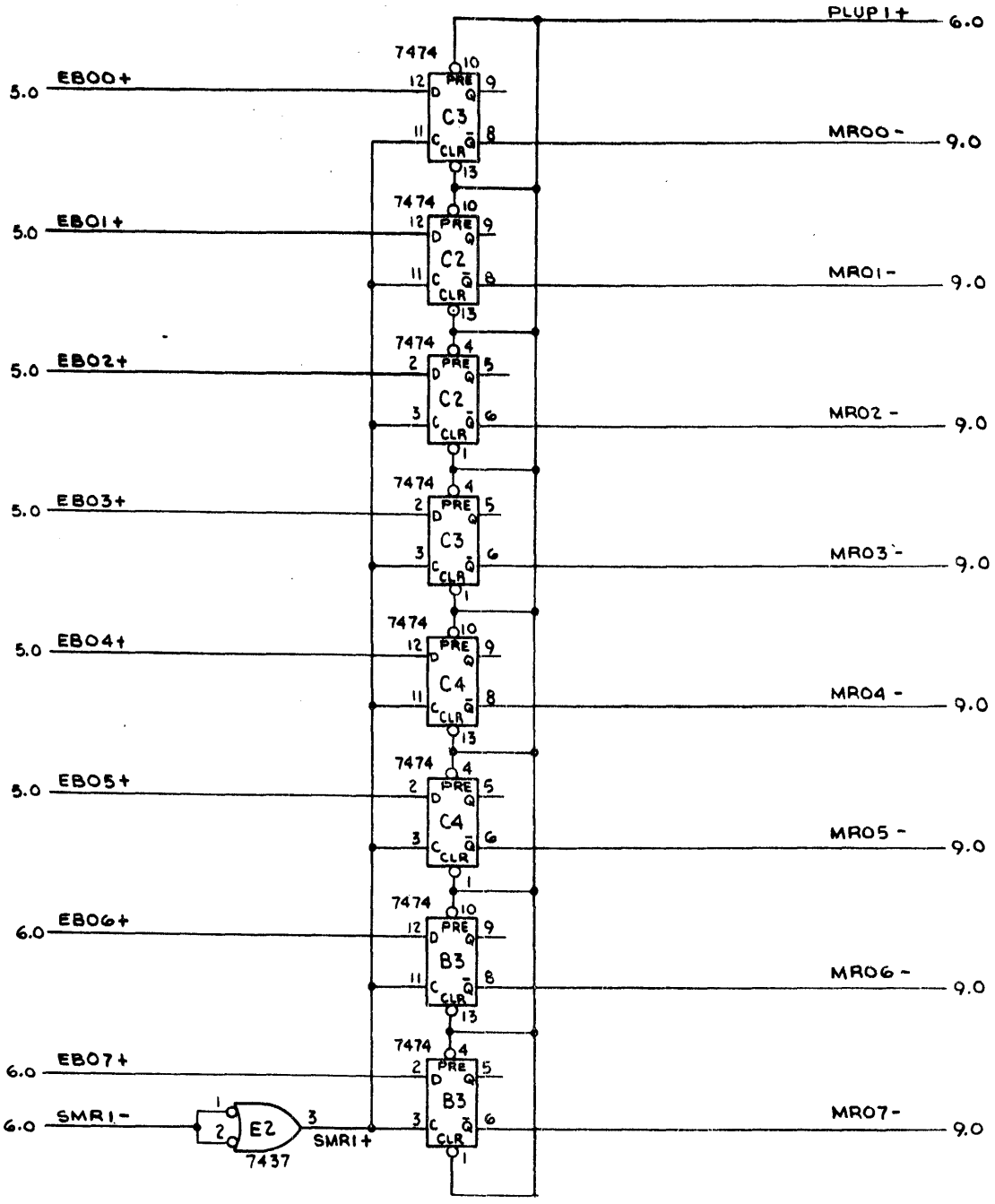
E-BUS RECEIVERS & DEVICE ADDRESS DECODE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0454	A
SCALE		SHEET 5.0 OF	



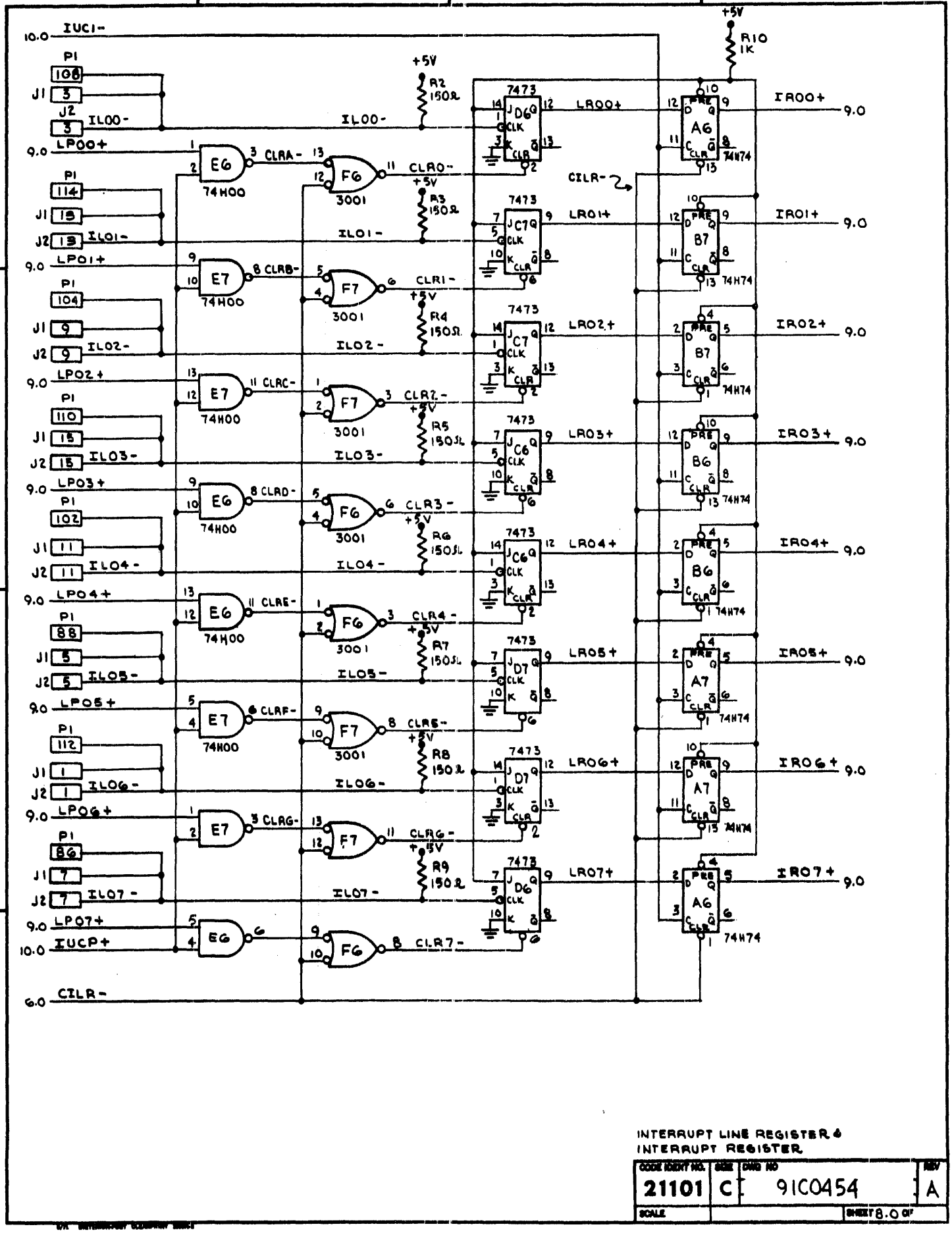
E-BUS RECEIVERS & CONTROL LOGIC

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0454	A
SCALE			SHEET 6.0 OF



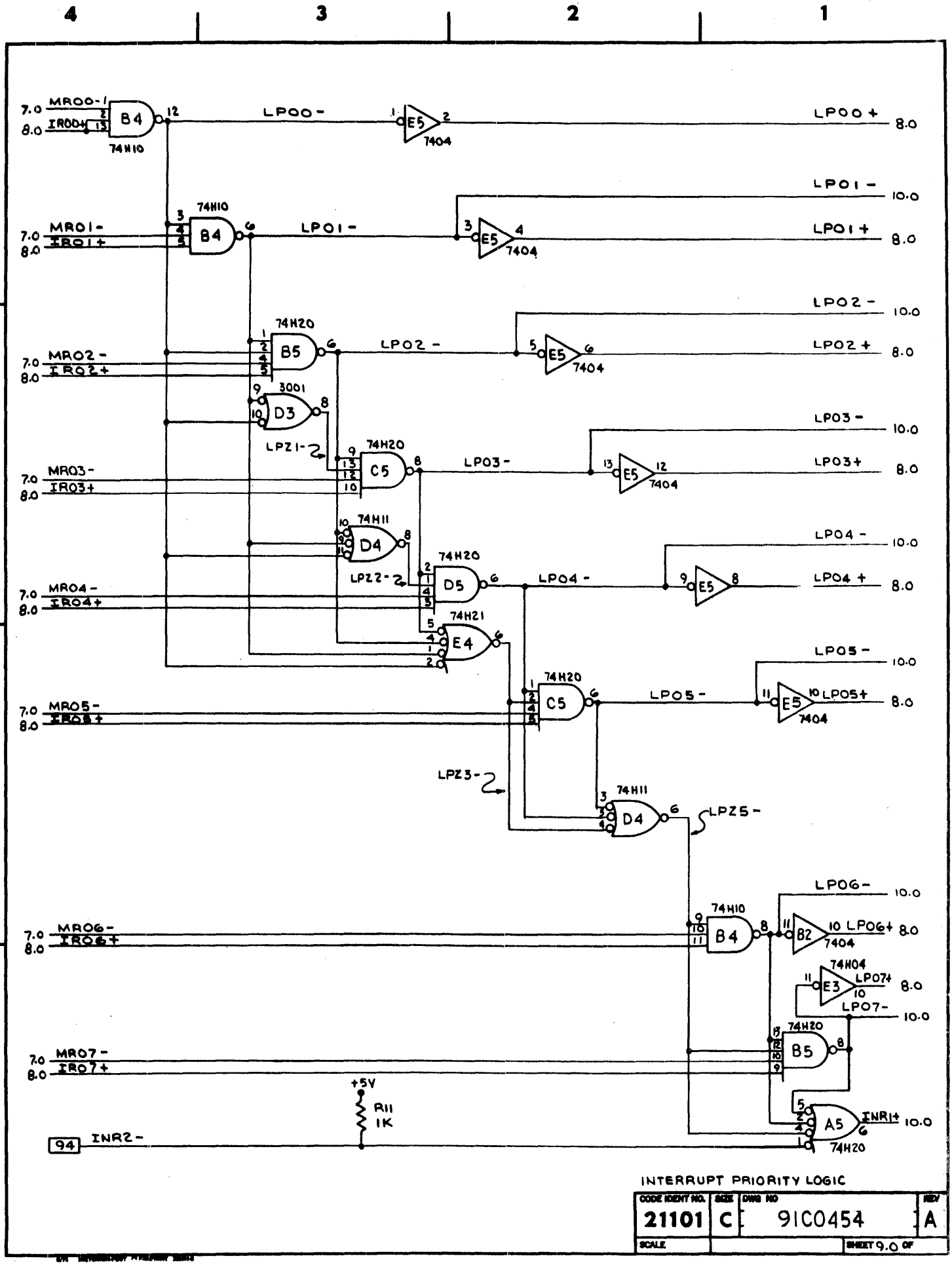
INTERRUPT MASK REGISTER

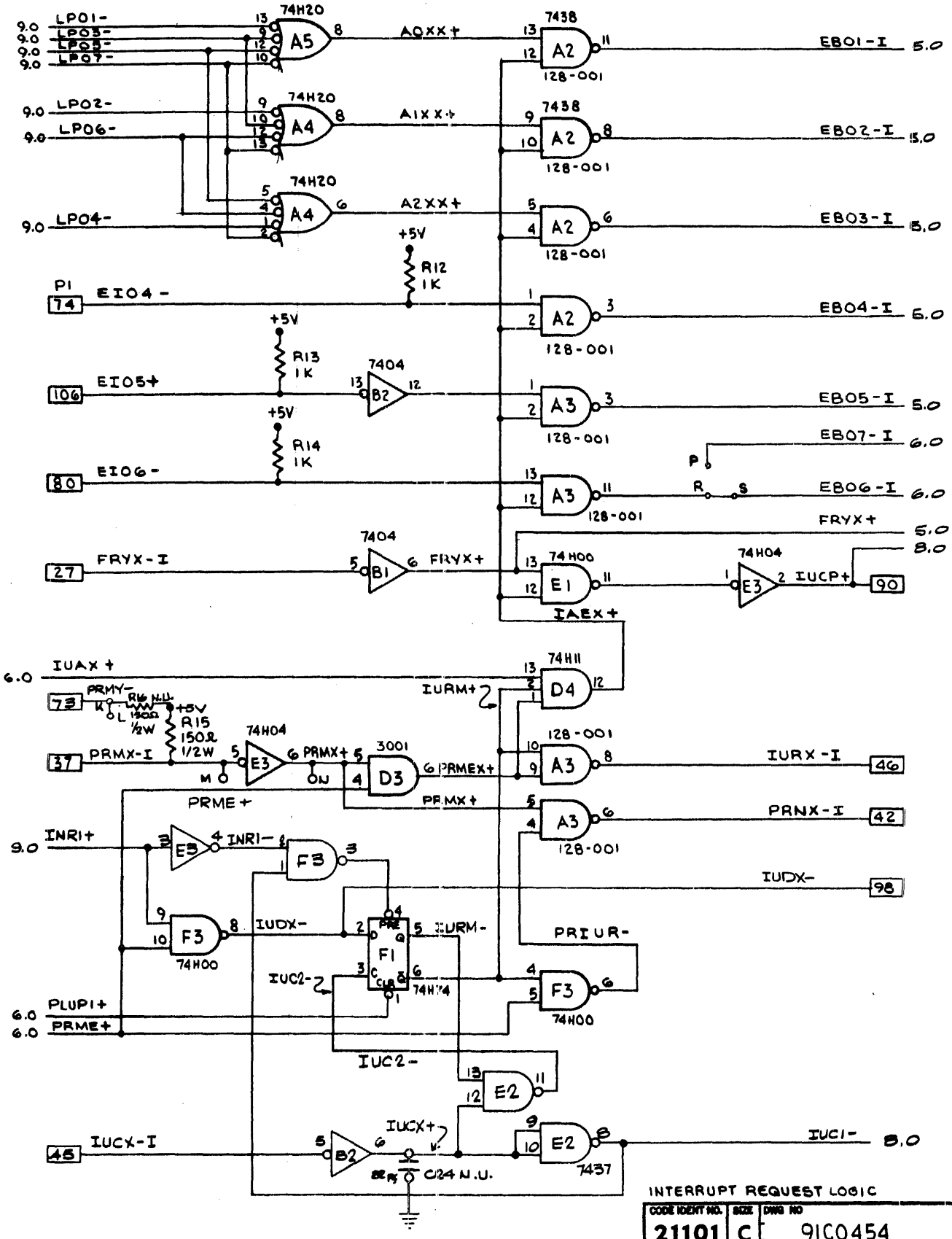
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0454	A
SCALE			SHEET 7.0 OF

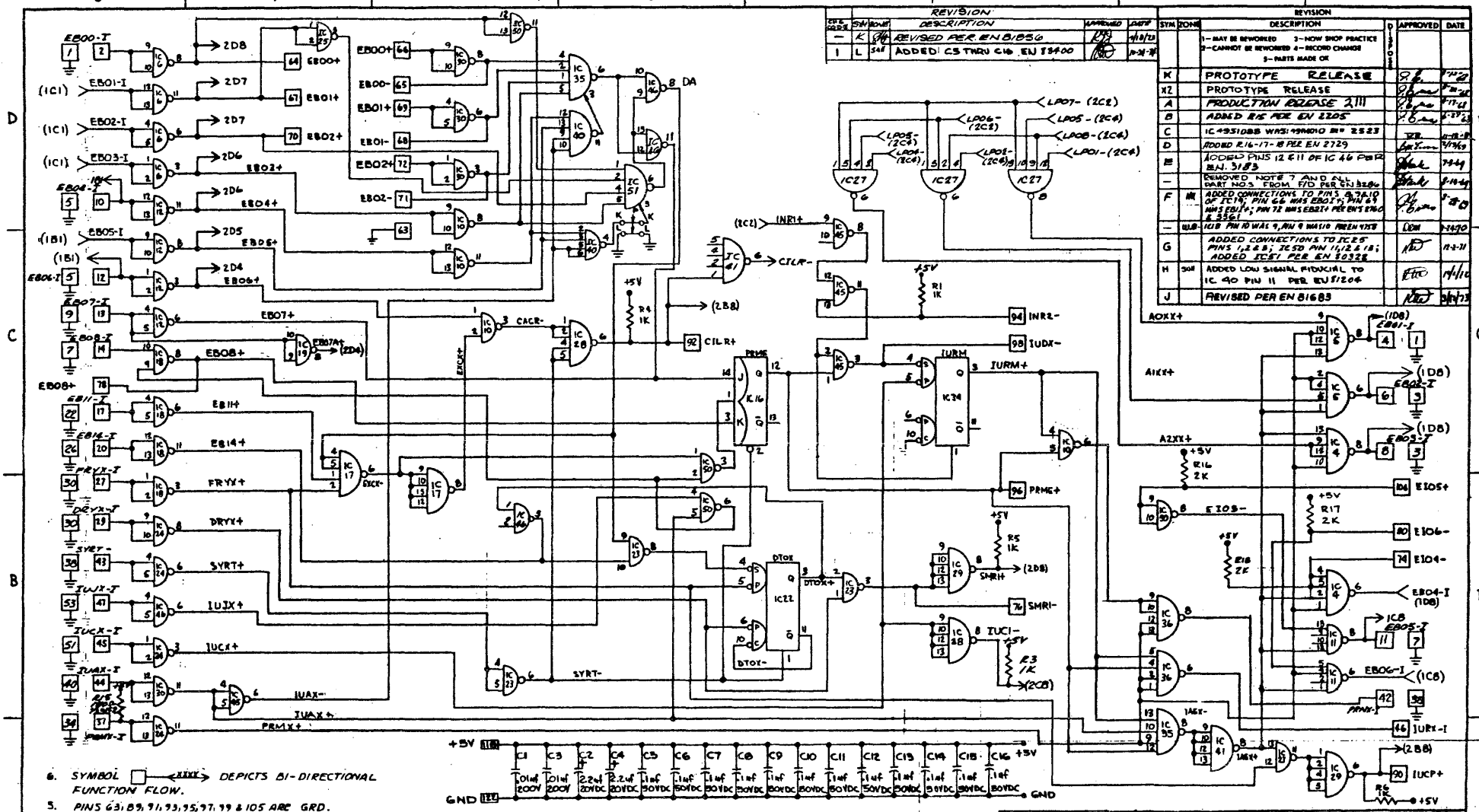


INTERRUPT LINE REGISTER &
INTERRUPT REGISTER

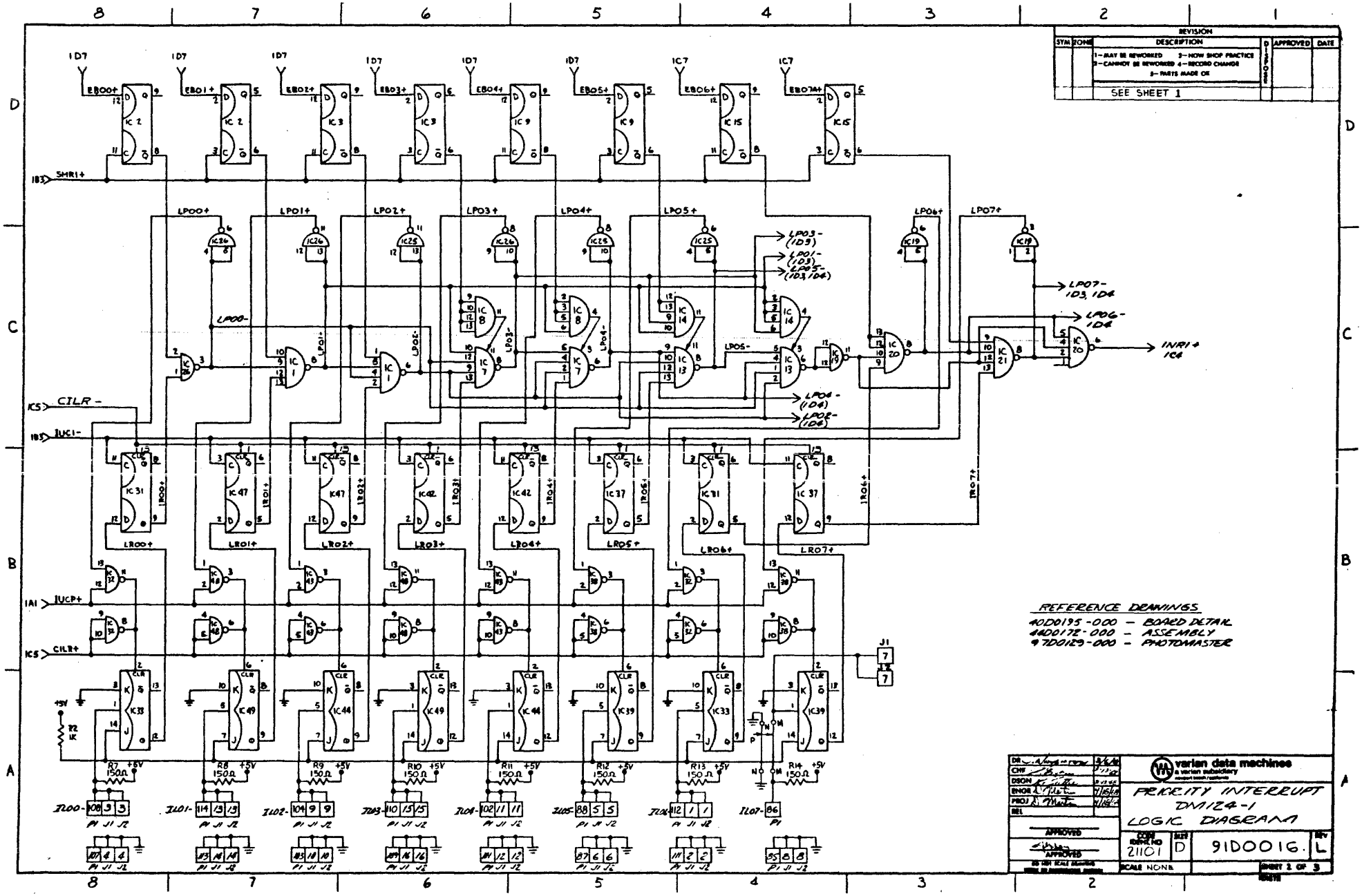
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9IC0454	A
SCALE			SHEET 8.0 OF

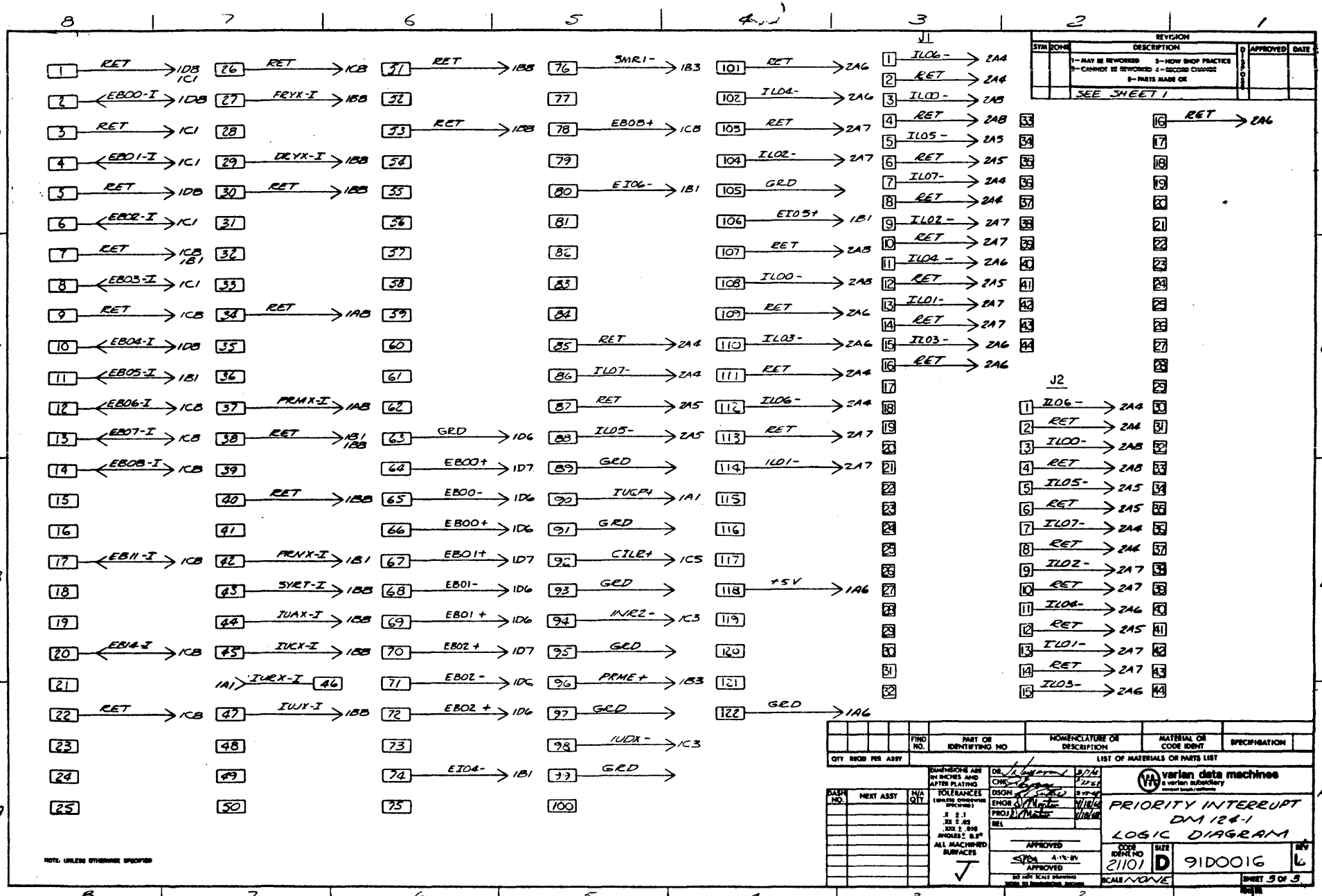

4
3
2
1
D
C
B
A
7.0 MR00-1
8.0 IR00+
B4
74H10
LP00-
E5
7404
LP00+
8.0
LP01-
10.0
MR01-
IR01+
LP01-
LP01+
LP02-
MR02-
IR02+
B5
74H20
LP02-
LP02+
3001
D3
LPZ1-2
MR03-
IR03+
C5
LP03-
LP03+
D4
74H11
LP04-
LPZ2-2
MR04-
IR04+
D5
LP04-
LP04+
E4
74H21
LP05-
MR05-
IR05+
LP05-
LP05+
LPZ3-2
LPZ5-
LP06-
MR06-
IR06+
LP06+
74H04
E3
LP07+
LP07-
MR07-
IR07+
+5V
R11
1K
94
INR2-
A5
INR1+
INTERRUPT PRIORITY LOGIC
CODE IDENT NO. 21101
SIZE C
DWG NO 91C0454
REV A
SCALE
SHEET 9.0 OF


LPO1-
LPO3-
LPO5-
LPO7-
LPO2-
LPO6-
LPO4-
74H20
A5
A4
A4
AOXX+
A1XX+
A2XX+
7438
A2
128-001
EBO1-I
EBO2-I
EBO3-I
+5V
R12
1K
P1
74
EIO4-
EBO4-I
R13
1K
7404
B2
106
EIO5+
EBO5-I
R14
1K
80
EIO6-
EBO7-I
EBO6-I
P
R
S
FRYX+
27
FRYX-I
B1
74H00
E1
74H04
E3
IUCP+
90
IAEX+
IUAX+
6.0
74H11
D4
IURM+
PRMY-
R16 1KΩ
1/2W
R15
150Ω
1/2W
37
PRMX-I
3001
D3
PRMEX+
PRMX+
IURX-I
46
PRME+
PRNX-I
42
INRI+
9.0
E3
INRI-
F3
IUDX-
98
F1
74H74
IUDX-
IURM-
PRIUR-
IUC2-
PLUP1+
6.0
PRME+
6.0
E2
IUC2-
IUCX+
45
IUCX-I
B2
C24 N.U.
7437
IUC1-
8.0
INTERRUPT REQUEST LOGIC
CODE IDENT NO.
21101
SIZE
C
DWG NO
9IC0454
REV
A
SCALE
SHEET 10.0 OF



6. SYMBOL □ <XXXX> DEPICTS BI-DIRECTIONAL FUNCTION FLOW.
5. PINS 63, 89, 91, 93, 95, 97, 99 & 105 ARE GRD.
4. POWER DISTRIBUTION TO IC 16, 33, 39, 44 & 49 PIN 4 = +5V, PIN 11 = GND.
3. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GND, (EXCEPTIONS NOTE 4).
2. ALL RESISTORS ARE 1/4W ±5%.
1. THE SYMBOLS XXY ——→ AND ←—— INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.


REVISION
SEE SHEET 1
REFERENCE DRAWINGS
40D0195-000 - BOARD DETAIL
44D0172-000 - ASSEMBLY
97D0129-000 - PHOTOMASTER
varian data machines
PRIORITY INTERRUPT
DMI24-1
LOGIC DIAGRAM
91D0016.
SCALE NONE
SHEET 2 OF 3


1 RET → 1D8 1C1
2 EB00-I → 1D8
3 RET → 1C1
4 EB01-I → 1C1
5 RET → 1D8
6 EB02-I → 1C1
7 RET → 1C8 1B1
8 EB03-I → 1C1
9 RET → 1C8
10 EB04-I → 1D8
11 EB05-I → 1B1
12 EB06-I → 1C8
13 EB07-I → 1C8
14 EB08-I → 1C8
15
16
17 EB11-I → 1C8
18
19
20 EB14-I → 1C8
21
22 RET → 1C8
23
24
25
26 RET → 1C8
27 FRYX-I → 1B8
28
29 DRYX-I → 1B8
30 RET → 1B8
31
32
33
34 RET → 1A8
35
36
37 PRMX-I → 1A8
38 RET → 1B1 1B8
39
40 RET → 1B8
41
42 PRNX-I → 1B1
43 SYET-I → 1B8
44 IUAX-I → 1B8
45 IUCX-I → 1B8
1A1 IUAX-I 46
47 IUJX-I → 1B8
48
49
50
51 RET → 1B8
52
53 RET → 1D8
54
55
56
57
58
59
60
61
62
63 GRD → 1D6
64 EB00+ → 1D7
65 EB00- → 1D6
66 EB00+ → 1D6
67 EB01+ → 1D7
68 EB01- → 1D6
69 EB01+ → 1D6
70 EB02+ → 1D7
71 EB02- → 1D6
72 EB02+ → 1D6
73
74 EI04- → 1B1
75
76 SMR1- → 1B3
77
78 EB08+ → 1C8
79
80 EI06- → 1B1
81
82
83
84
85 RET → 2A4
86 IL07- → 2A4
87 RET → 2A5
88 IL05- → 2A5
89 GRD →
90 IUCP4 → 1A1
91 GRD →
92 CILR+ → 1C5
93 GRD →
94 INR2- → 1C3
95 GRD →
96 PRME+ → 1B3
97 GRD →
98 IUDX- → 1C3
99 GRD →
100
101 RET → 2A6
102 IL04- → 2A6
103 RET → 2A7
104 IL02- → 2A7
105 GRD →
106 EI05+ → 1B1
107 RET → 2A8
108 IL00- → 2A8
109 RET → 2A6
110 IL03- → 2A6
111 RET → 2A4
112 IL06- → 2A4
113 RET → 2A7
114 IL01- → 2A7
115
116
117
118 +5V → 1A6
119
120
121
122 GRD → 1A6
J1
1 IL06- → 2A4
2 RET → 2A4
3 IL00- → 2A8
4 RET → 2A8
5 IL05- → 2A5
6 RET → 2A5
7 IL07- → 2A4
8 RET → 2A4
9 IL02- → 2A7
10 RET → 2A7
11 IL04- → 2A6
12 RET → 2A5
13 IL01- → 2A7
14 RET → 2A7
15 IL03- → 2A6
16 RET → 2A6
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
J2
1 IL06- → 2A4
2 RET → 2A4
3 IL00- → 2A8
4 RET → 2A8
5 IL05- → 2A5
6 RET → 2A5
7 IL07- → 2A4
8 RET → 2A4
9 IL02- → 2A7
10 RET → 2A7
11 IL04- → 2A6
12 RET → 2A5
13 IL01- → 2A7
14 RET → 2A7
15 IL03- → 2A6
16 RET → 2A6
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
SEE SHEET 1
REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1-MAY BE REWORKED 3-NEW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
NOTE: UNLESS OTHERWISE SPECIFIED
FIND NO. PART OR IDENTIFYING NO NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT SPECIFICATION
QTY REQD PER ASSY LIST OF MATERIALS OR PARTS LIST
DASH NO. NEXT ASSY N/A QTY
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES
ALL MACHINED SURFACES
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING
varian data machines a varian subsidiary
PRIORITY INTERRUPT DM 124-1 LOGIC DIAGRAM
CODE IDENT NO 21101
SIZE D
91D0016
REV L
SCALE NONE
SHEET 5 OF 5