DWG NO. 98A0887

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NEXT ASSEMBLY

MODEL NO. V70 SERIES

varian data machines / a varian subsidiary
2722 michelson drive / irvine / california / 92664

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DSGN	———	—
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ND	A.WHITCOMB	8/1/73

CODE IDENT NO. 21101

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TITLE

V70 SERIES MICRO WORD FLOWCHARTS

SIZE	DWG NO.	REV
A	98A0887	B

SHEET 1 OF 57

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SECTION 1
INTRODUCTION

1.1 Purpose

The function of this document is to provide microprogram information describing the standard V70 series "macro" instruction on set. This instruction set is implemented in page zero of the control store (512 words of Read-only memory), and is designed to emulate the 620F instruction set a maximum performance level. For a description of this standard instruction set, see the V70 series handbooks (V72, V73, or V74 System Handbooks).

Although the V70 series "macro" instruction set is fixed, pages of 256 or 512 words of user definable control store (random access memories) may be added, via a "Writable Control Store Option", thus allowing for user defined "macro" and "micro" instructions on programs in a second environment. For information about the Writable Control Store Option, see the WCS manual (98A9906-08X).

1.2 Performance Specifications

The use of high speed logic; and read-only memory, allows for a micro-exicution time of 165 nanoseconds. This high speed micro-exicution time results in very efficient use of existing system resources, such as semiconductor memory with a cycle time of 330 nanoseconds (or two micro-instructions).

1.3 Reference Documents

For further information concerning V70 Series hardware and micro-programming refer to the following documents:

Title	Document Number
Writable Control Store Manual	98A9906-08X
V70 Series Processor Manual	98A9906-02X
V73 System Handbook	98A9906-01X
Varian Microprogramming Guide	98A9906-07X
Core Memory Manual	98A9906-03X
Semiconductor Memory	98A9906-04X
Option Board Manual	98A9906-05X
Power Supply Manual	98A9906-06X

SECTION 2
FUNCTIONAL DESCRIPTION

2.1 Flowchart Definitions

Flowchart definitions will consist of explanations for memory operation, control store addressing, data loop operations, and the use of processor flags. Included are examples of several types of operations performed in the flow diagrams to follow.

2.1.1 Memory Operations

When memory operations are to be performed, or initiated by a micro-command, a statement of the type of memory operation to be performed, as well as the sources and/or destinations for memory data and address, will be made. An example is given below:

Example: A.F. @ A, M = address fetch with ALU as address and MIL as the fetched data's destination.

2.1.1.1 Type of operations:

a. I.F. = instruction fetch

b. A.F. = address fetch

c. O.F. = opened fetch

d. O.S. or STO = store

e. Cond. = conditional memory initiation (condition specified by ◇).

2.1.1.2 Memory Address Sources:

a. P = program counter to memory address

b. A = ALU output to memory address

c. M = memory input latch (MIL register) to memory address

2.1.1.3 Memory Fetch Destinations:

a. I = MII and MIL register - data from memory is to be loaded into both the instruction buffer register (MII) and the memory input latch (MIL).

b. M = MIL register - data from memory is to be loaded into the memory input latch (MIL).

2.1.2 Field Selection

The operation of selecting and decoding up to a five bit field from the instruction register (C21), for use in control store branching operations, is known as field selecting. Field selecting can only take place from the instruction register - C21. Field Selection statements will appear as follows:

F. Sel I (00-02) or Fld Sel. 0-2 - Field selection from the instruction register (C21) bits 0 thru 2.

2.1.3 Data Loop Operations

When data loop operations are performed, statement describing the action taking place will occur. Examples are given below:

a. P + 1 → S1 - program register added to 1 and transferred to the S1 register.

b. A → DOR - The contents of the A-register are transferred to the Data Loop Operand register.

2.1.4 Instruction Register Transfer

Instruction register transfers are labeled as below:

Statement: I1 → I2 = M11 → C21 = transfer contents of instruction buffer (M11) to the instruction register (C21).

2.1.5 Flags

Several Flags are used for storing and testing the status of the machine A few are listed below:

a. Statement = operation on the interrupt flag, CINTF.
Example = RST CINTF - reset the interrupt flag.

b. Statement = Ofl., Ovrfl - overflow indicator

c. Statement = DSB - a utility flip-flop used to provide temporary storage of data or control information during the execution of various instructions.

2.1.6 Other Terms

Other terms used with the micro-flow are given in Table 1. See Sheet 7.

TABLE I

FLOWCHART DEFINITIONS

EXPRESSION	INTERPRETATION
Mem. Strt.	Memory start. A memory operation is being initiated.
Incr. P	Increment the Program Counter by one.
0 → DOR	The contents of the Data Loop Operand Register are set to zero.
A → DOR	The contents of the A Register are transferred to the Data Loop Operand Register.
AVB → DOR	The contents of the A and B Registers are inclusively OR'ed and are transferred to DOR.
Cond.	Conditional. Used to denote that the execution of a specific operation is dependent upon the outcome of a test being performed.
En.	Enable.
D-ROM	Instruction decoder read-only-memory.
M11	Preliminary instruction register. A buffer register used to receive all instructions from memory. This register provides input to both C21 and the D-ROM.
MDN	Memory Done. A signal which identifies the completion of a memory operation.
IDN	I/O done. A signal which identifies the completion of an I/O operation.
S1, S2	Two registers located in the Register File which are used for temporary storage of operands, addresses, etc. Also known as E (S1) and F (S2).

EXPRESSION	INTERPRETATION
Zero	A status indicator which is set during various instructions when the result of an arithmetic/logical operation is zero.
Enable "Jump" Signal.	A "Jump" signal is generated and sent to the Memory Protect option to signify that a program "jump" or "skip" operation is occurring.
Mask → DOR	The 16-bit "Mask" field of the micro-word is transferred to DOR (after inversion of each bit).
I/O Strt.	I/O Start. An I/O operation is being initiated or allowed to continue execution.
IOR	A buffer register used for temporary storage of data or control information during the execution of various I/O operations.
C21	Main instruction register. This register contains the current instruction during most of instruction execution.
CINTF	Interrupt flag. A flip-flop used to denote that an interrupt instruction execution is or has been in progress.
DOR $\xrightarrow[\text{Func}]{\text{Spec. ALU}}$ A	The contents of DOR are transferred through the adder (ALU) to the A Register. The adder operation will transfer, increment, decrement, or invert as a function of a hardware decoding of bits 6 and 7 of the current instruction.
Override Mem.	A modification to a previously initiated and current memory operation; e.g., a "Read" is modified to a "Write".
Sample Overflow	An operation in which the results of an arithmetic operation are allowed to set the Overflow Indicator if overflow conditions exist.
Mask I + P → DOR	A 16-bit word, generated by AND'ing the micro-word "Mask" field and the current instruction word (contents of C21), is added to the contents of the Program Counter. The result is placed in DOR.

EXPRESSION	INTERPRETATION
Mem. Contr.	Memory Control logic section.
MIL	A buffer register used to receive and hold operands and operand addresses from memory.
I/O Sense Flag	A flip-flop used to receive and hold the sense response bit transmitted from a device controller during a SEN instruction execution.
Intrpt.	Interrupt.

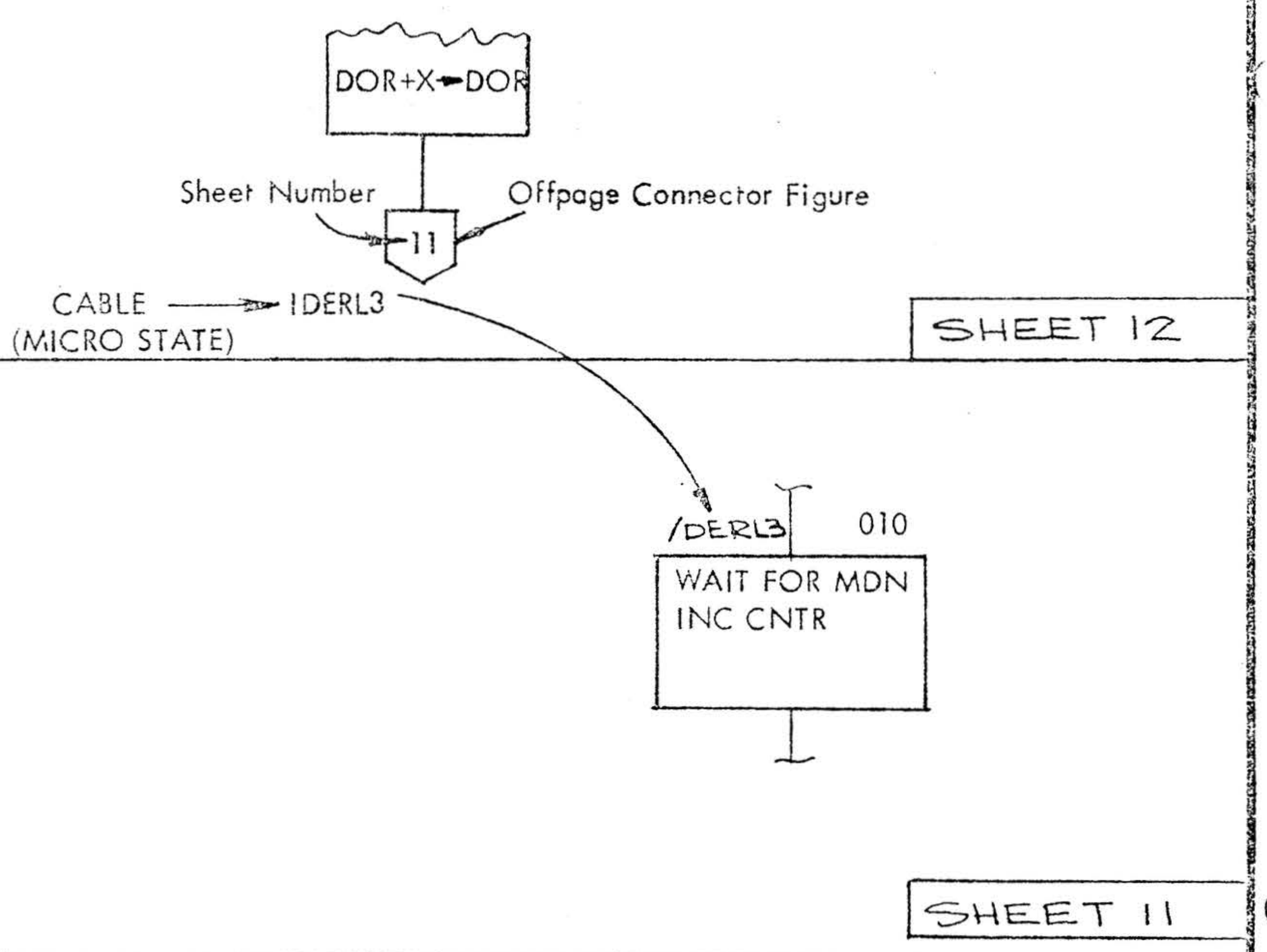
2.2 V70 Series Flowcharts

The V70 Series Flowcharts give detailed information for each class of instruction used in the standard V70 instruction set; front panel routines; interrupt routine; automatic bootstrap loader routines; V70 "Standard" micro-states; and Input/Output microflows.

For exact Binary Contents of each control store address, see listing for V70 Control Store #49A0195-000 and #49A0195-001.

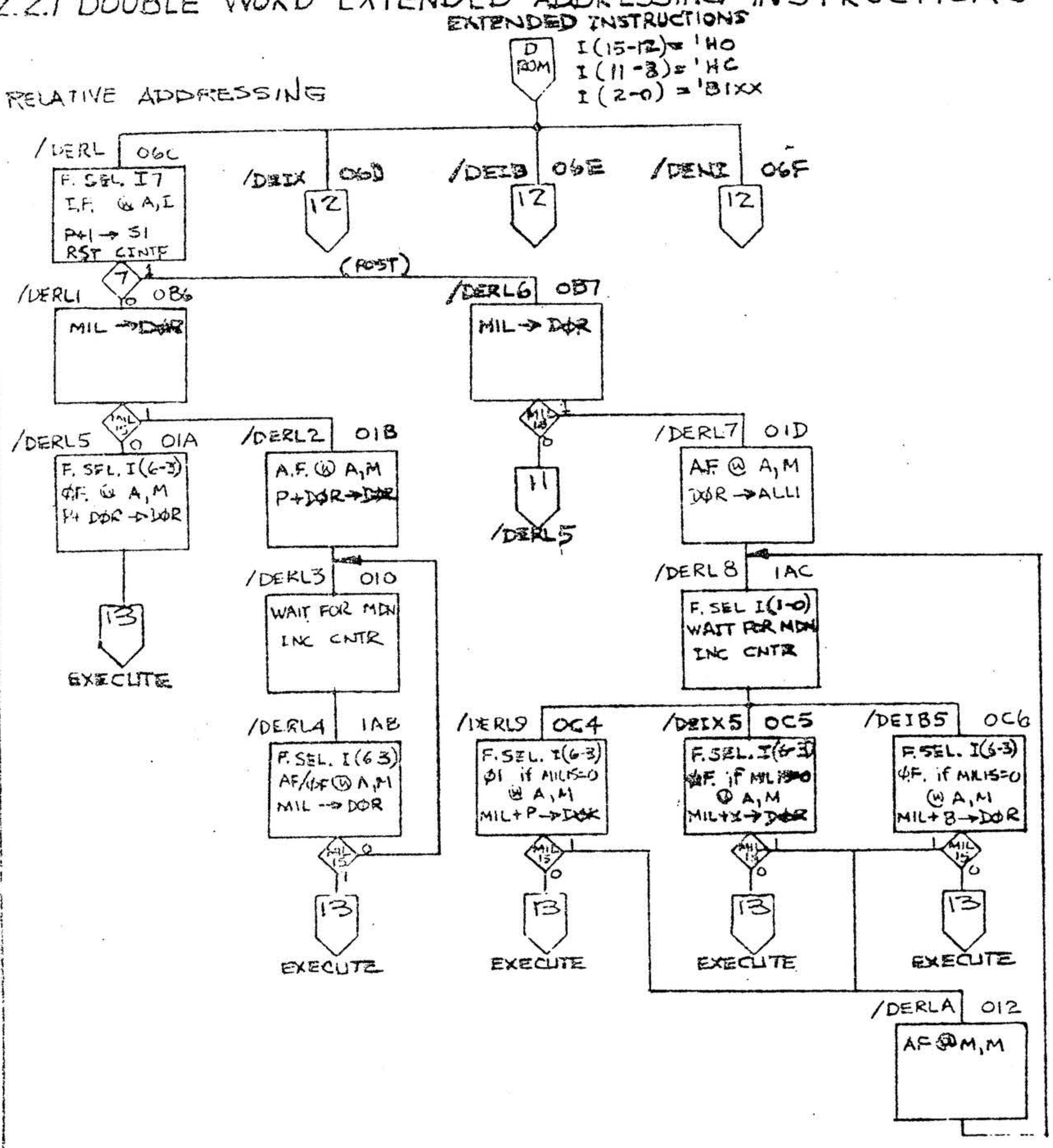
Offpage connectors are referenced by sheet number, located at bottom of each sheet (right hand side). Offpage connectors will reference to a specific Micro State, or will indicate some general operation to follow (i.e. Execute, Next Instruction, etc.). See example below.

Example:



PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

2.2.1 DOUBLE WORD EXTENDED ADDRESSING INSTRUCTIONS



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varian data machines a varian subsidiary	CODE IDENT. NO.	EXTENDED INSTRUCTIONS	98A0887	REV. B
	PREPARED BY	APPROVED BY	SHEET 11 OF 57	

PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

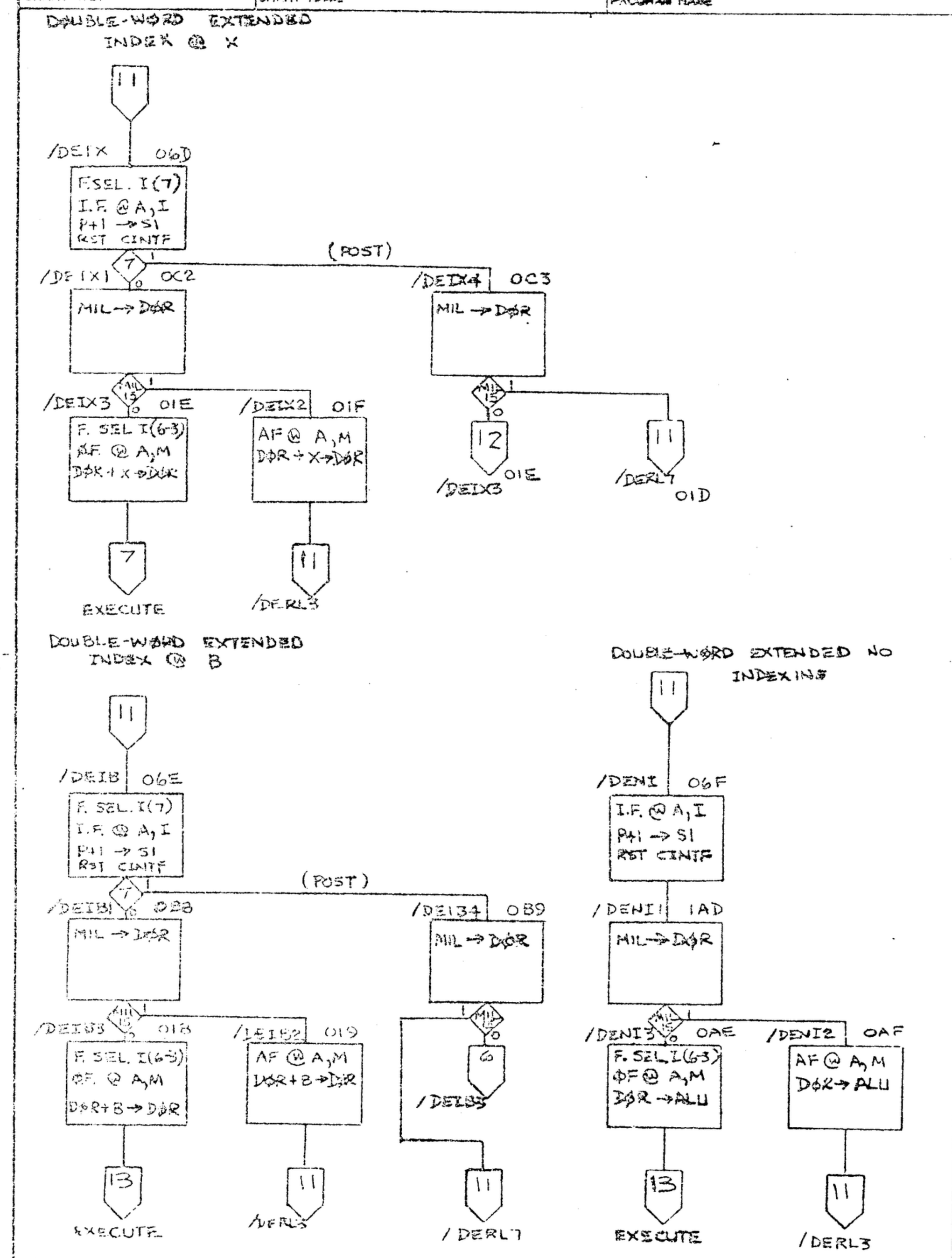

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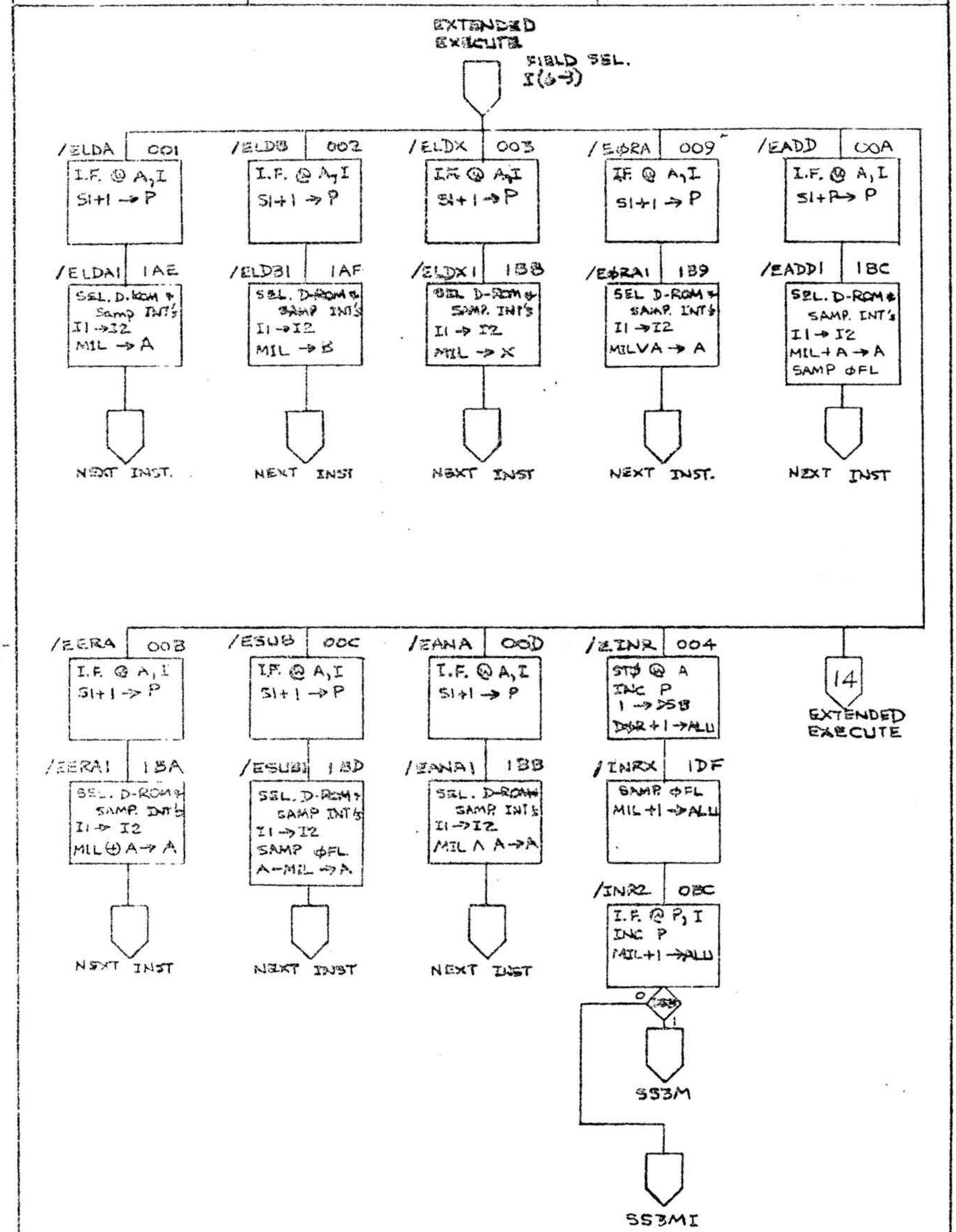
CHART I.D.	CHART NAME	PROGRAM NAME	



varian data machines a varian subsidiary	CODE IDENT. NO.	EXTENDED INSTRUCTIONS	93A0887	REV. D
	PREPARED BY	APPROVED BY	SHEET 13 OF 57	

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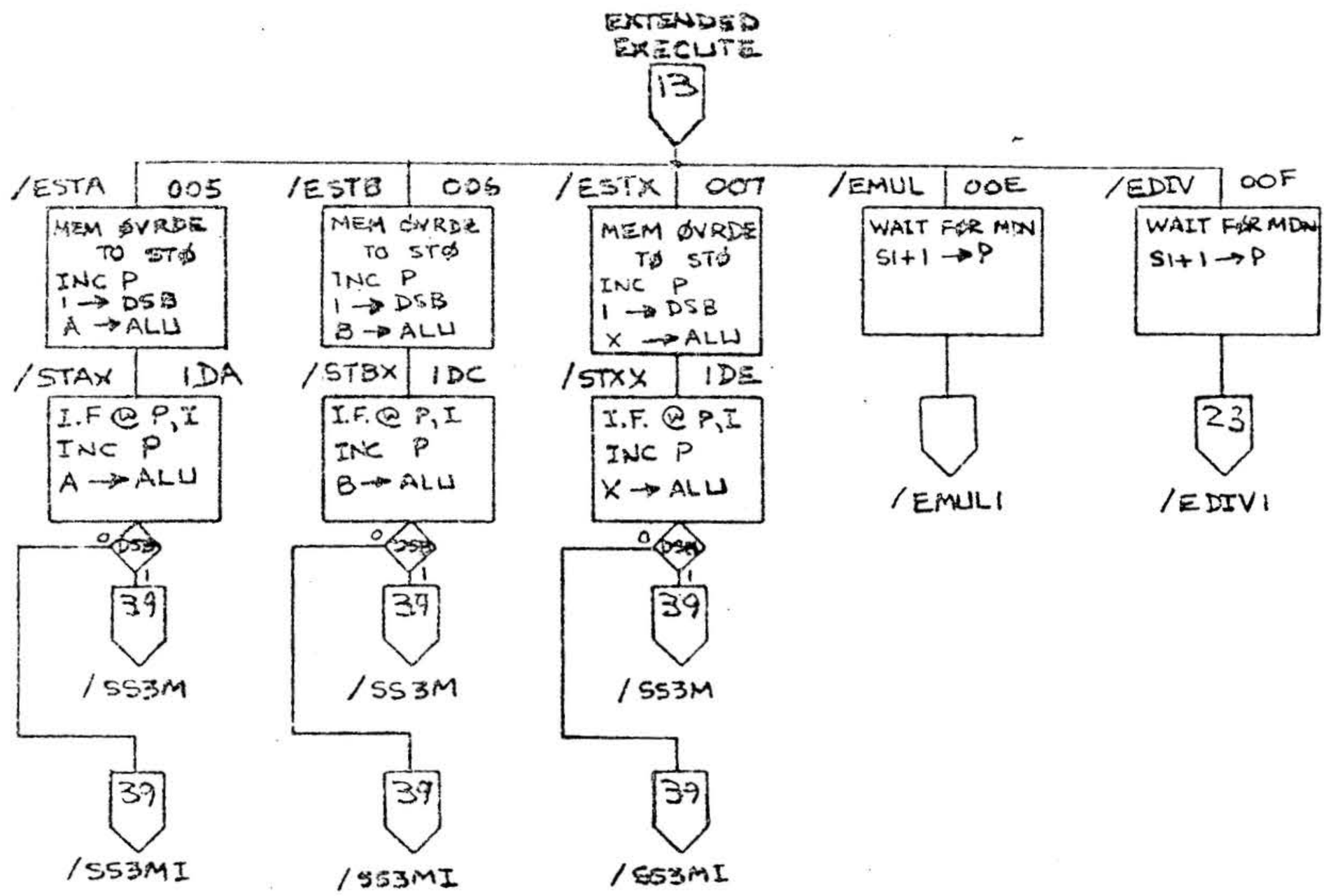

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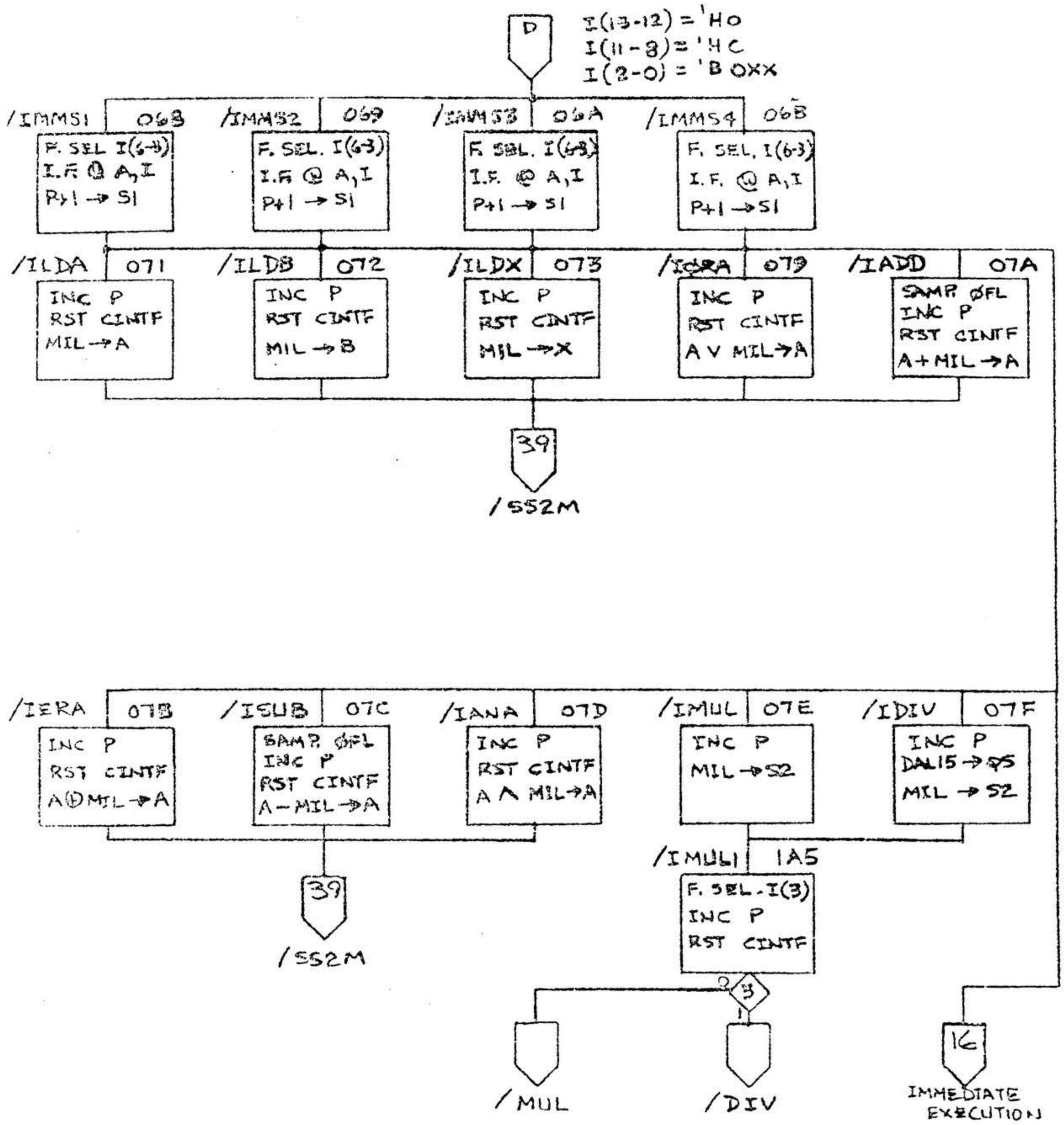
	PREPARED BY	APPROVED BY	SHEET 14 OF 57	

PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

2.2.2 DOUBLE WORD IMMEDIATE INSTRUCTION



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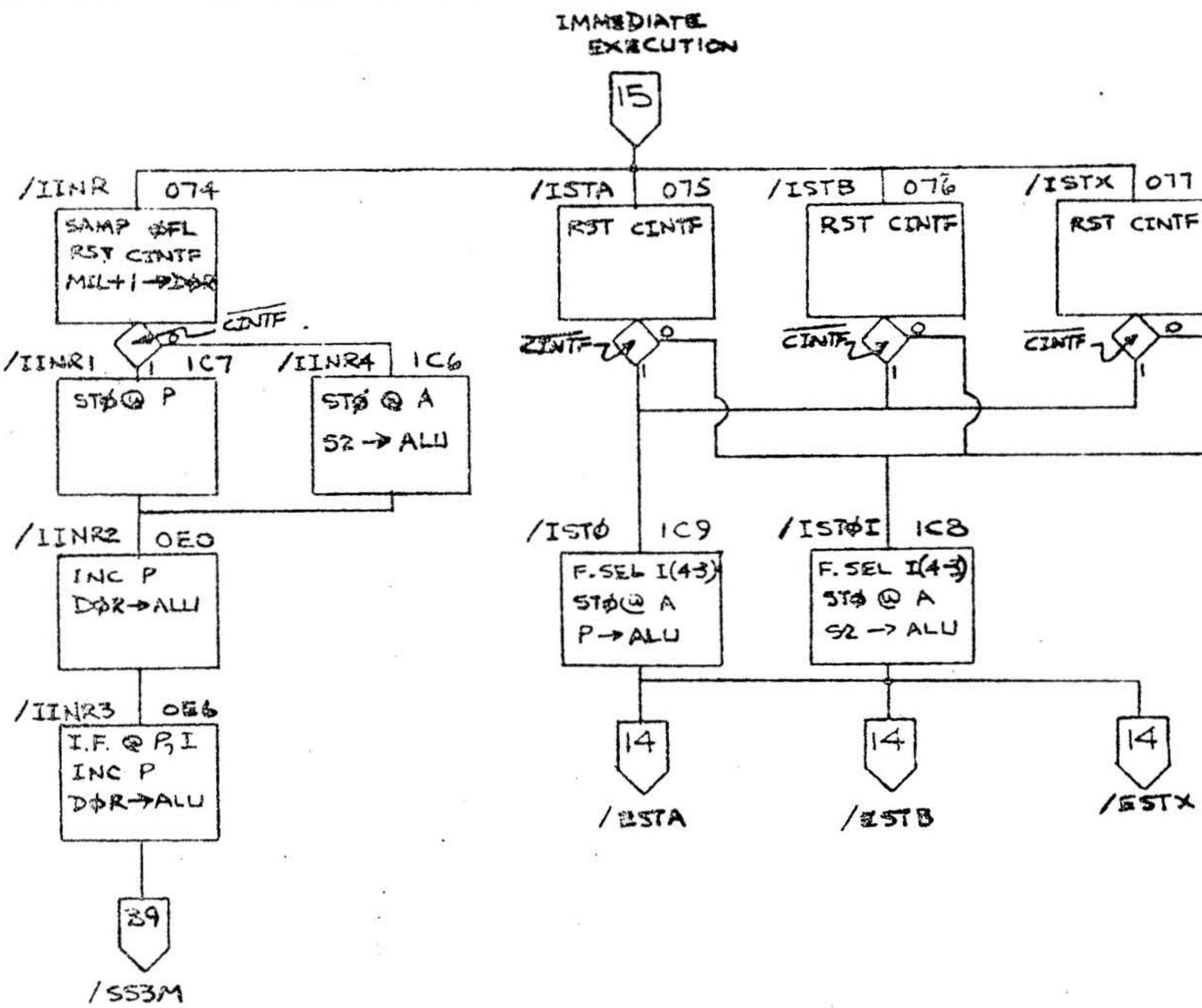

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2.2.3 FRONT PANEL ROUTINES

PROGRAMMER	PROGRAM NO.	DATE	PAGE
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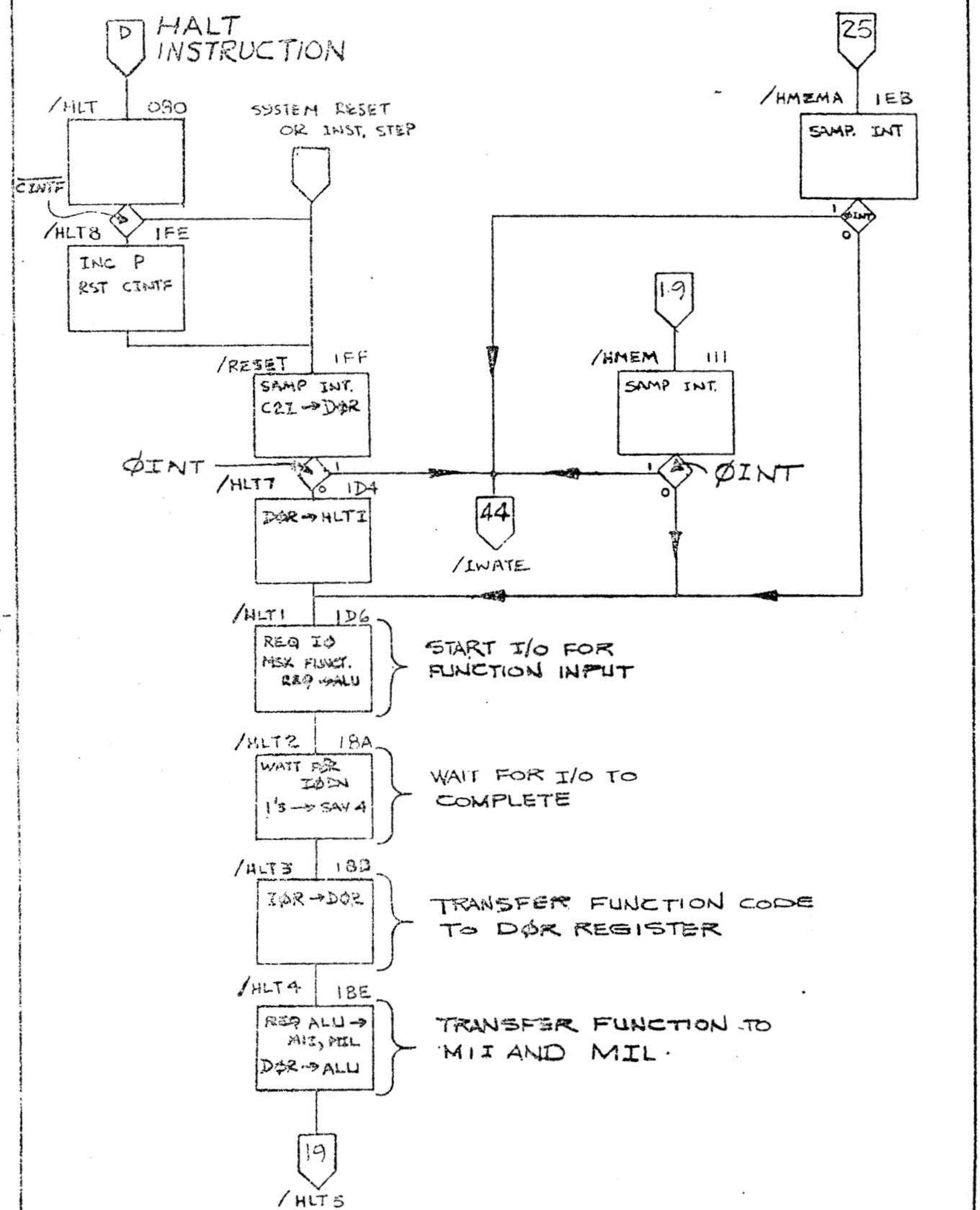
2.2.3.1 HALT LOOP



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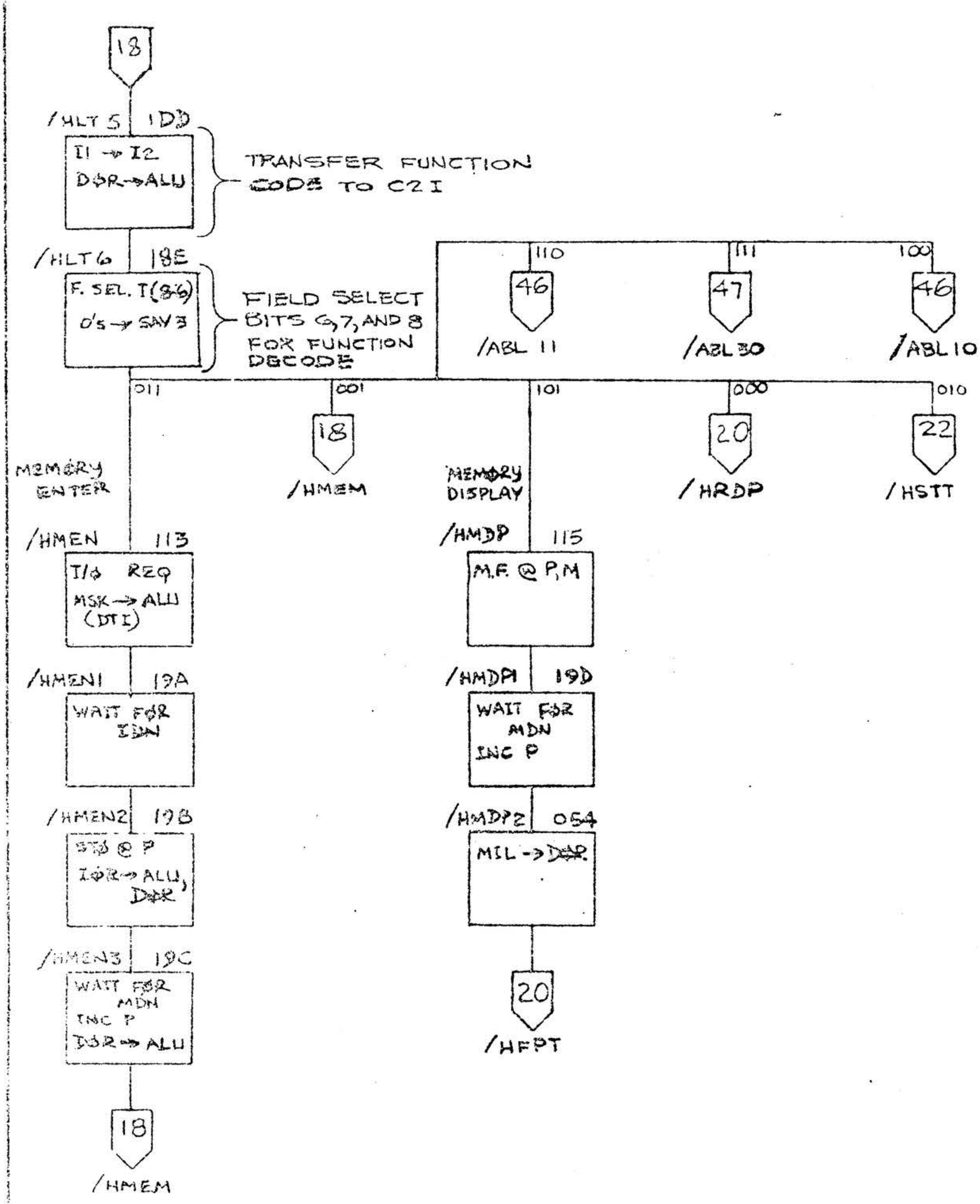
PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	



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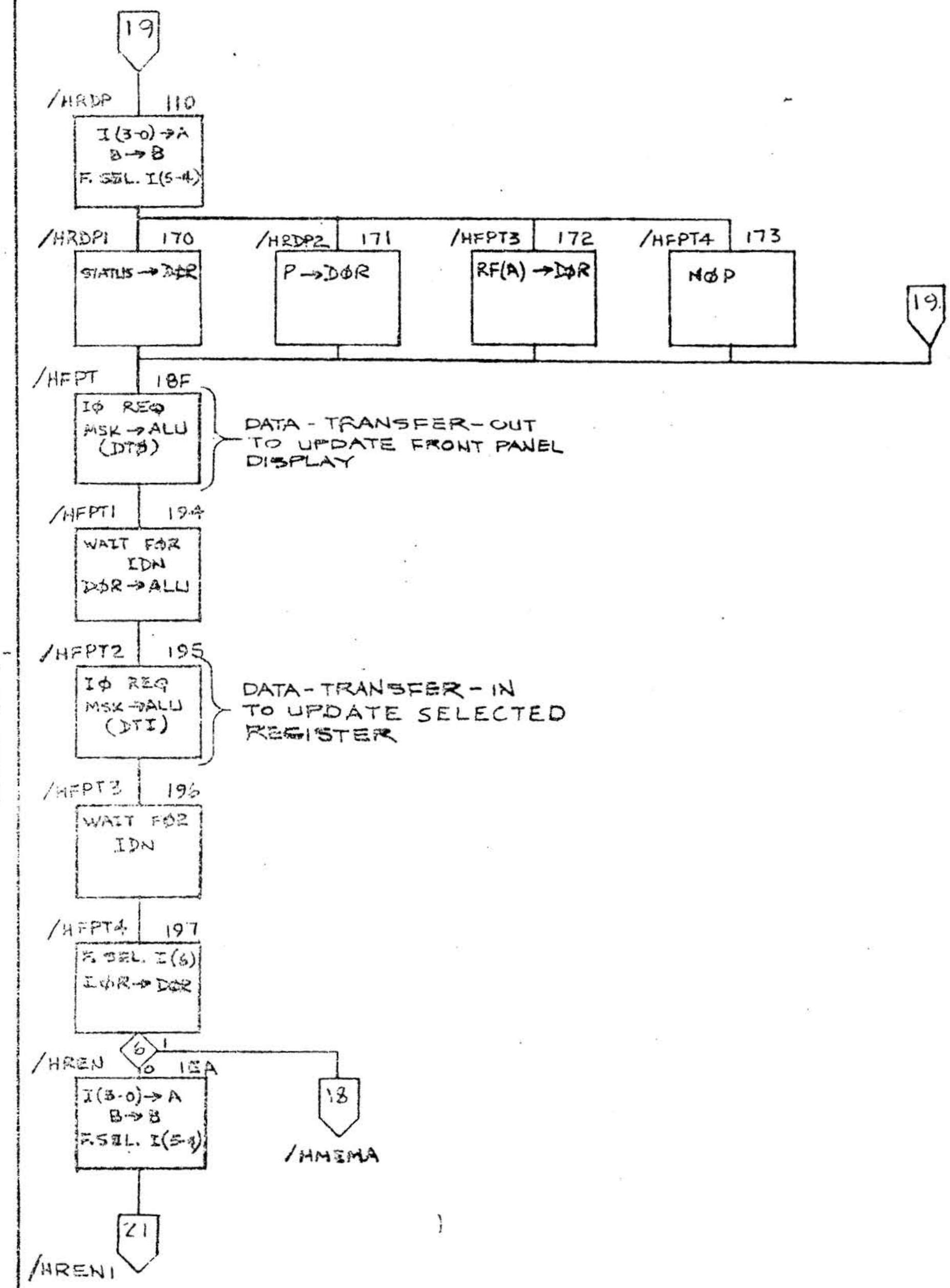
	PREPARED BY	APPROVED BY	SHEET 19 OF 57	

PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

2.2.3.2 REGISTER DISPLAY / ENTER



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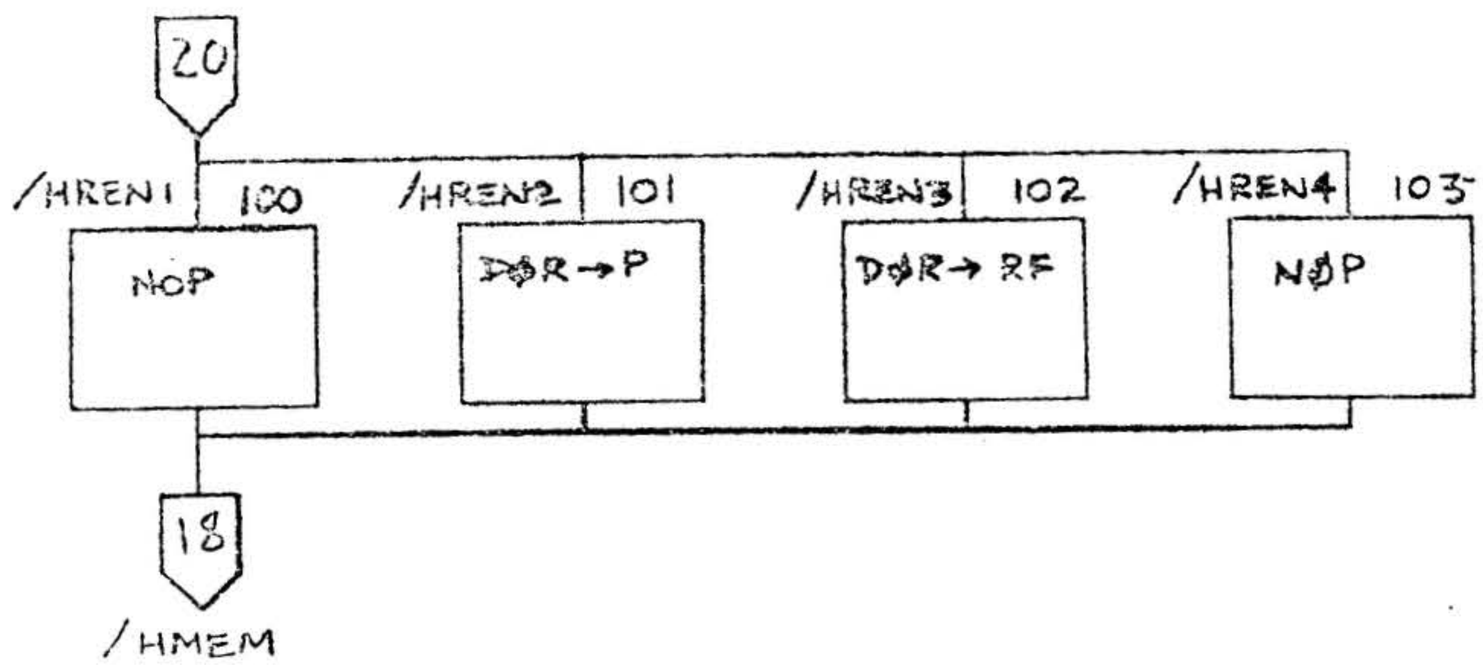

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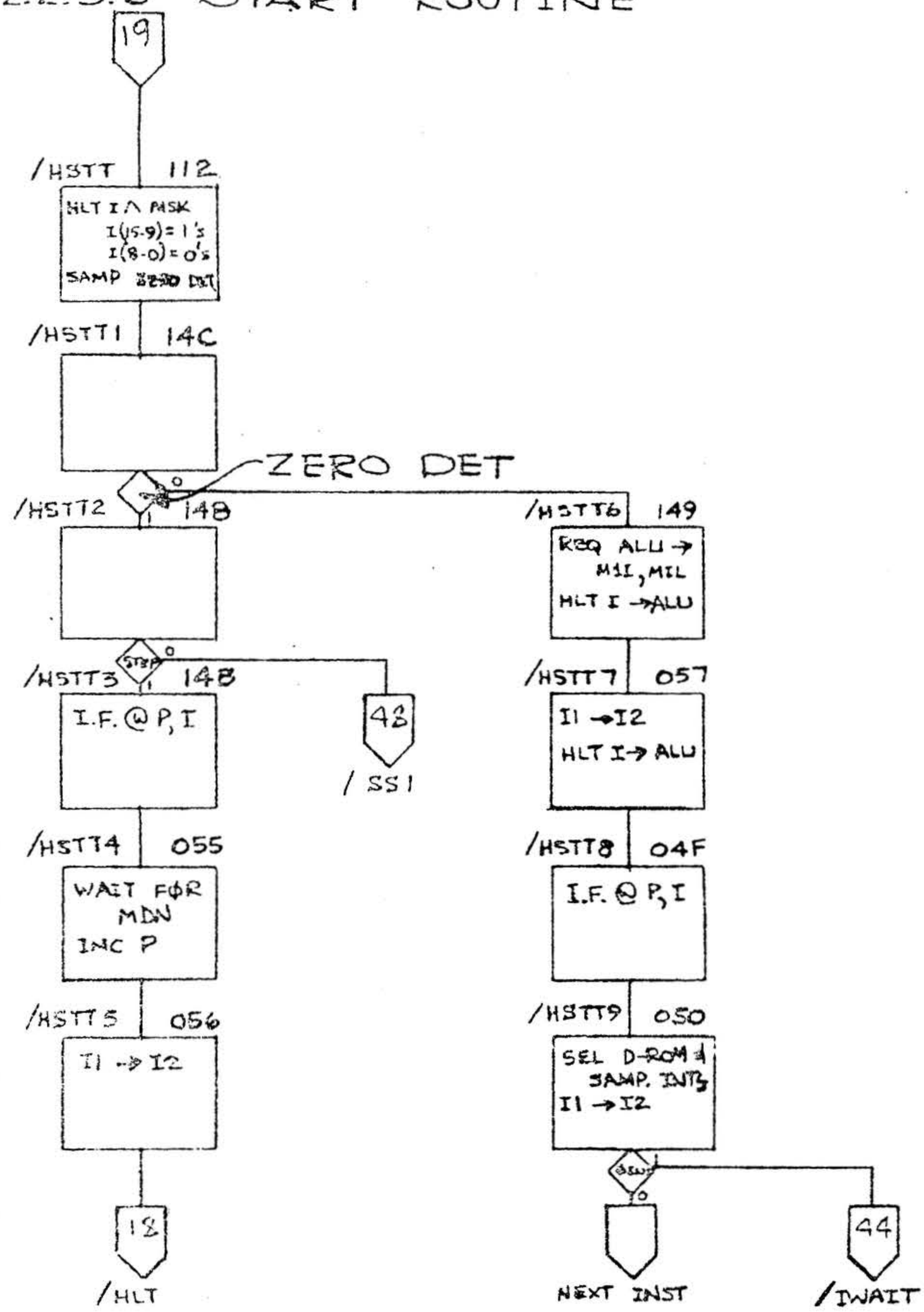
varian data machines, a varian subsidiary	CODE IDENT. NO.	REGISTER DISPLAY/ENTER	99A0887	REV. C
	PREPARED BY	APPROVED BY	SHEET 21 OF 57	

93-29365-000A

PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

2.2.3.3 START ROUTINE



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	PREPARED BY	APPROVED BY	SHEET 22 OF 57	

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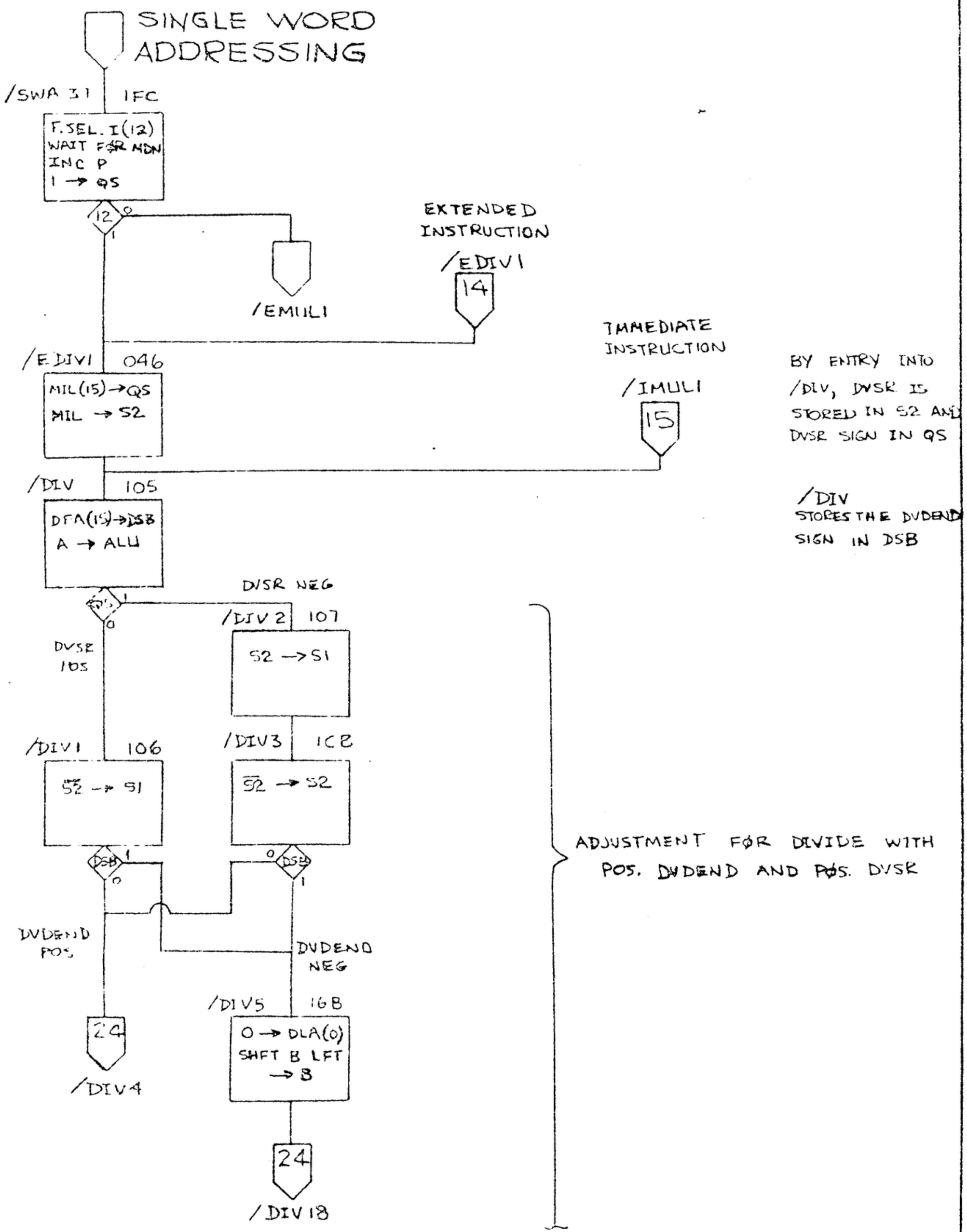
2.2.4 DIVIDE ROUTINE



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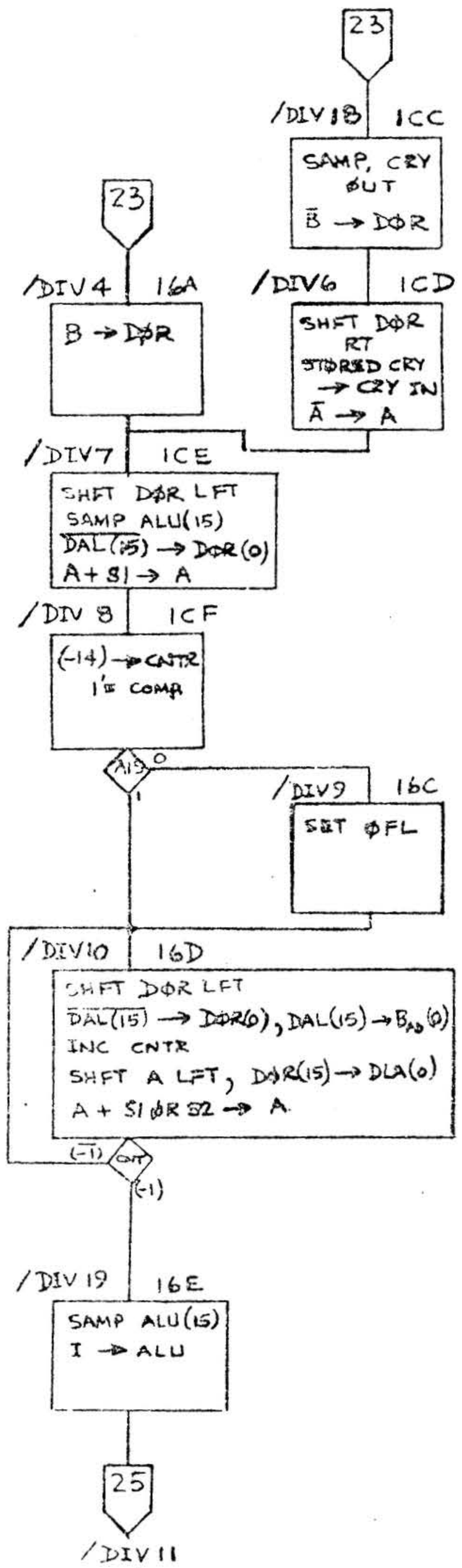

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CHART I.D.	CHART NAME	PROGRAM NAME	

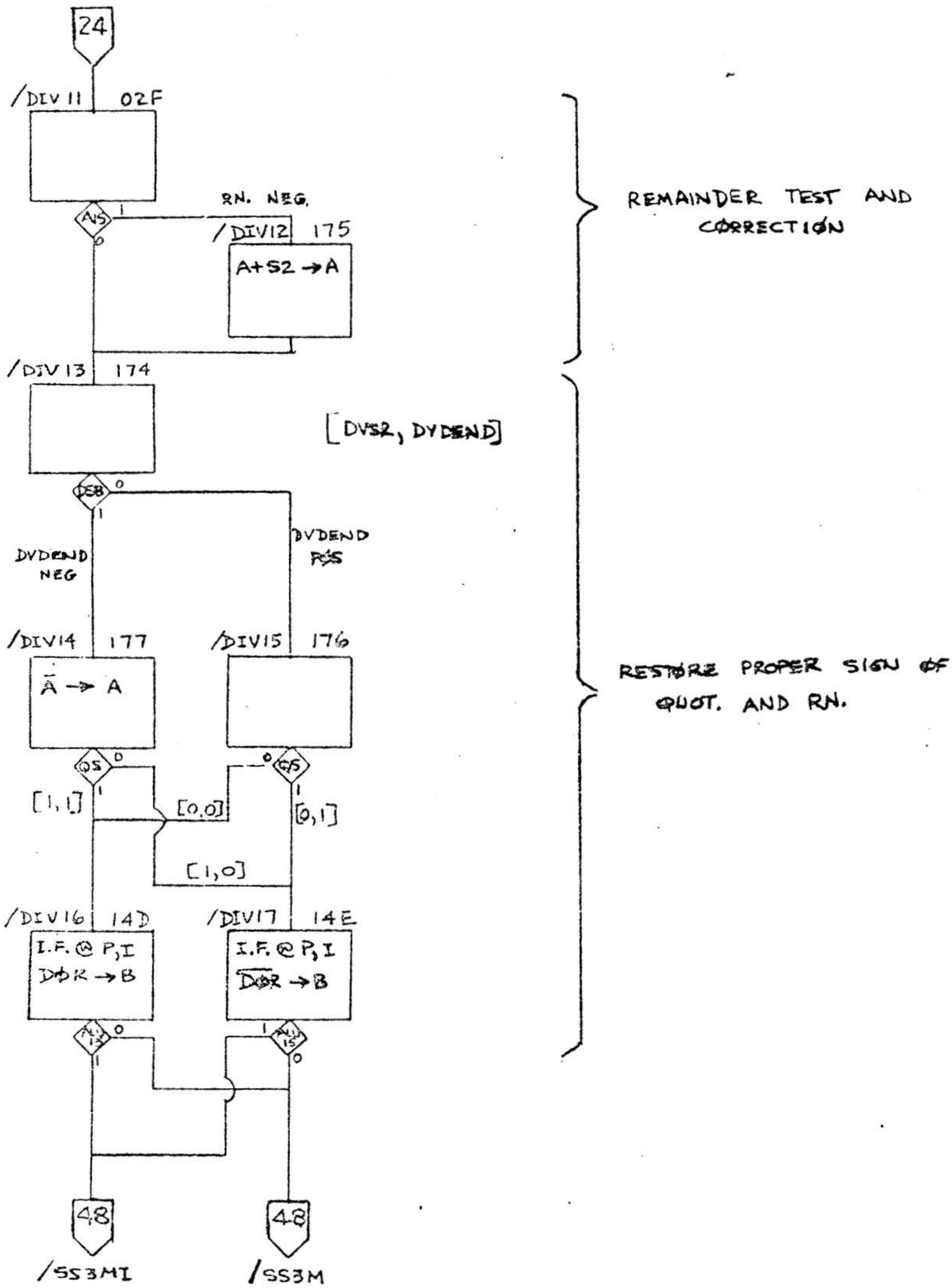

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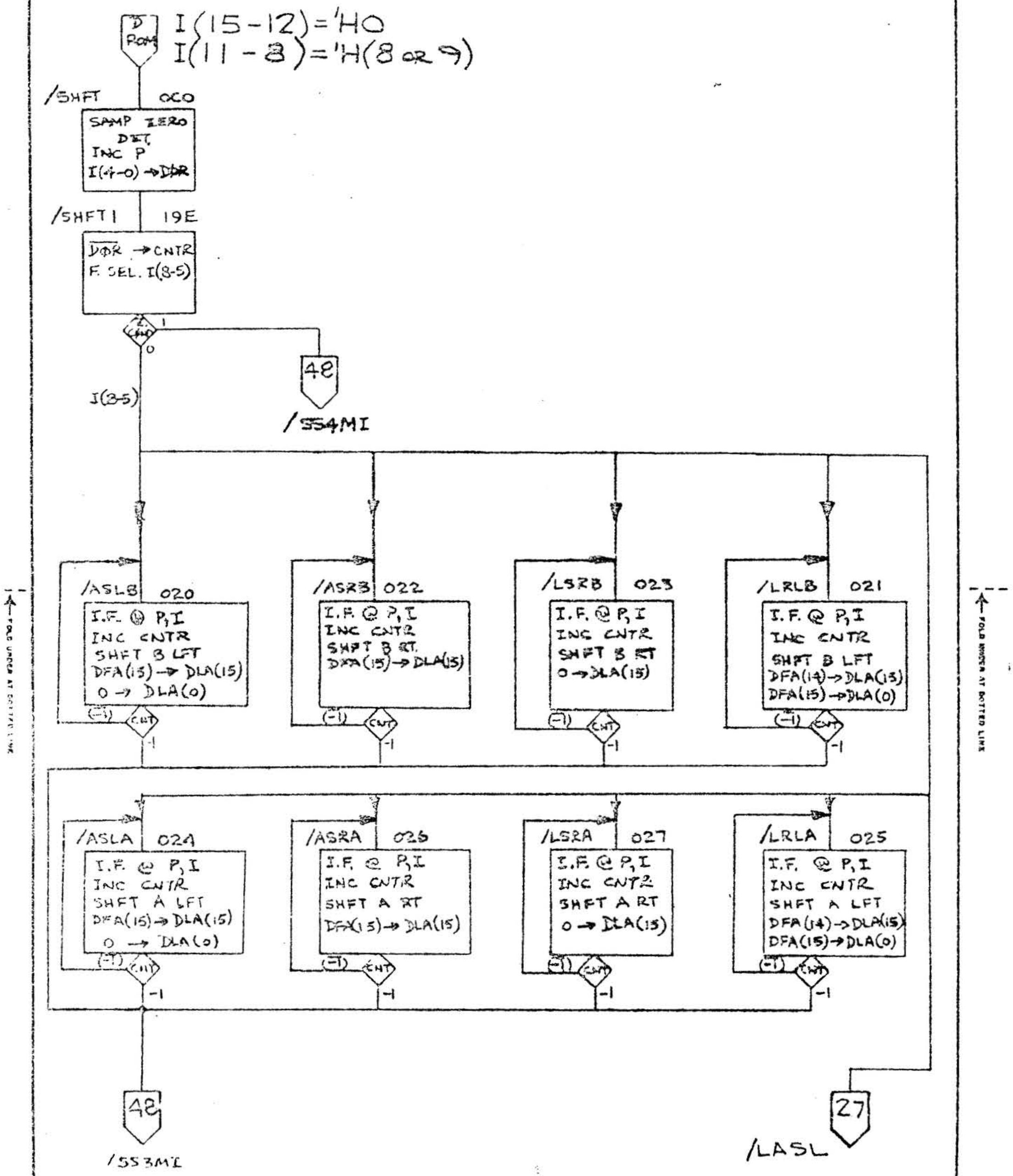
CHART I.D.	CHART NAME	PROGRAM NAME	

2.2.5 SHIFT INSTRUCTIONS



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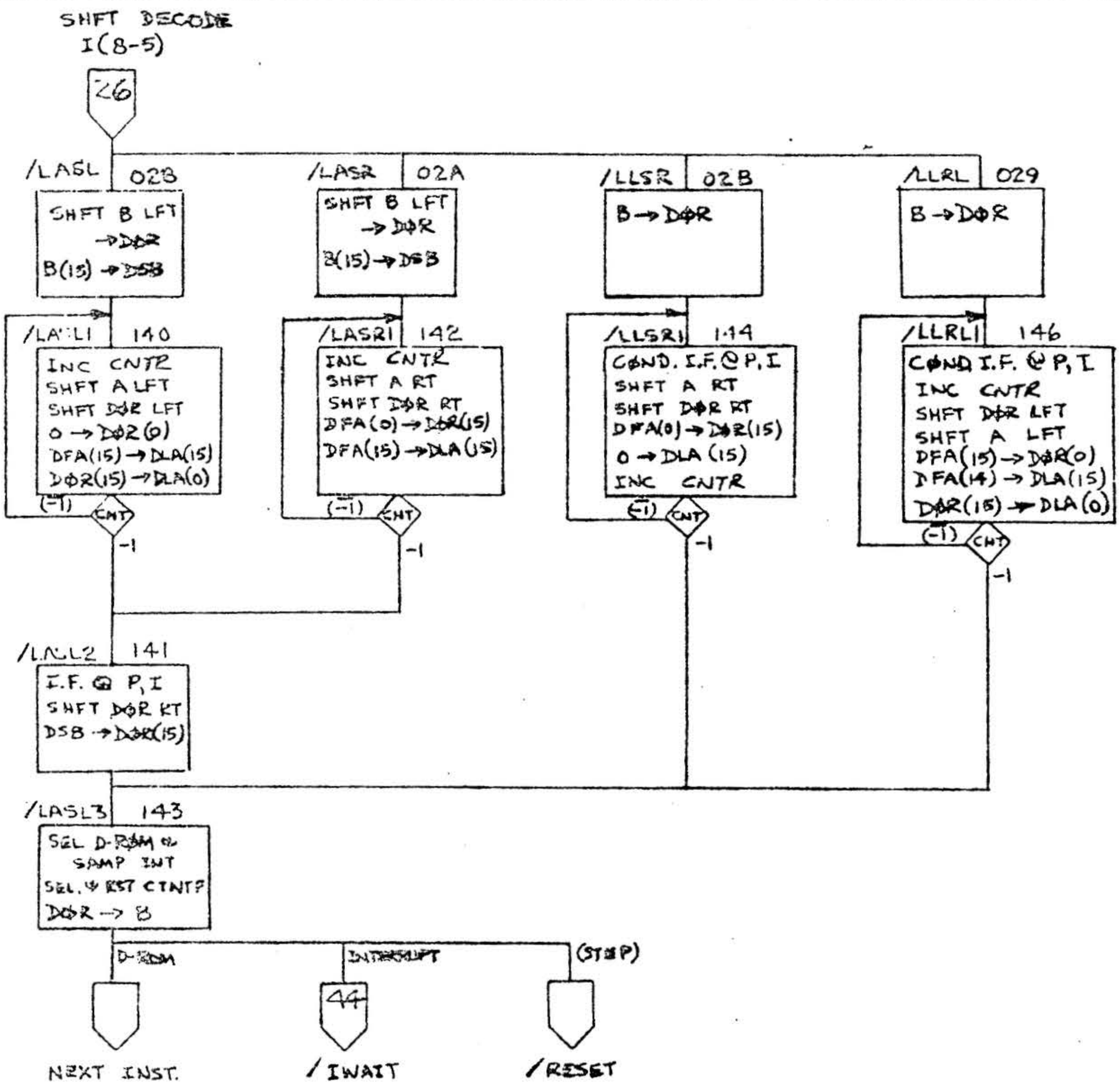
PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	



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varian data machines, a varian subsidiary	CODE IDENT. NO.	SHIFT INSTRUCTIONS	98A0887	REV. B
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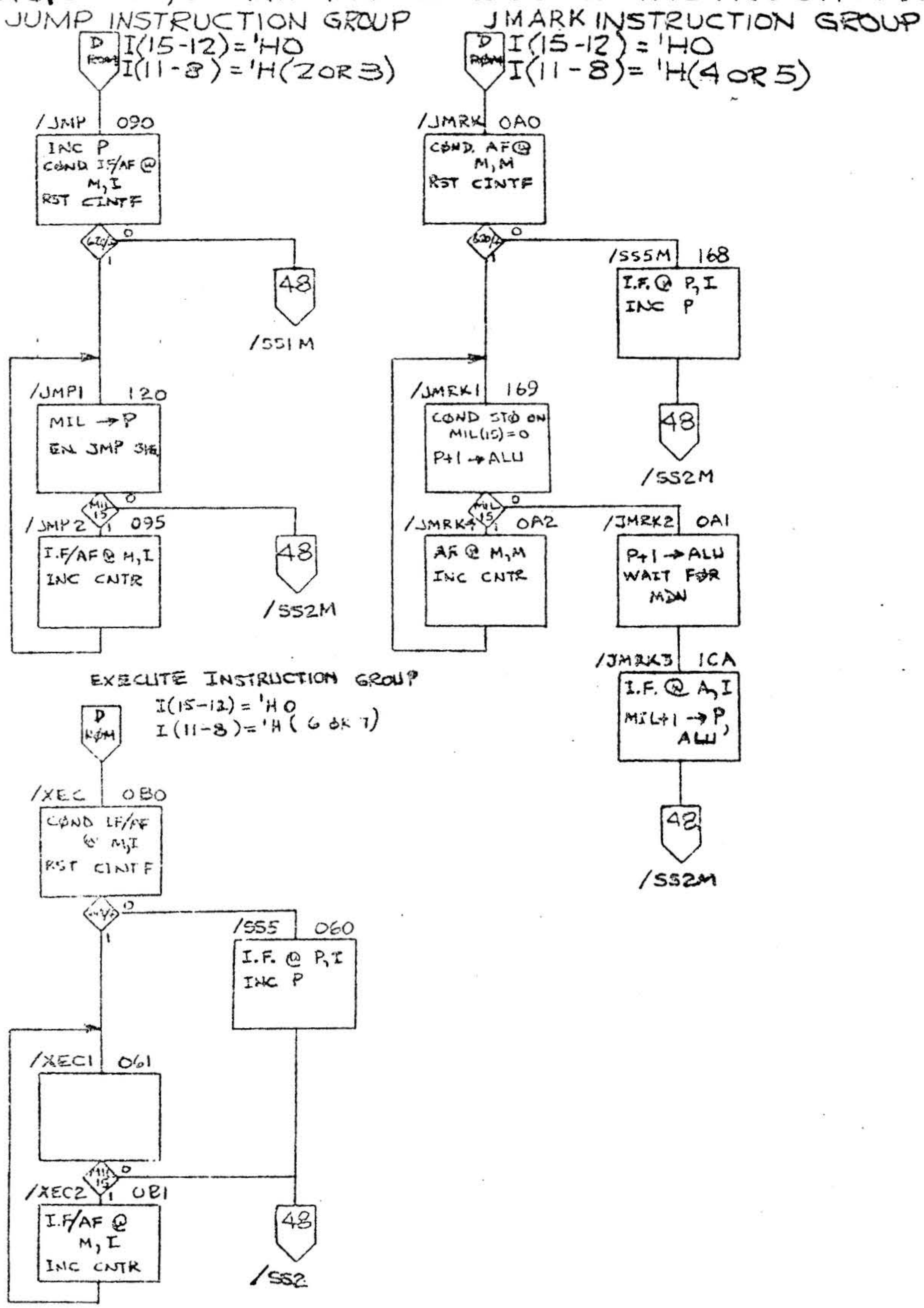
2.2.6 JMP, JMARK AND EXECUTE INSTRUCTIONS



varian data machines a varian subsidiary	CODE IDENT. NO.	JMP, JMARK, & EXECUTE INSTRUCTIONS	98A0887	REV. D
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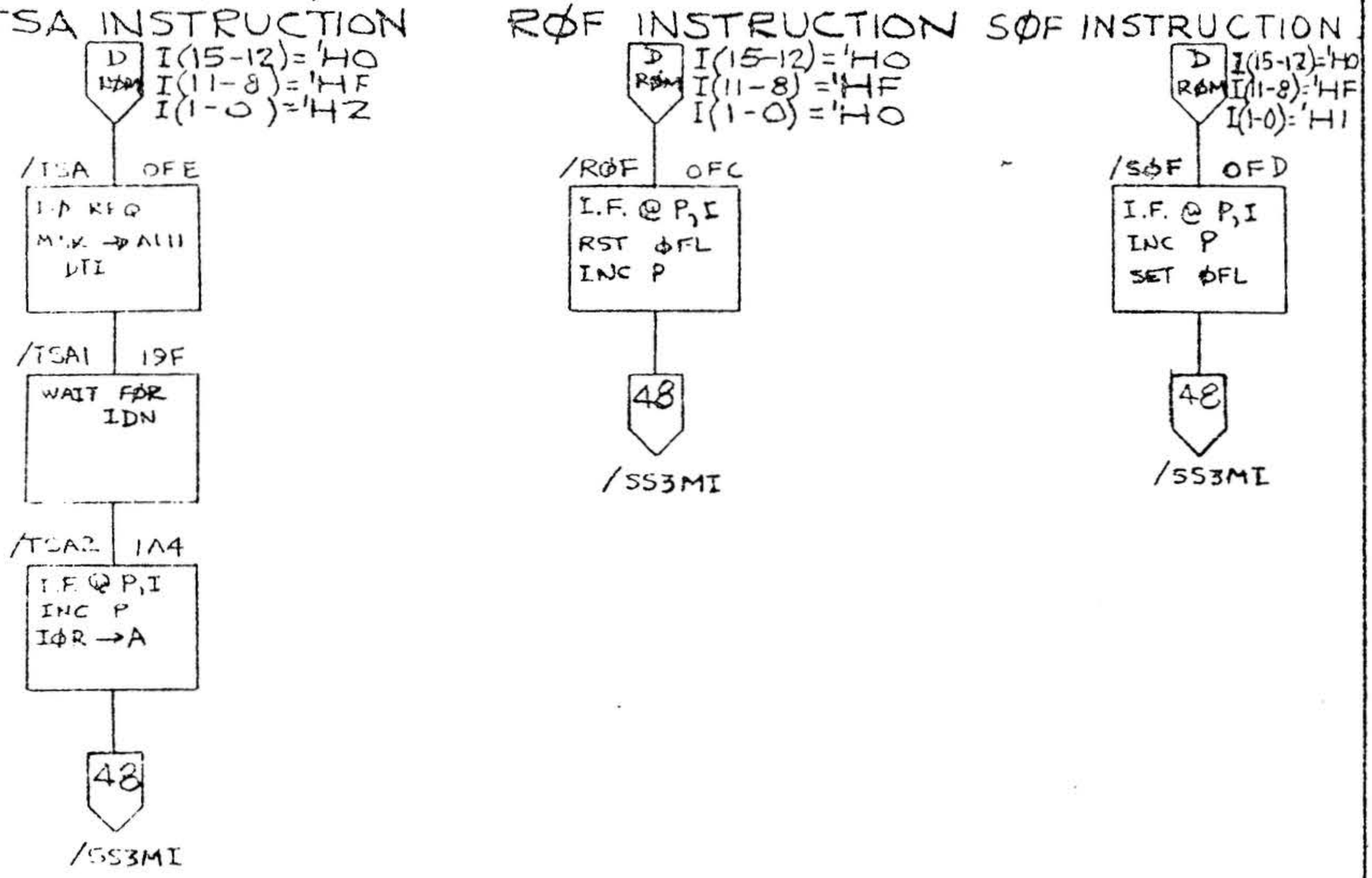
2.2.7 TSA, RØF, AND SØF INSTRUCTIONS



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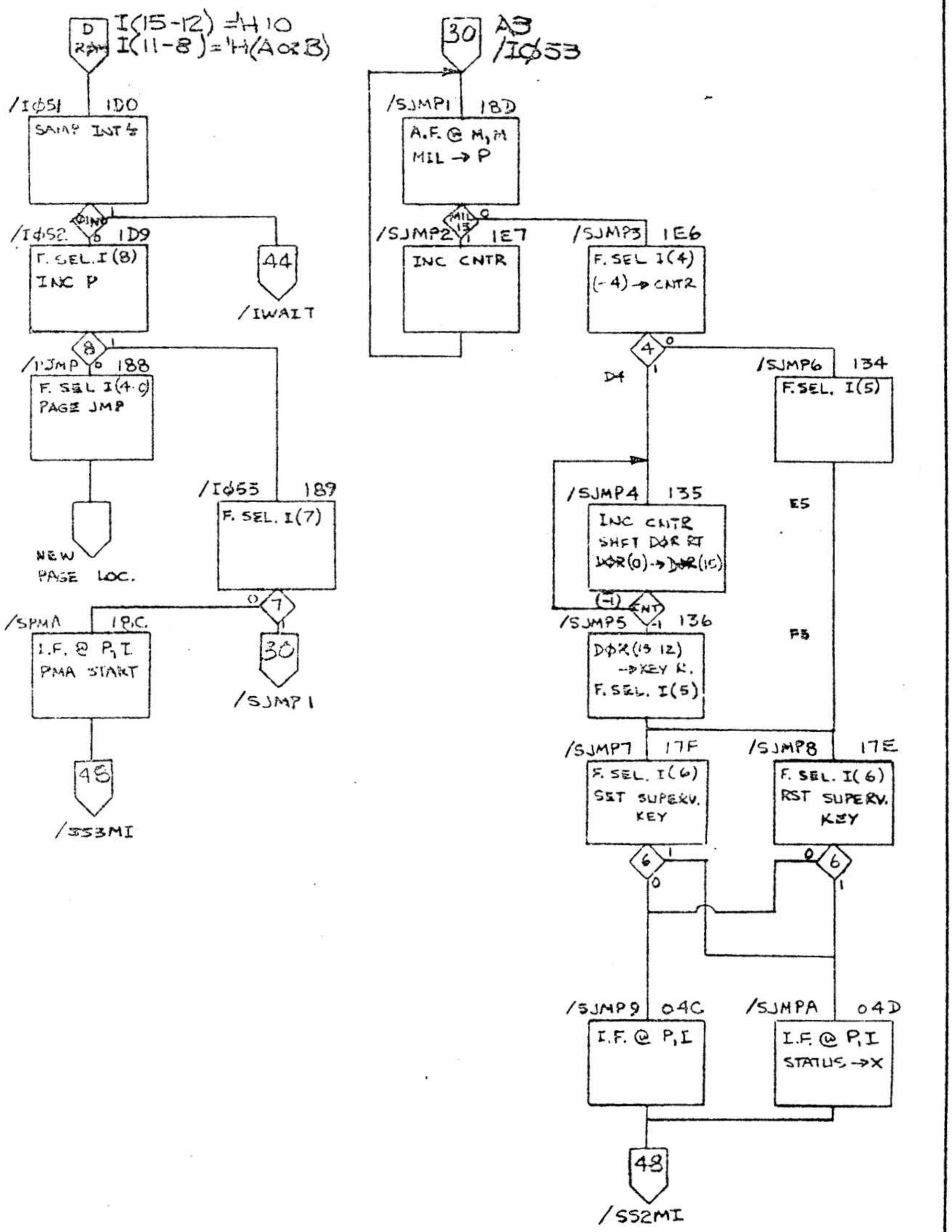
	PREPARED BY	APPROVED BY	SHEET 29 OF 57

FOLD UNDER AT DOTTED LINE

PROGRAMMER	PROGRAM NO.	DATE	PAGE
CHART I.D.	CHART NAME	PROGRAM NAME	

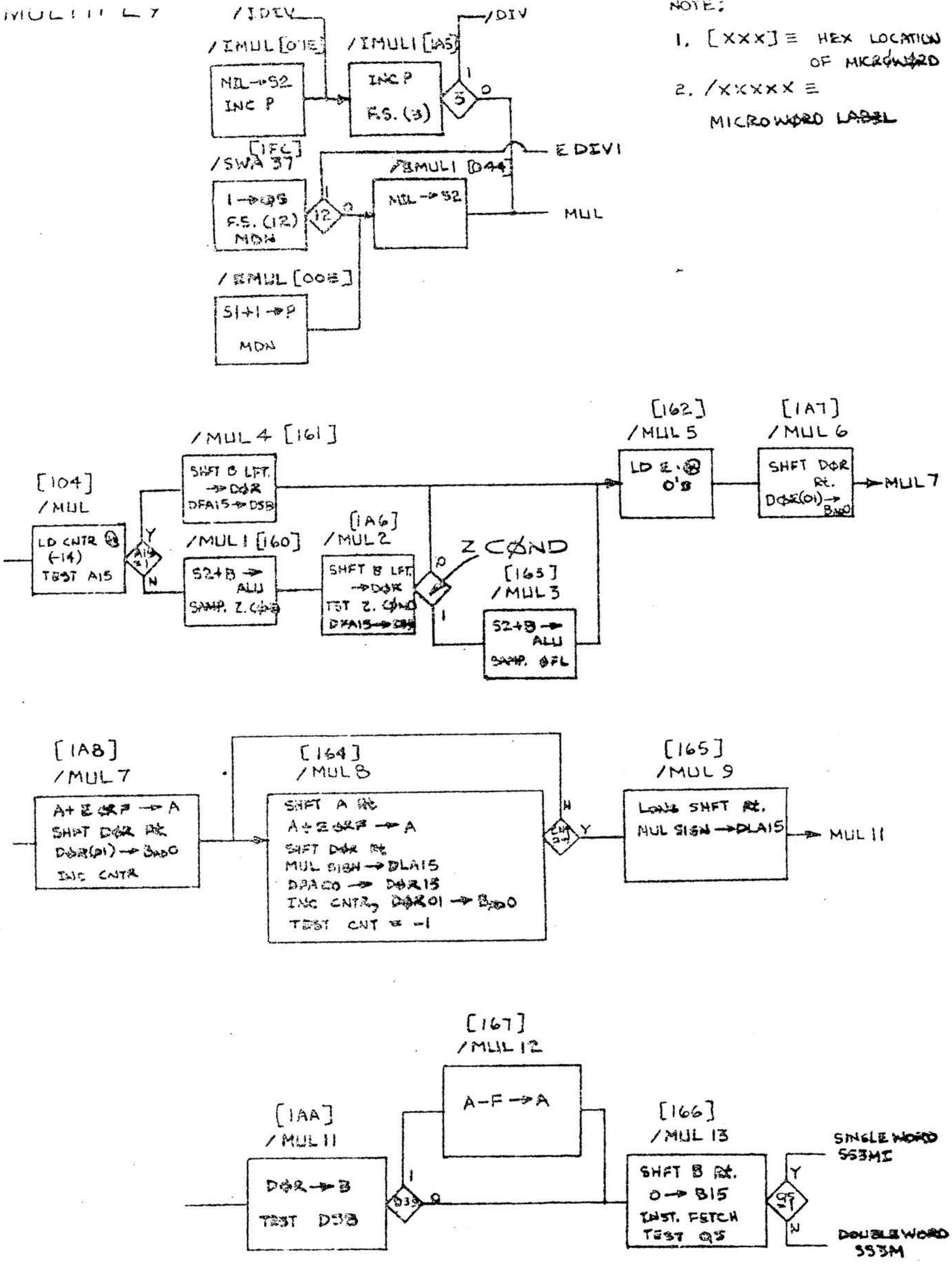
2.2.8 SPMA, BCS, SJUMP INSTRUCTIONS



varian data machines a varian subsidiary	CODE IDENT. NO.	SPM, BCS, SJUMP INSTRUCTIONS	98AC887	REV. B
	PREPARED BY	APPROVED BY	SHEET 30 OF 57	

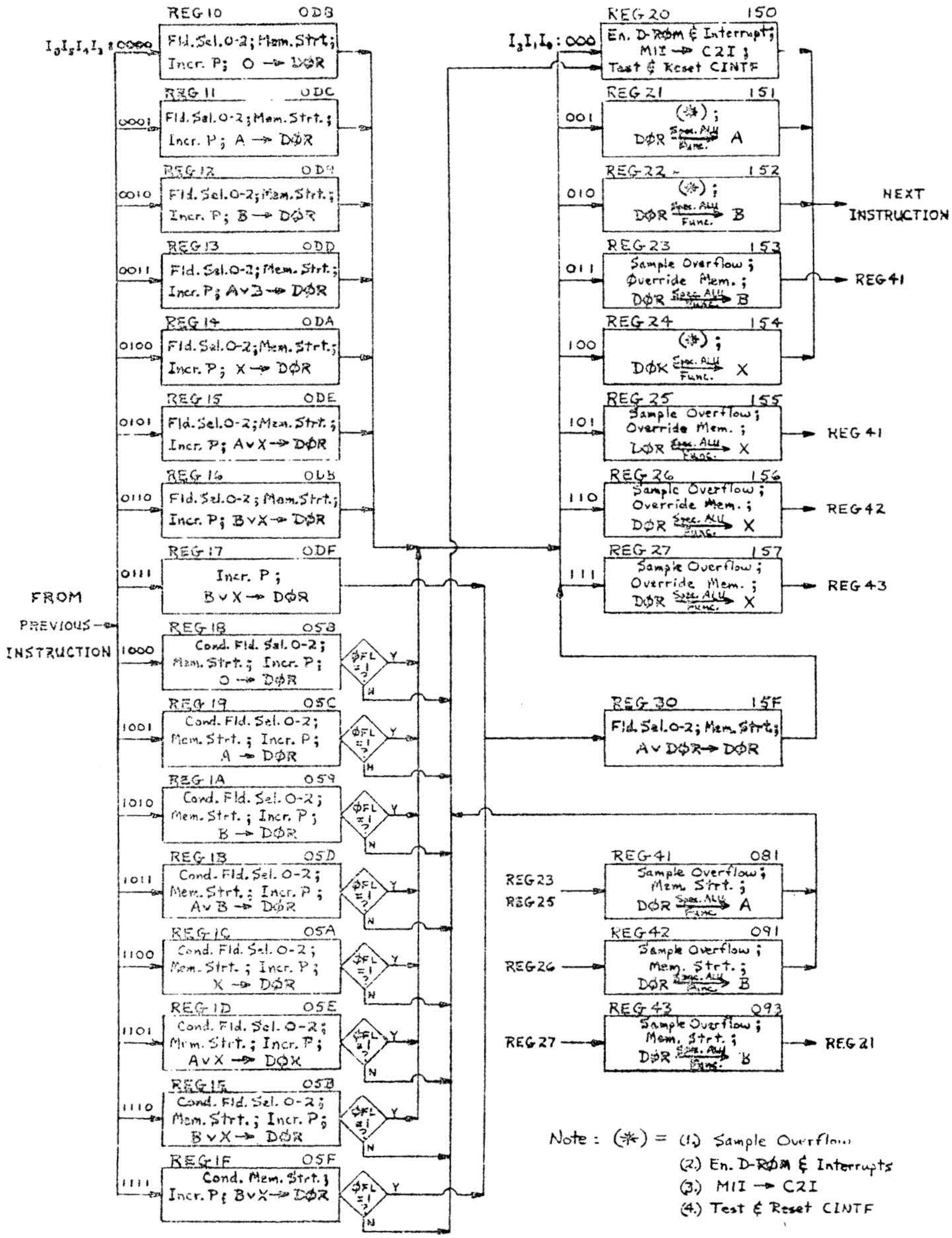
NOTE:

1. [XXX] ≡ HEX LOCATION OF MICROWORD
2. /XXXXX ≡ MICROWORD LABEL



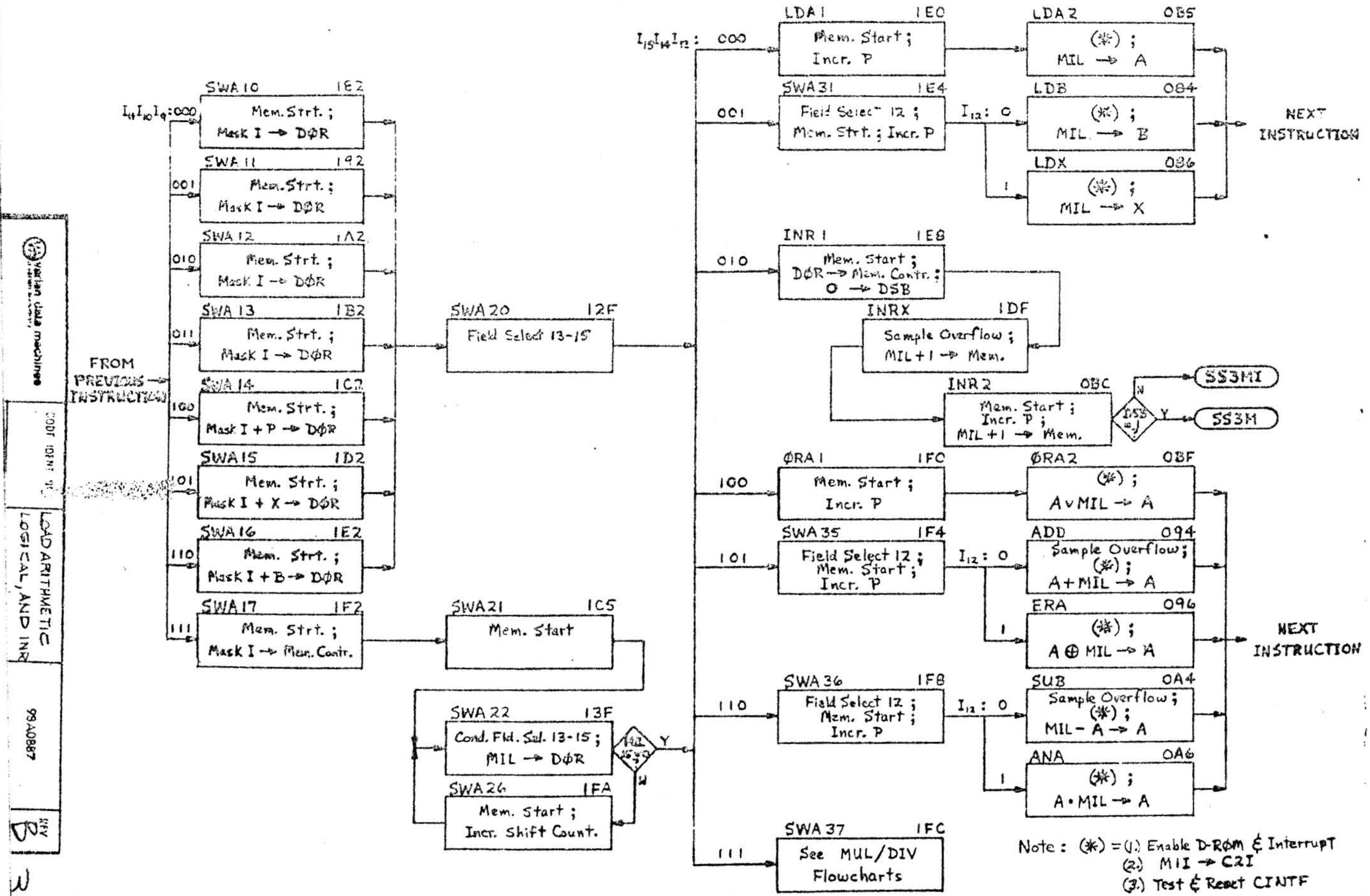
varian data machines	CODE IDENT NO.	MULTIPLY	98A0887	REV B
	PREPARED	APPR	SHEET 31 OF 57	

22.10 REGISTER TO REGISTER INSTRUCTIONS



varian data machines	CODE IDENT NO	REGISTER TO REGISTER INSTRUCTIONS	98A0387	REV B
	PREPARED D.M.	APPR	SHEET 32 OF 57	

2.2.11 SINCE - WORD ADDRESSING INSTRUCTIONS

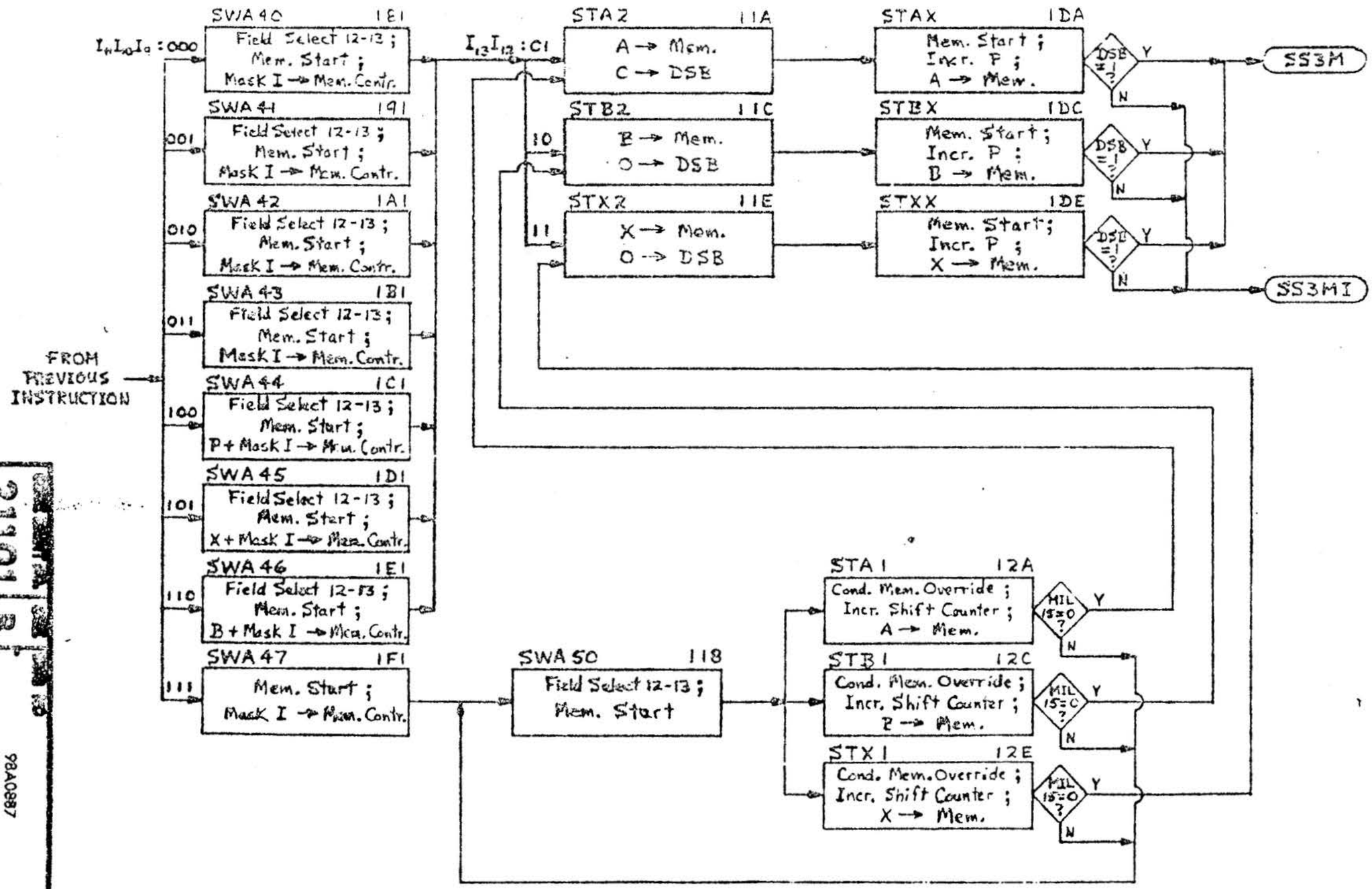


LOAD ARITHMETIC LOGICAL, AND INR

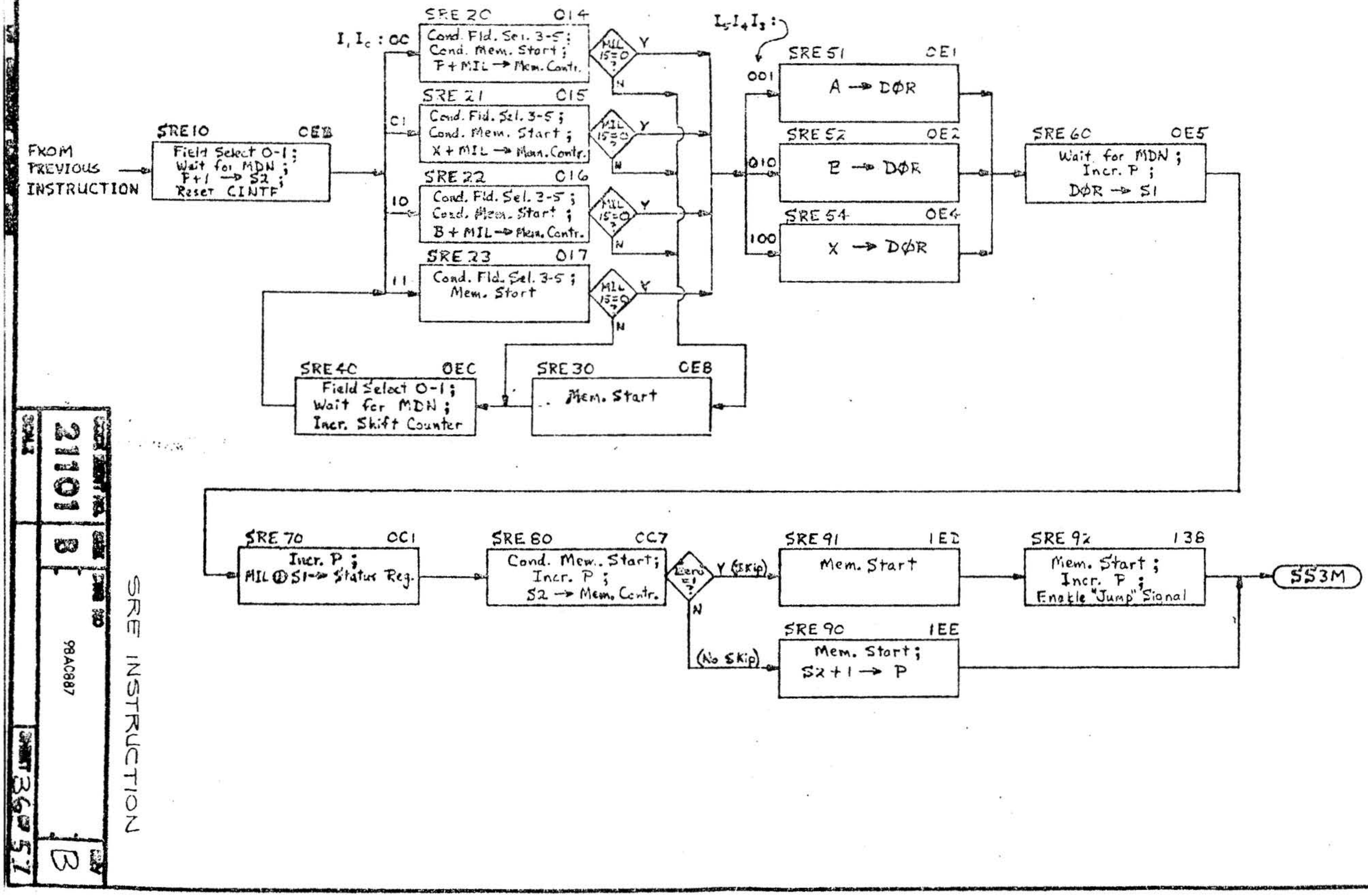
98A0887

REV B

22.11.2 STORE (SWA)

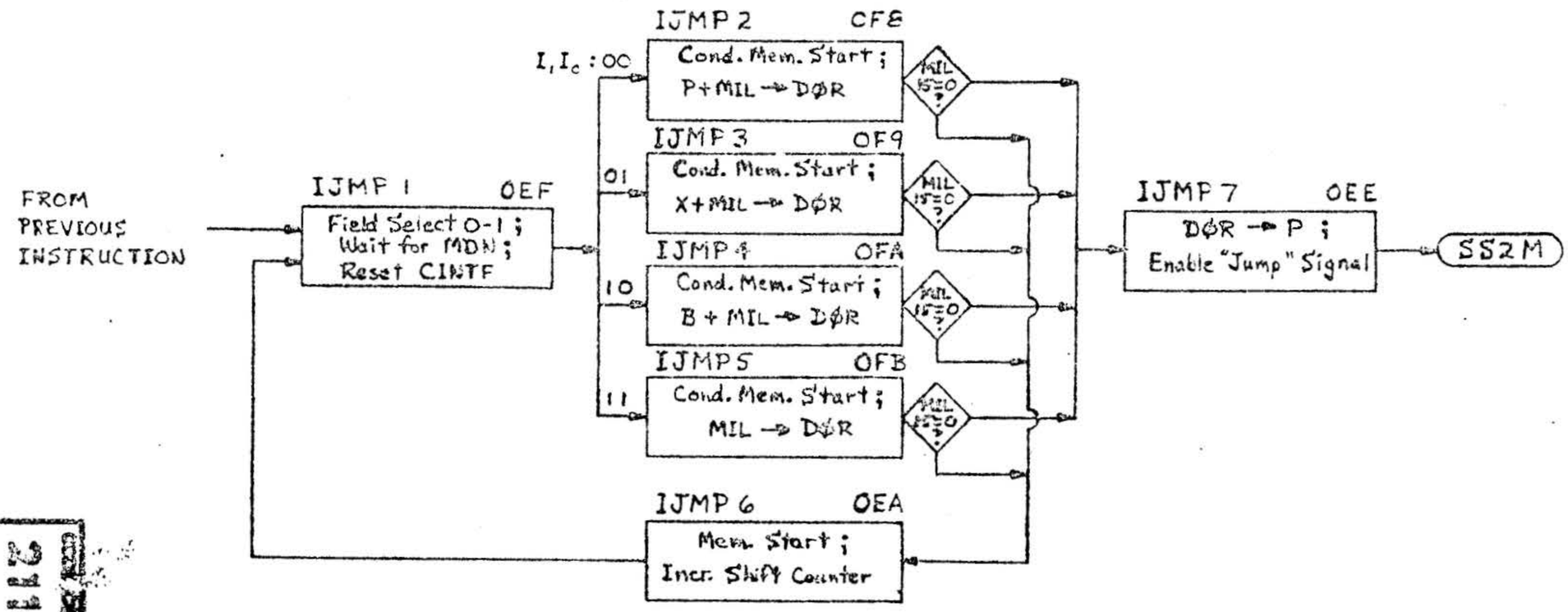


2.2.12 SRE INSTRUCTION



SRE INSTRUCTION

2.2.13 IJMP INSTRUCTION



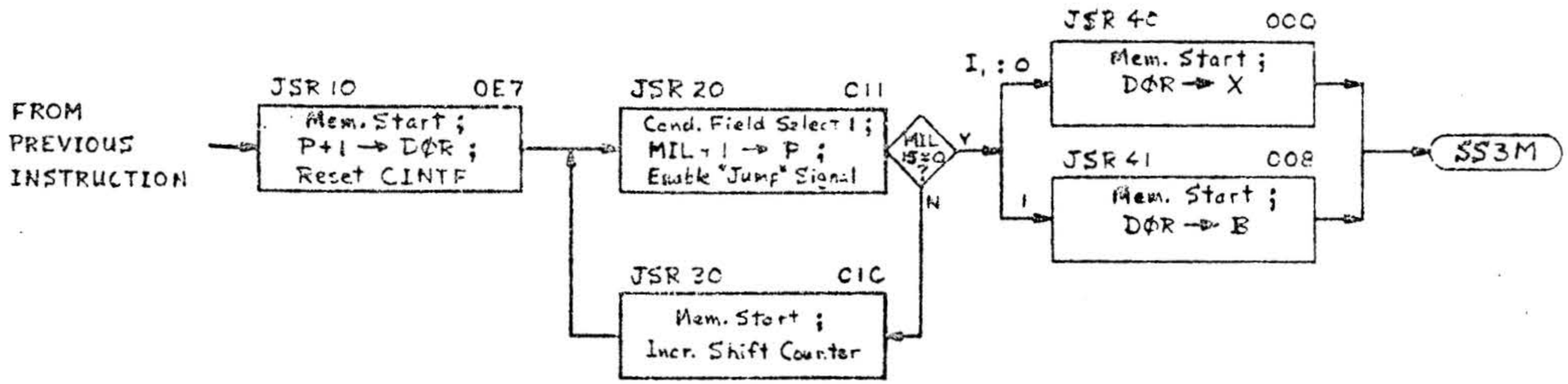
IJMP INSTRUCTION

21101 B

98A0887

SHEET 37 of 57

B

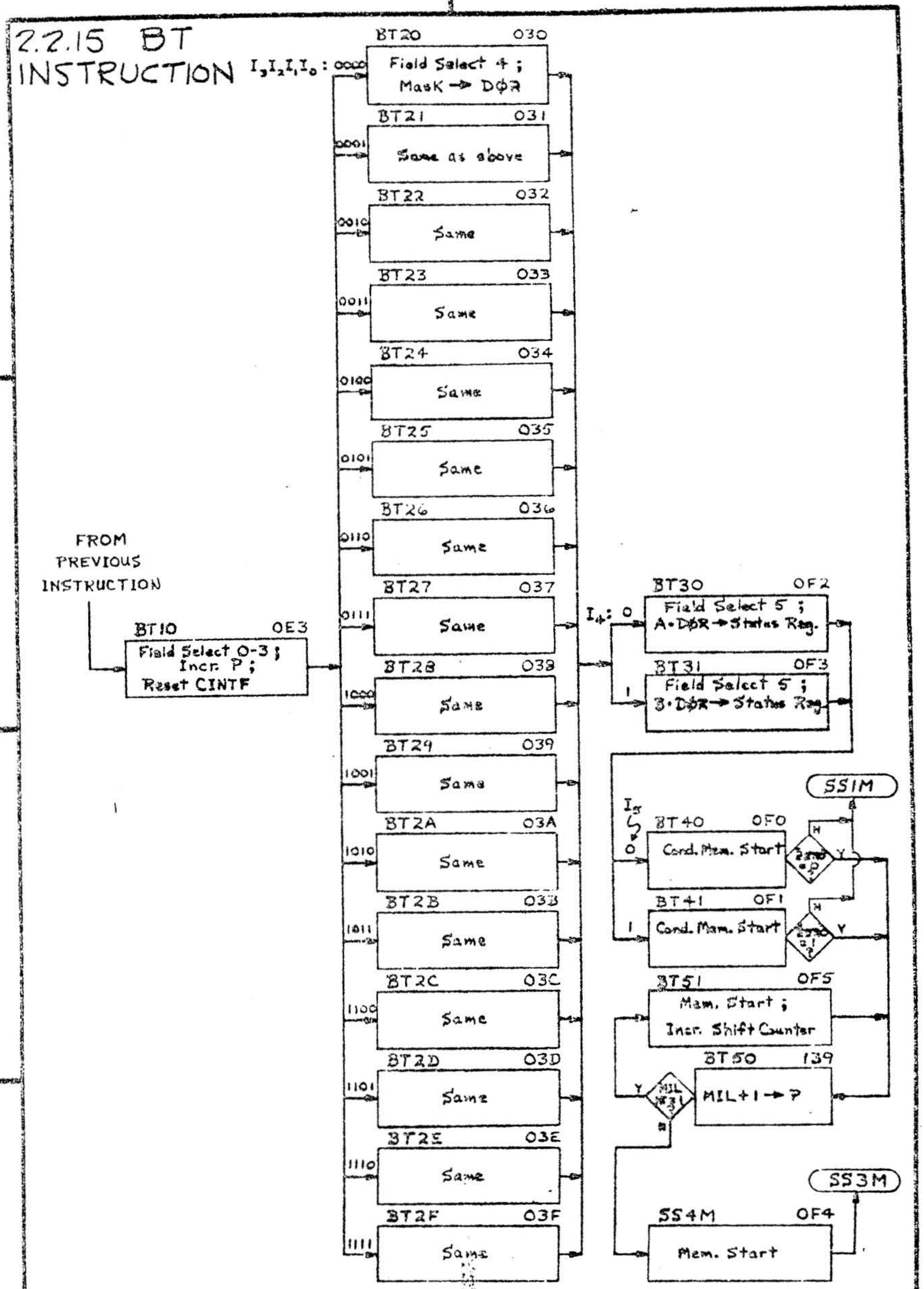


JSR INSTRUCTION

CODE IDENT NO.	CODE	DWG NO	REV
21101	B	93A0867	B

SCALE | SHEET 38 OF 57

22.14 LSB INSTRUCTION



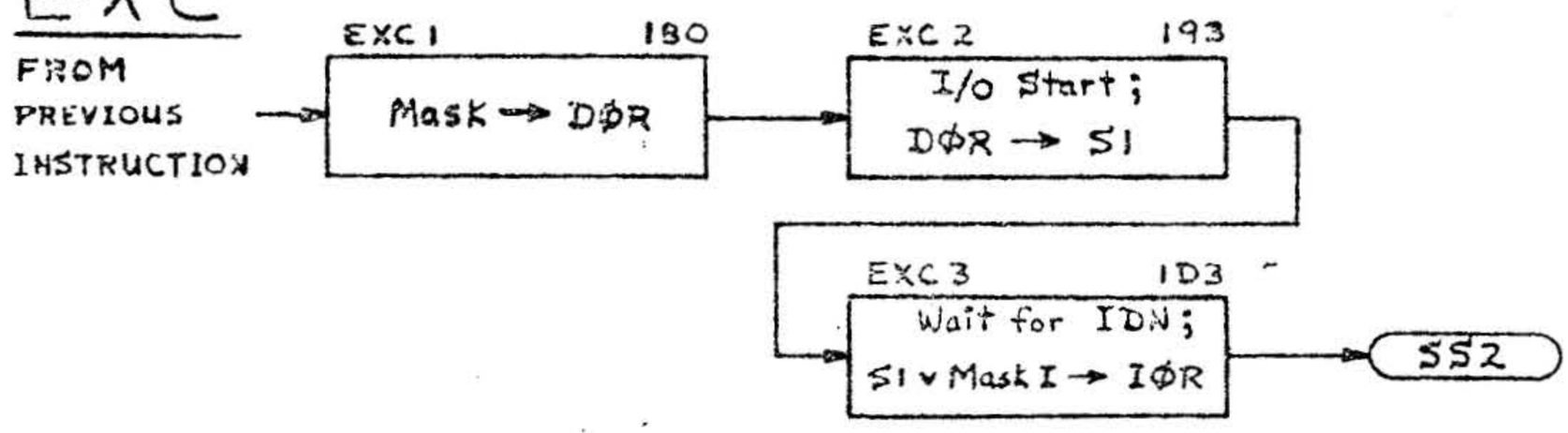
BT INSTRUCTION

21101	B	98A0837	B
		SHEET 39 OF 57	

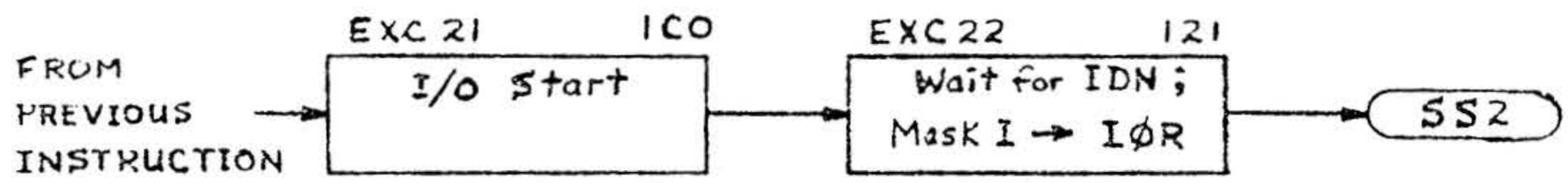
2.2.16 INPUT/OUTPUT (I/O) INSTRUCTIONS

2.2.16.1 I/O - EXC, EXC2, SEN

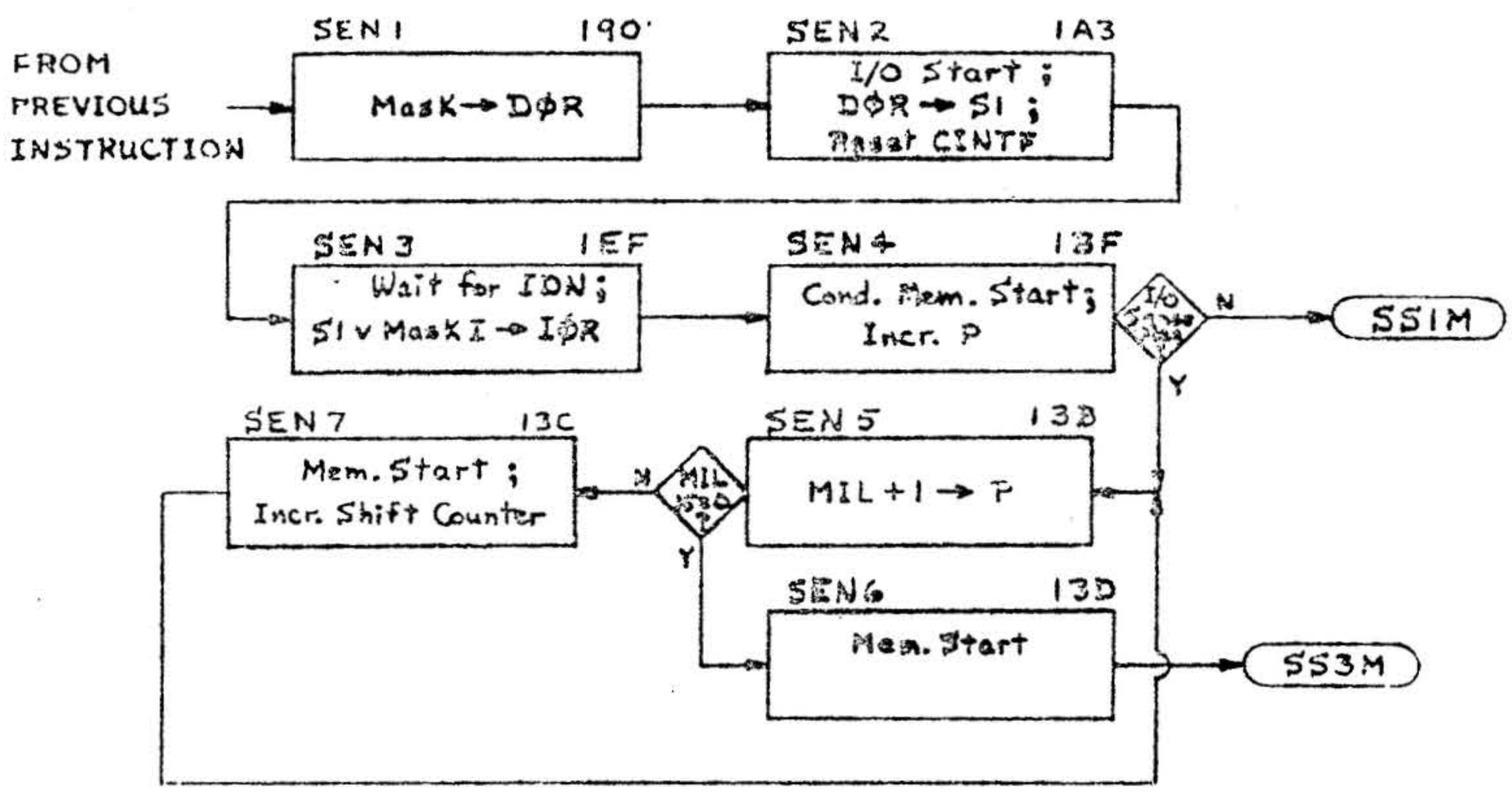
EXC



EXC 2



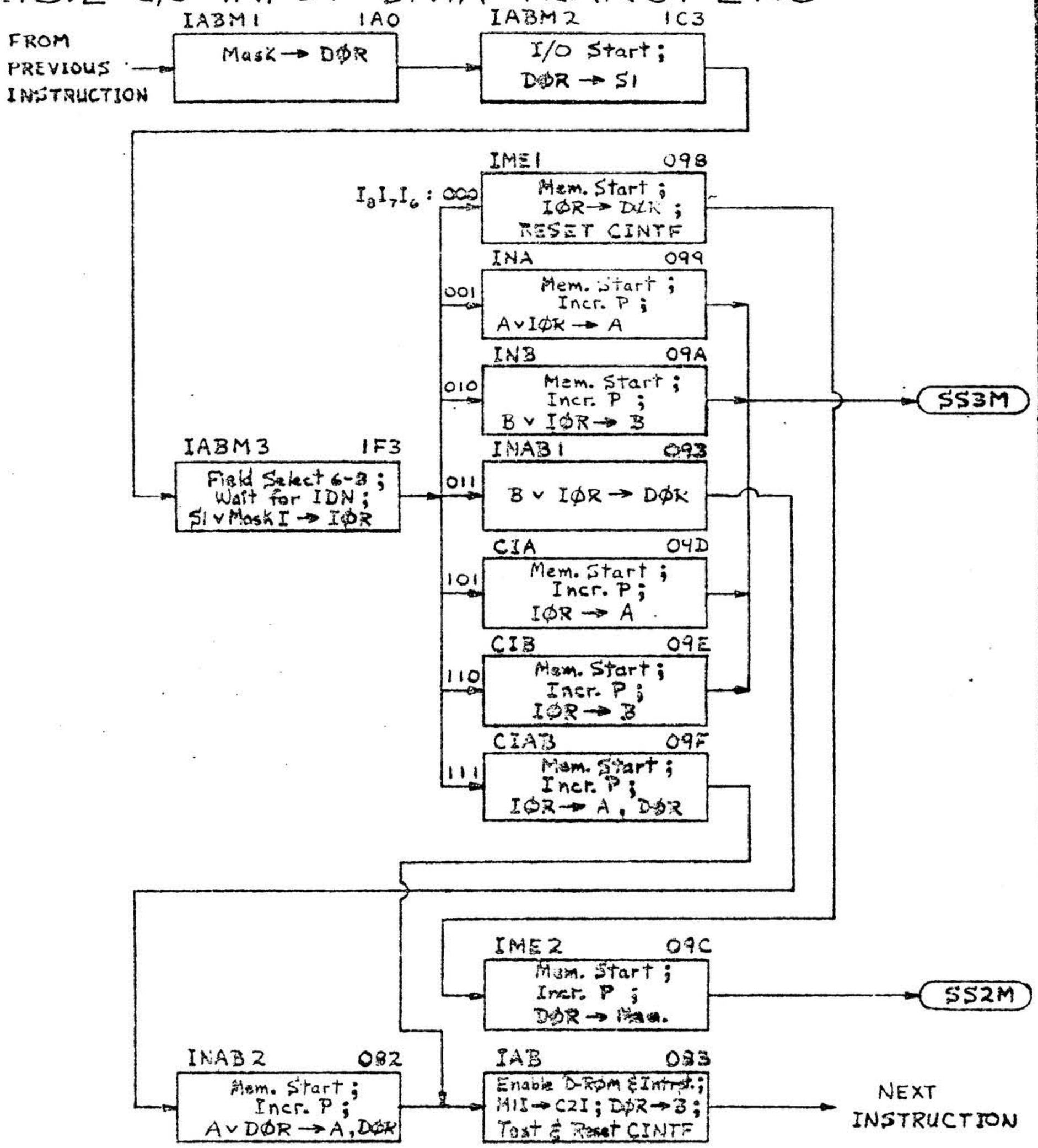
SEN



I/Ø-EXC, EXC2, SEN

CODE IDENT NO.	SIZE	DWG NO	REV
21101	B	98A0887	D
SCALE		SHEET 41 OF 57	

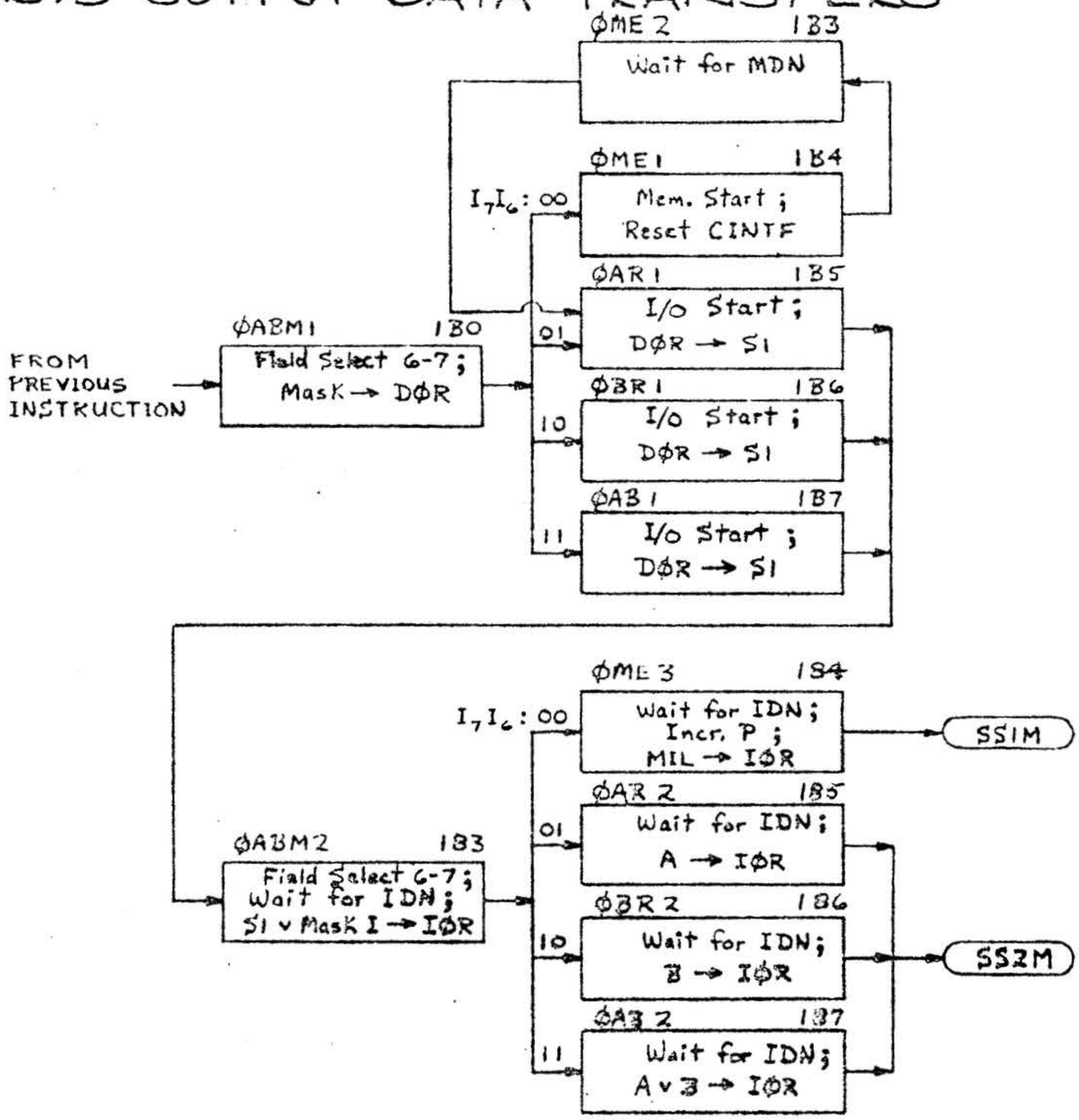
2.2.16.2 I/O INPUT DATA TRANSFERS



I/O INPUT DATA TRANSFER
(CIA, CIB, CIAB, INA, INB, INAB, IME)

CODE IDENT NO.	SIZE	DWG NO	REV
21101	B	98A0887	E
SCALE		SHEET 42 OF 57	

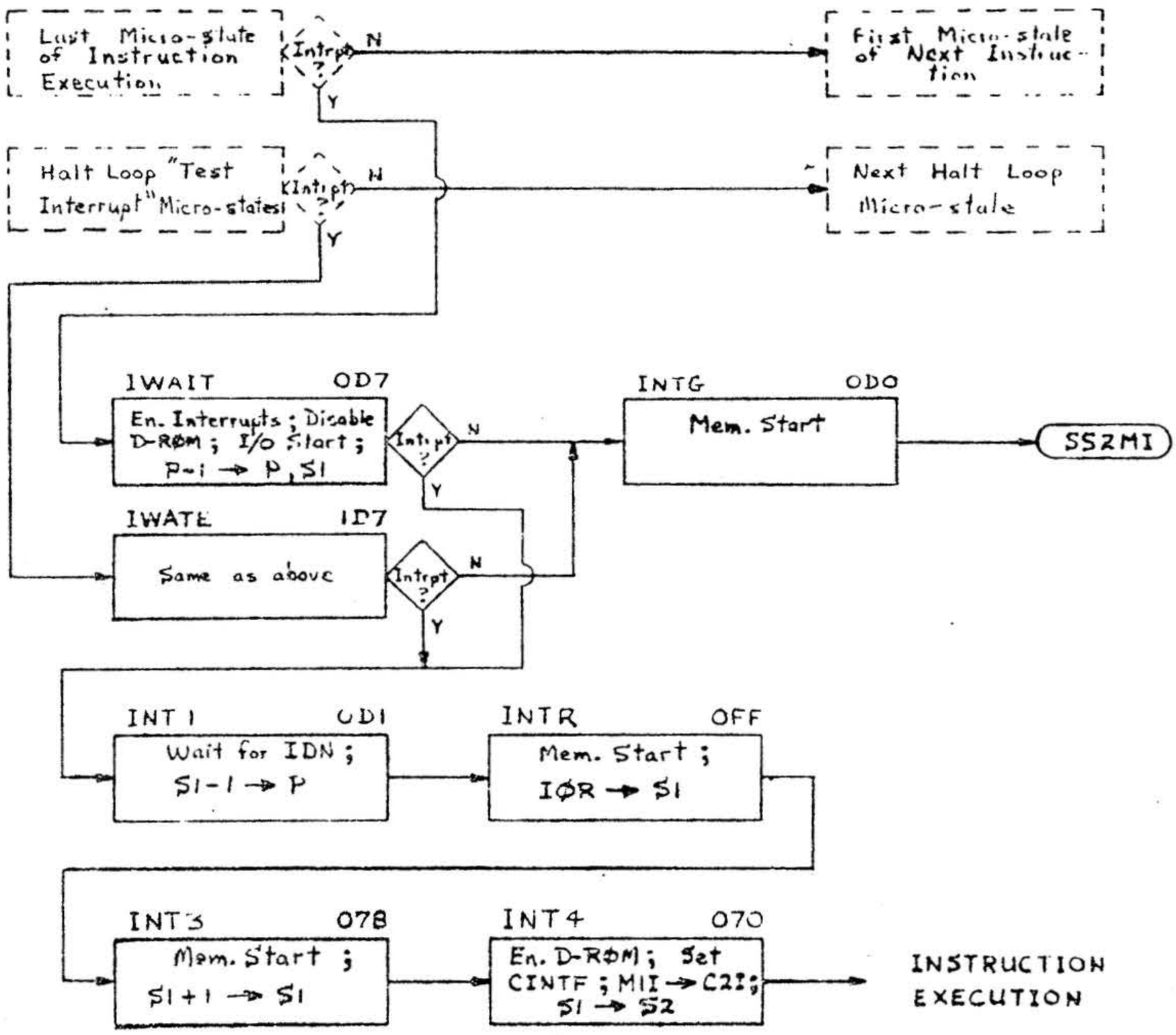
2.2.16.3 OUTPUT DATA TRANSFERS



OUTPUT DATA TRANSFERS
(ØAR, ØER, ØAB, ØME)

CODE IDENT NO.	SIZE	DWG NO	REV
21101	B	98A0887	B
SCALE		SHEET 43 OF 57	

2.2.17 INTERRUPT ROUTINE



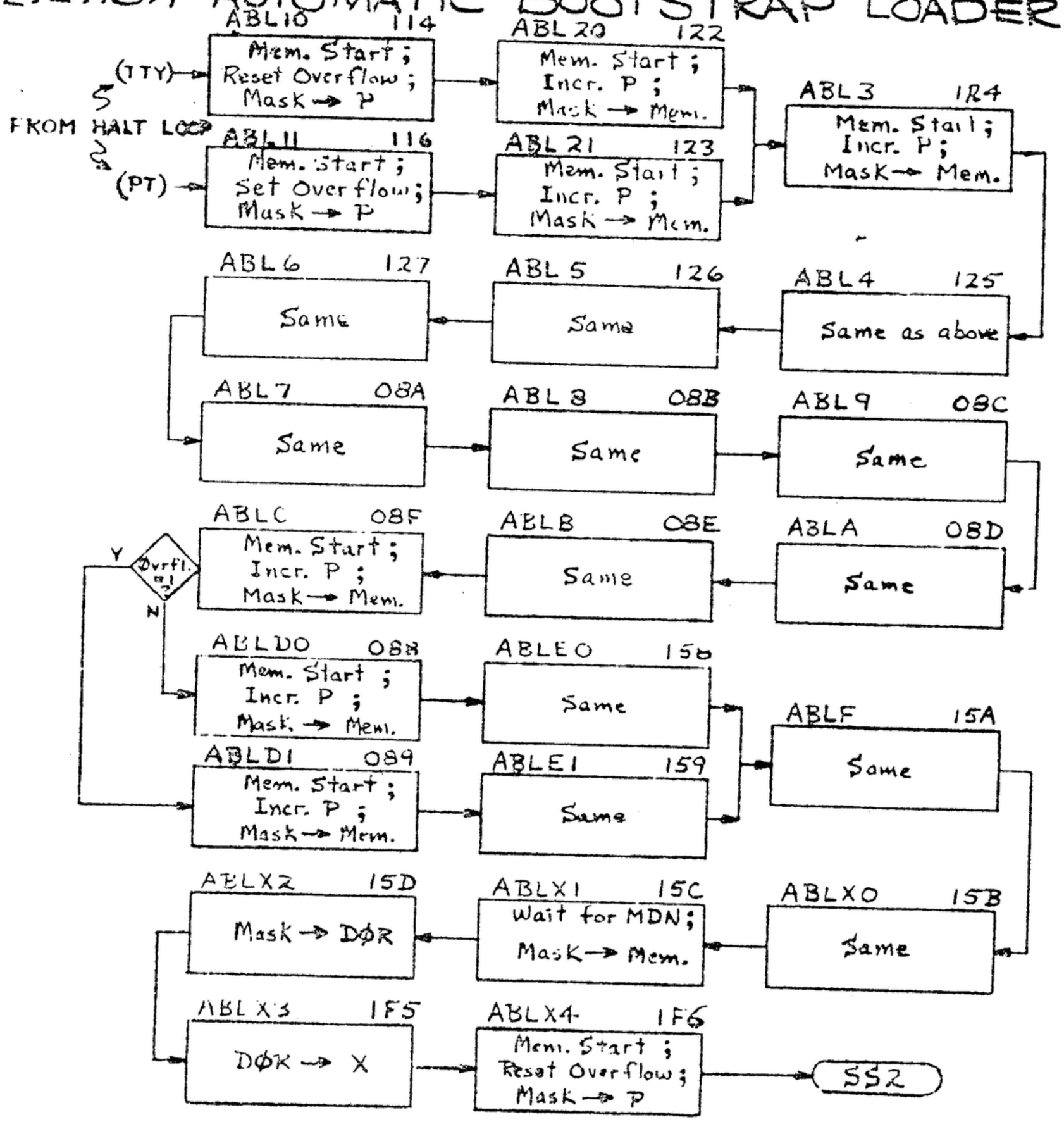
INTERRUPT ROUTINE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	B	98A0887	D

SCALE | SHEET 44 of 57

2.2.18 AUTOMATIC BOOTSTRAP LOADER ROUTINES

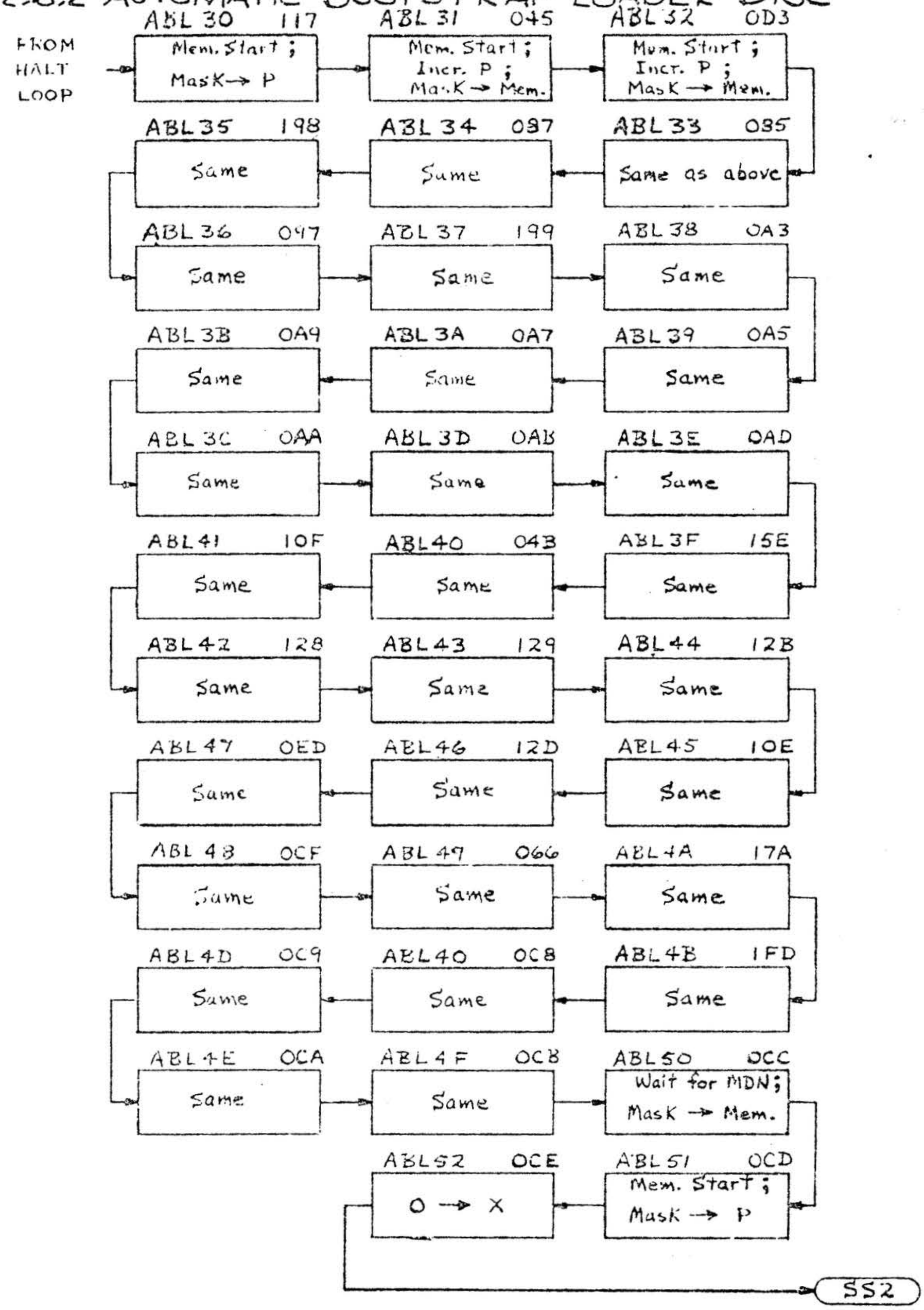
2.2.18.1 AUTOMATIC BOOTSTRAP LOADER TTY, PT



AUTO BOOTSTRAP LOADER TTY, PT

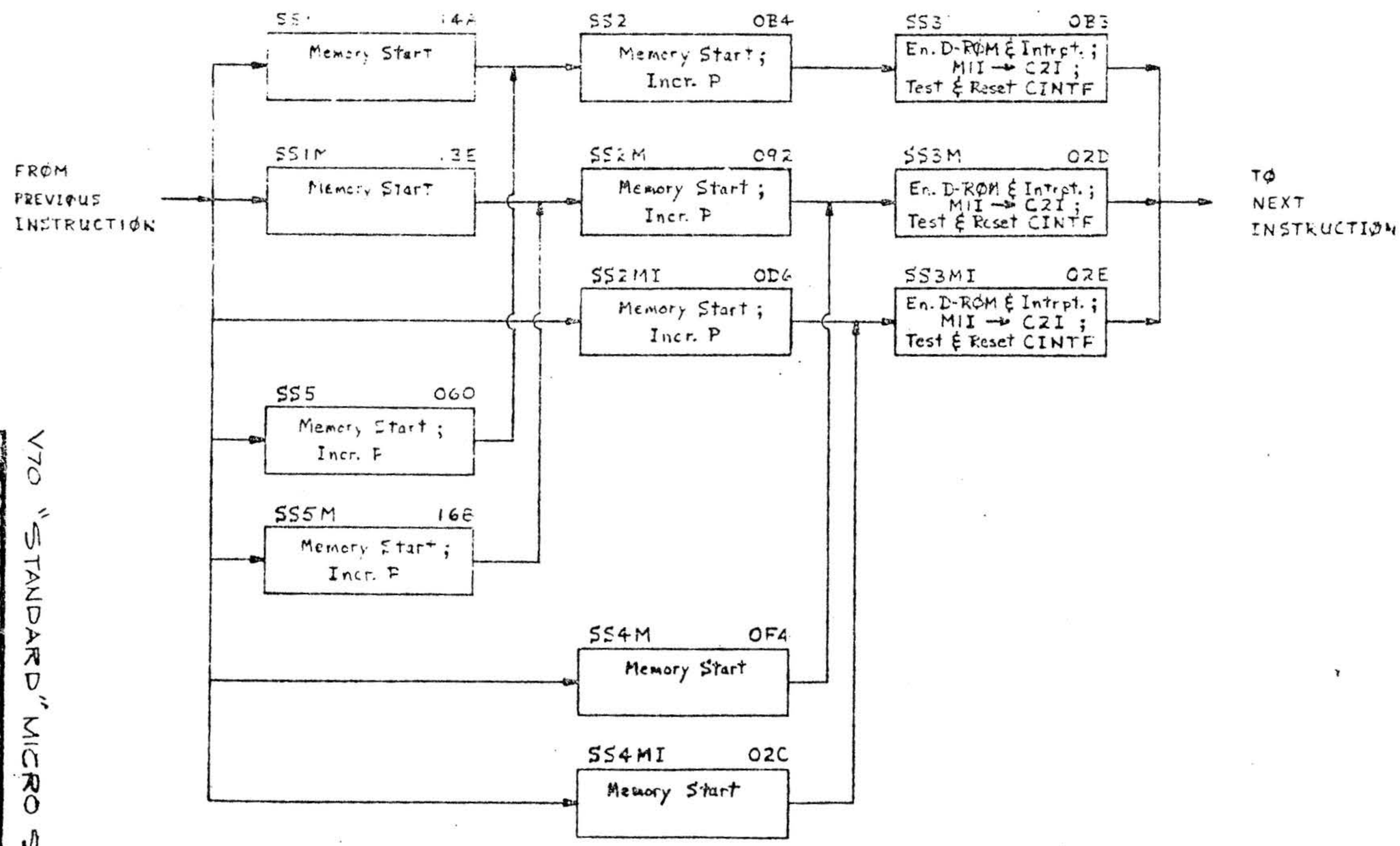
CODE IDENT. NO.	SIZE	DWG NO	REV
21101	B	98A0887	B
SCALE			

2.2.8.2 AUTOMATIC BOOTSTRAP LOADER DISC



AUTOMATIC BOOTSTRAP LOADER DISC

CODE IDENT NO.	SIZE	DWG NO	REV
21101	B	93A0887	B
SCALE		SHEET 47 OF 57	



V70 "STANDARD" MICRO STATE

21101 B

98A0887

B

2.2.19 V70 "STANDARD" MICRO STATE

2

1

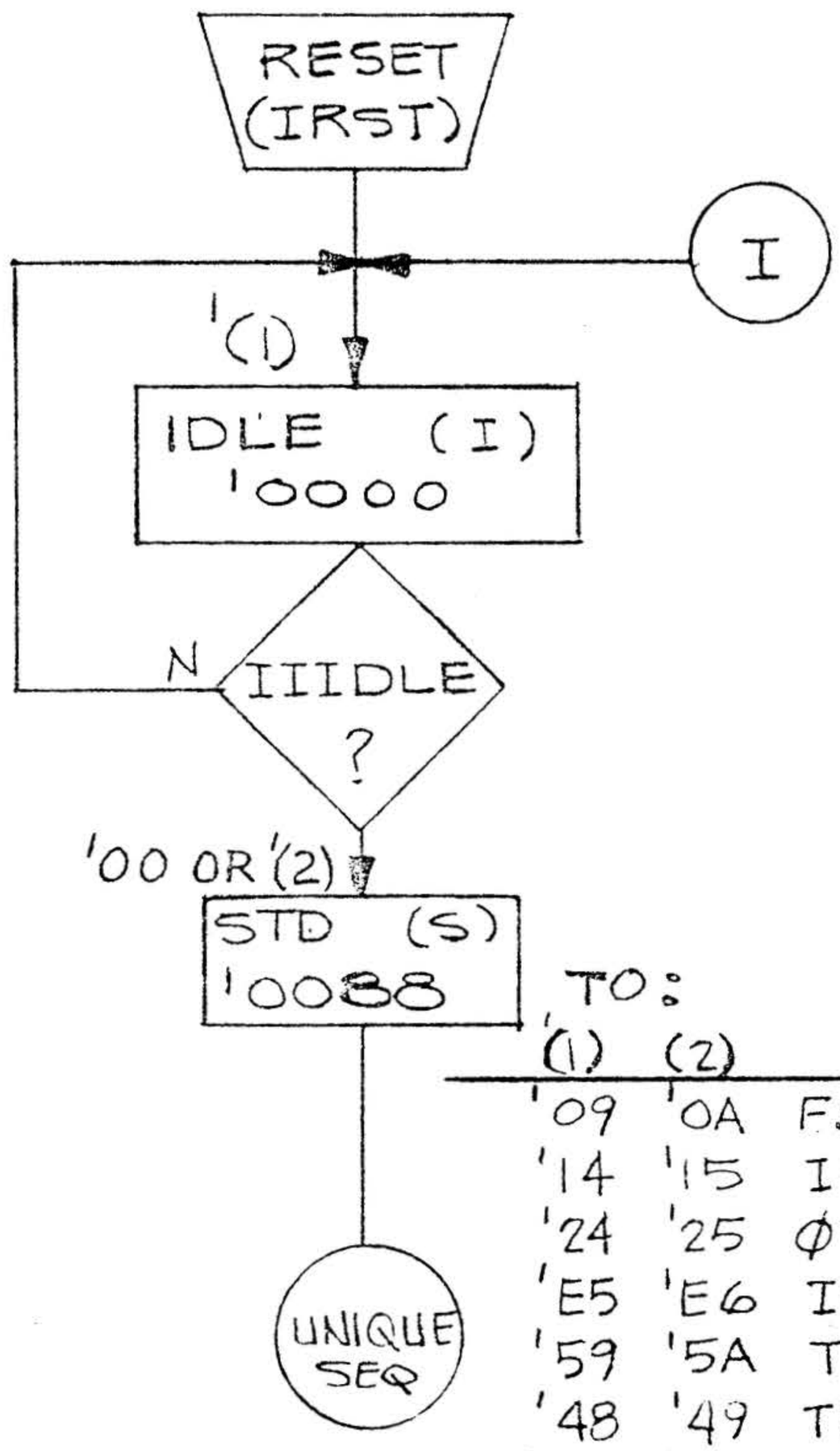
2.2.20 INPUT/OUTPUT (OPTION BOARD) MICRO FLOWS

2.2.20.1 IDLE STATE

NØTE: 1. 'XX INDICATES SØURCE ADDRESS ØF I/Ø CØNTRØL BUFFER WØRD

2. 'XXXX INDICATES I/Ø CØNTRØL BUFFER CØNTENTS

3. ALL NUMBERS ARE IN HEX.

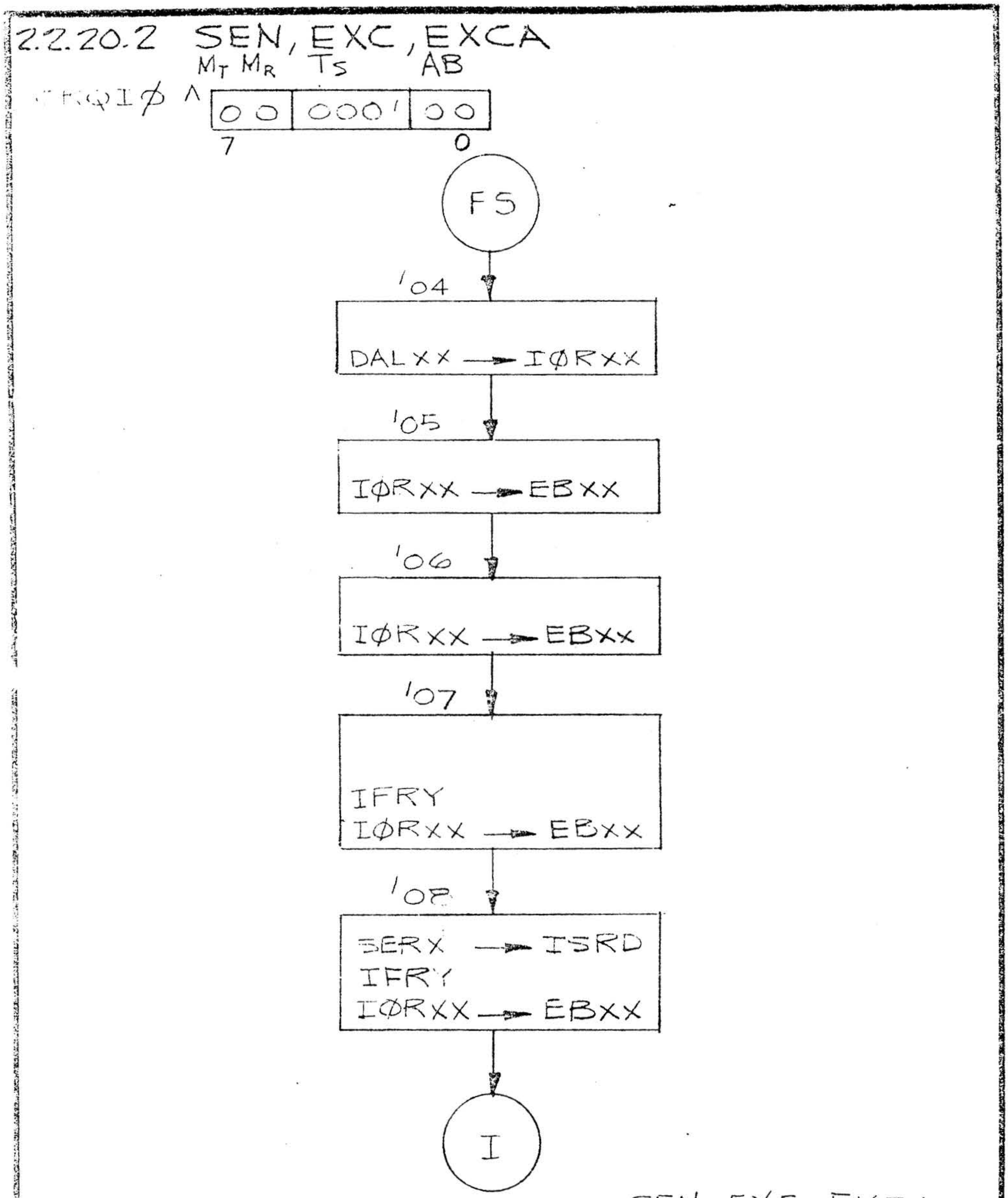


TO:

'(1)	'(2)		
'09	'OA	F.S.	FUNCTIØN STEP
'14	'15	IS	INPUT "
'24	'25	ØS	ØUTPUT "
'E5	'E6	INT.S.	INTERRUPT "
'59	'5A	TPIX	DMA IN "
'48	'49	TPØX	ØUT "
'74	'75	TPIF	HSDMA IN "
'64	'65	TPØF	ØUT "

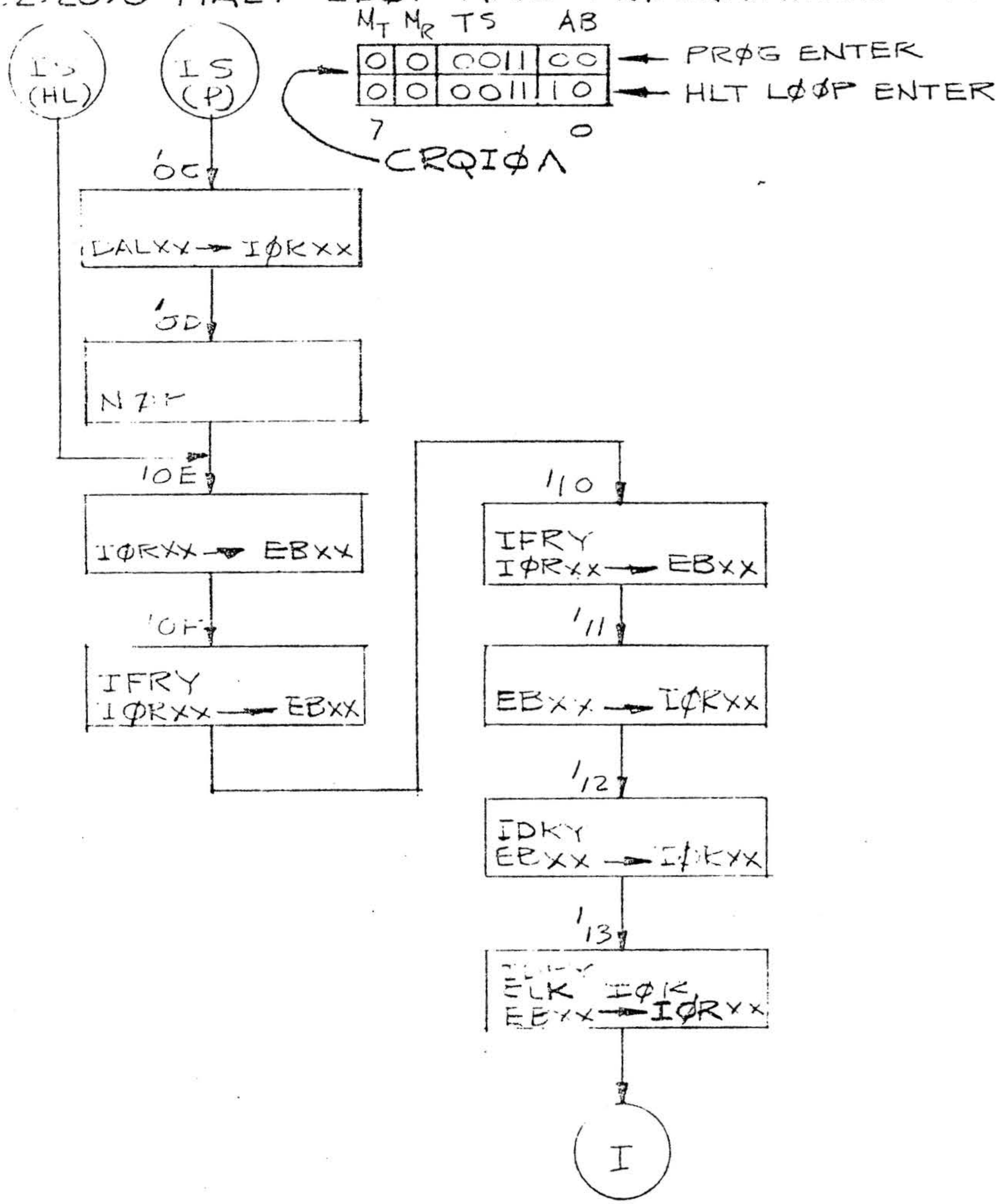
IDLE STATE

2.2.20.2 SEN, EXC, EXCA



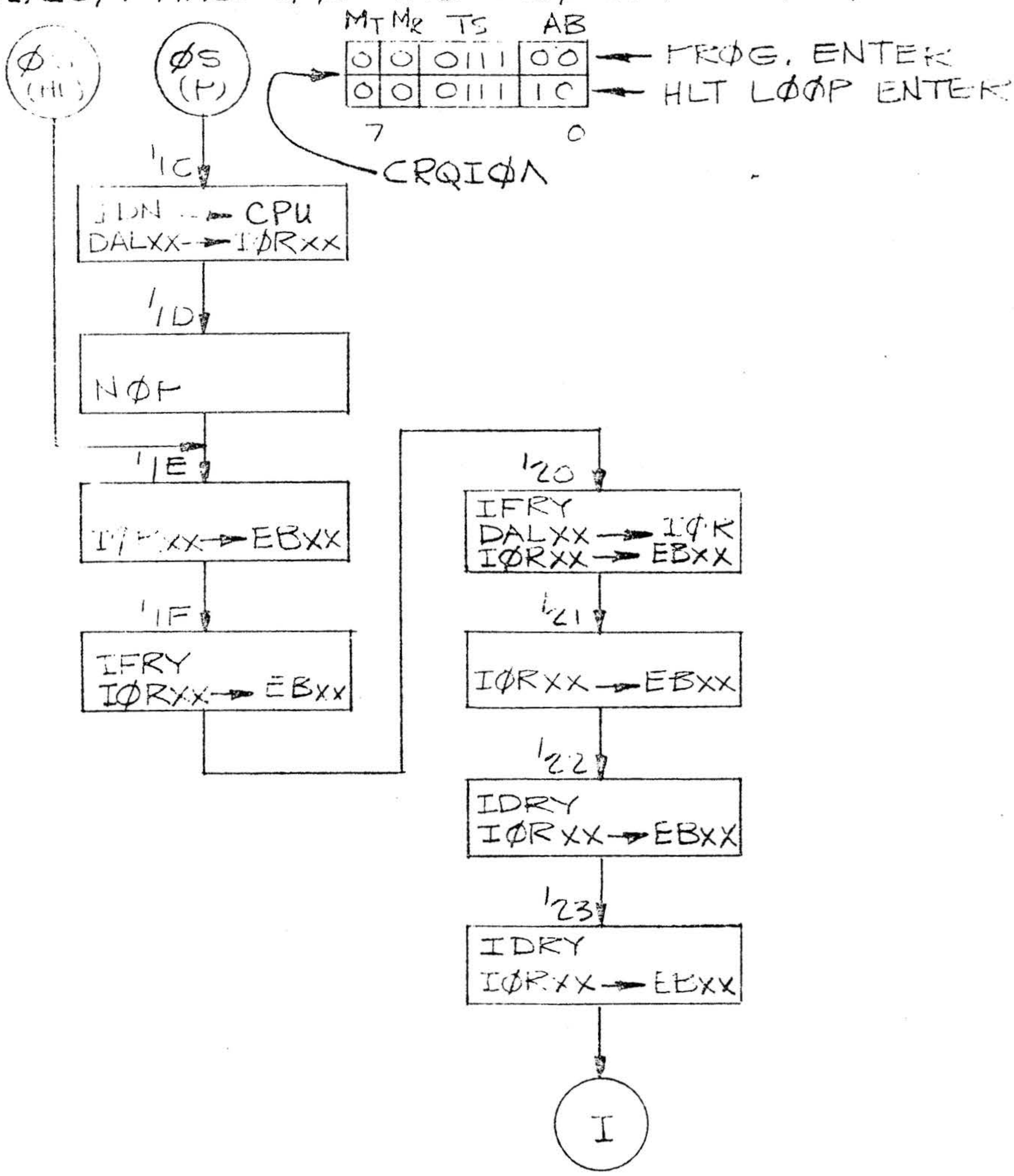
SEN, EXC, EXCA

2.2.20.3 HALT LØØP AND PRØGRAMMED INPUT



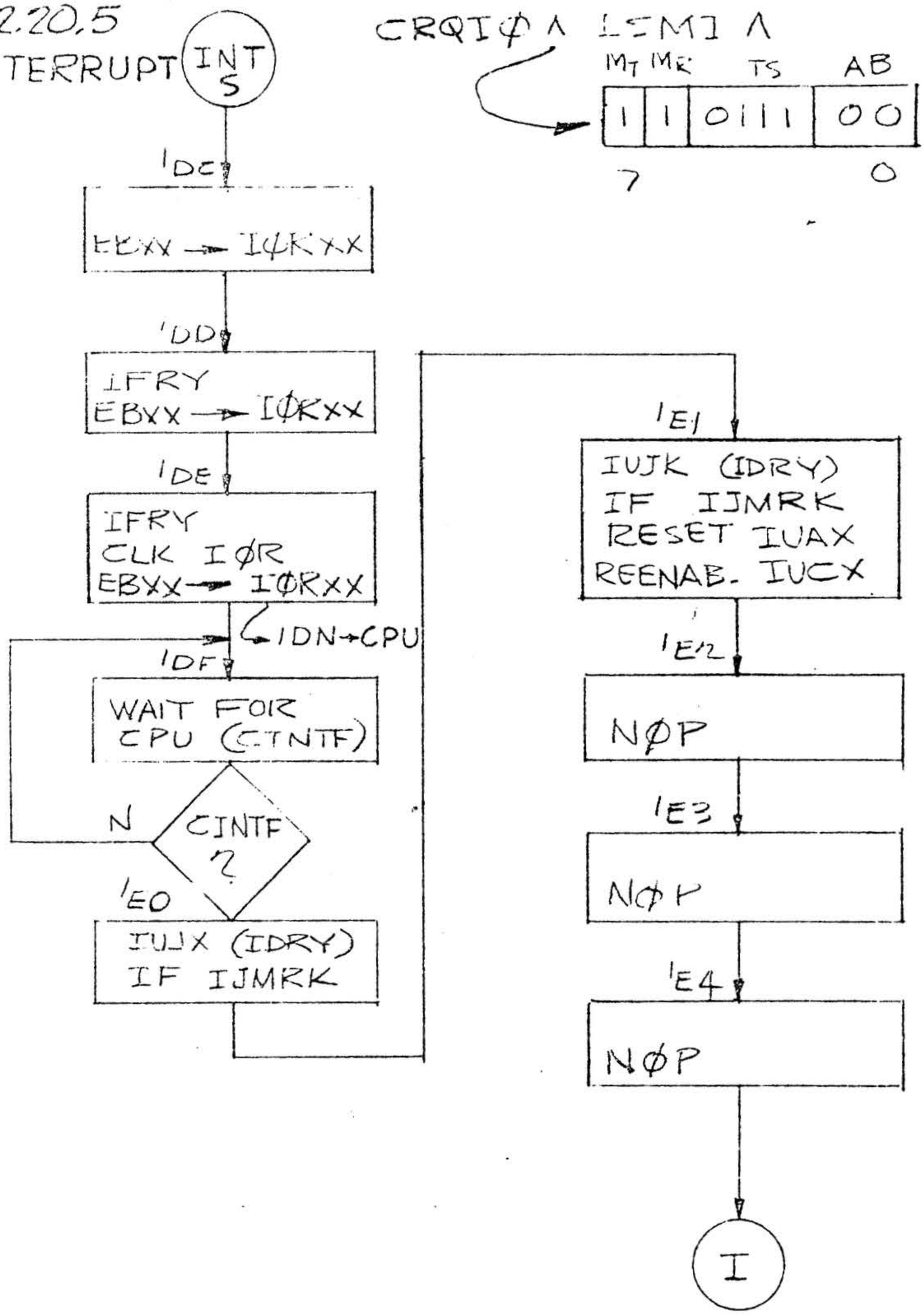
HALT LØØP AND
PRØGRAMMED INPUTS

2.2.20,4 HALT LØØP AND PRØGRAMMED ØUTPUT



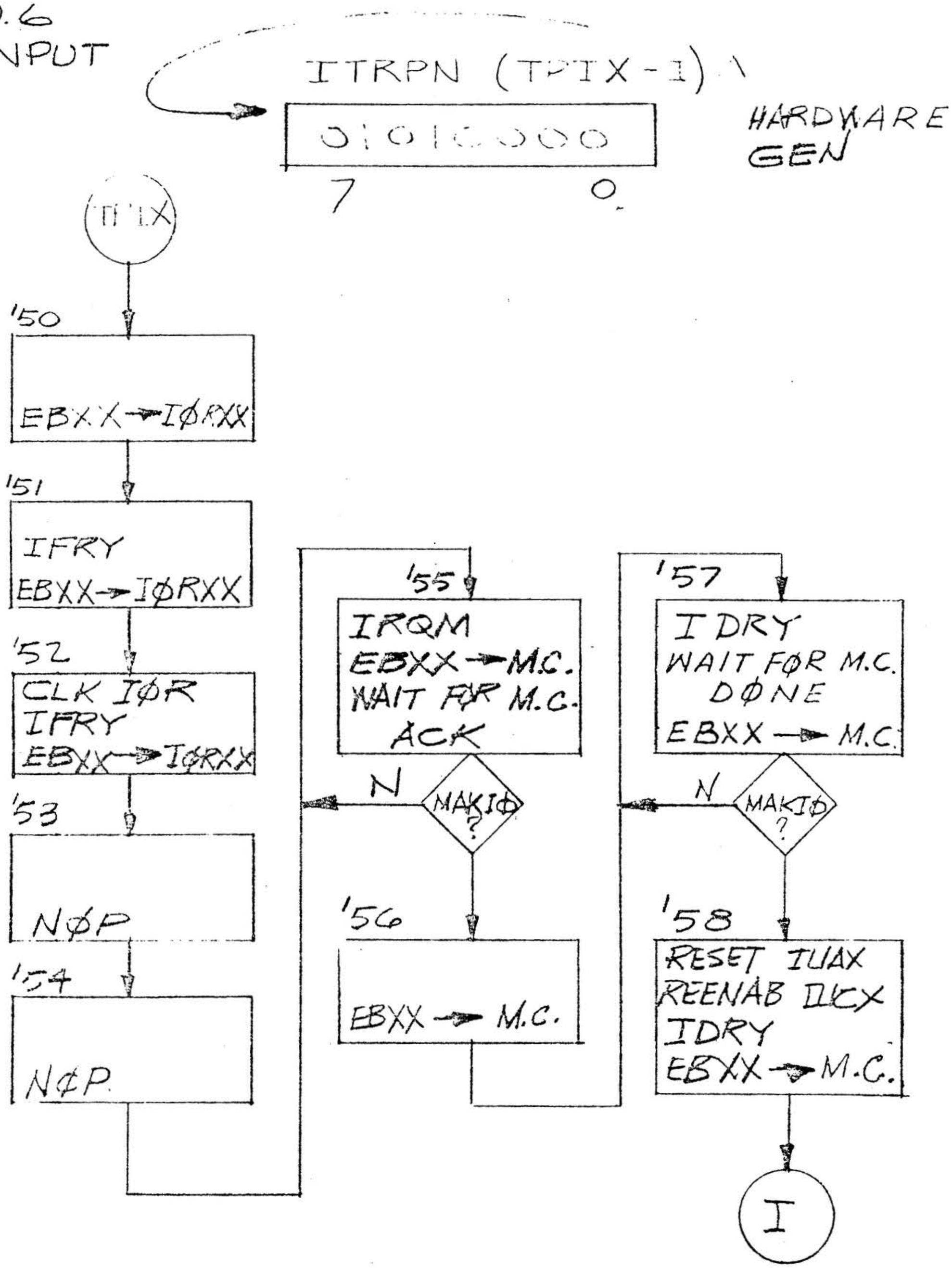
HALT LØØP AND
PRØGRAMMED ØUTPUTS

2.2.20.5
INTERRUPT



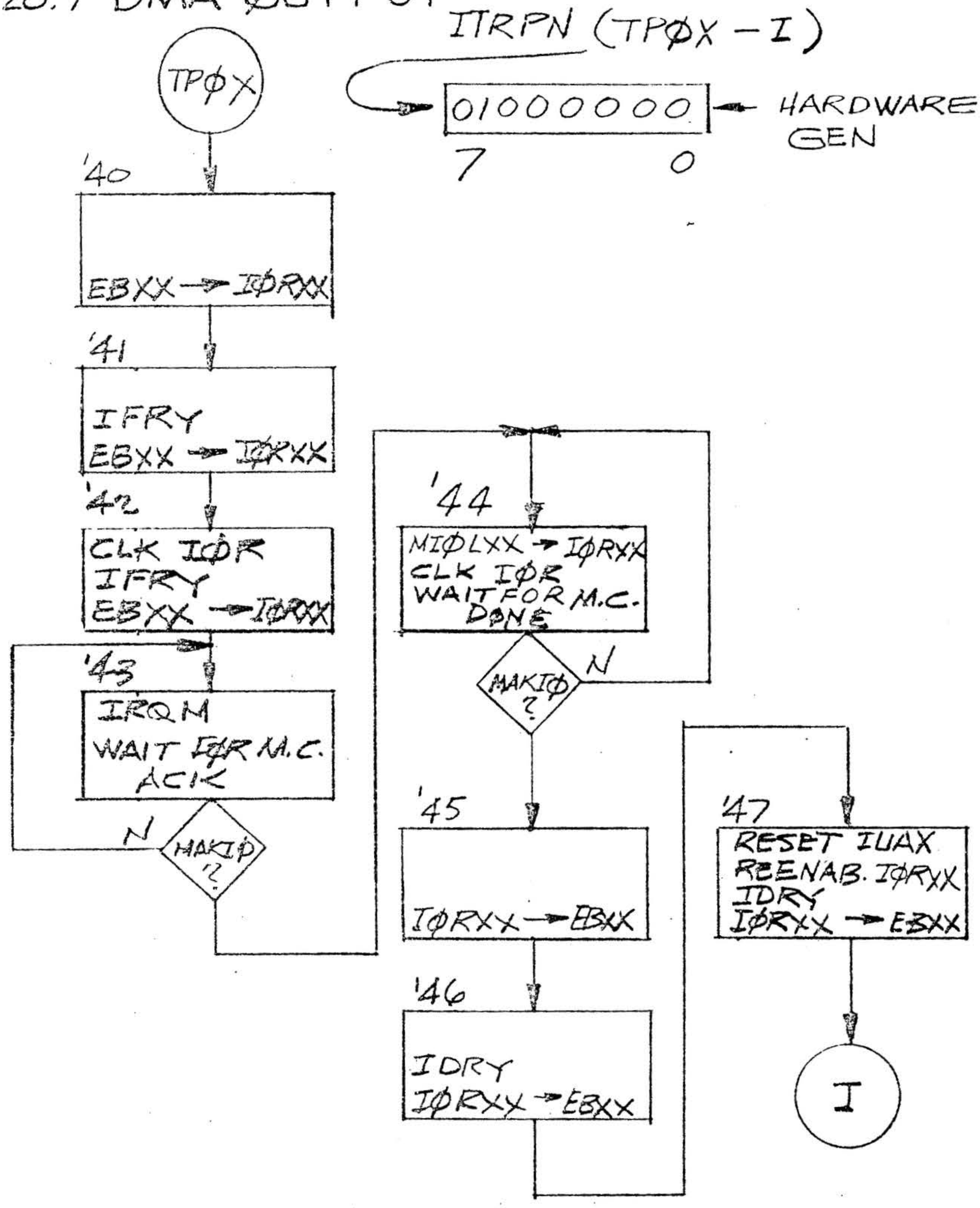
INTERRUPT

2.2.20.6
DMA INPUT



DMA INPUT (TPIX-I)

2.2.20.7 DMA ØUTPUT

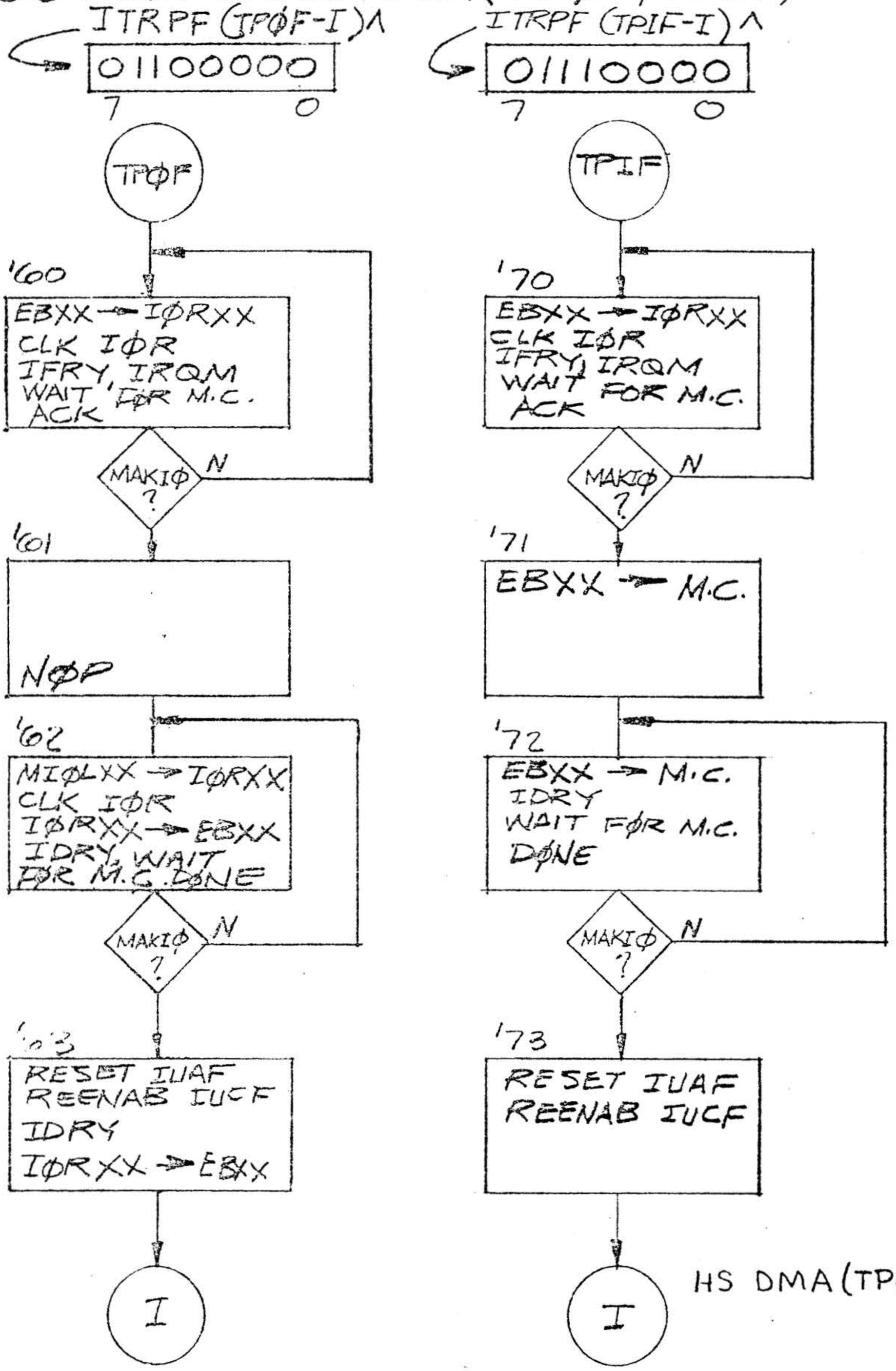


DMA ØUTPUT (TPØX – I)

varian data machines a varian subsidiary	CODE IDENT NO 21101		98A0887	B
			SH 56 OF 57	REV

96A0039-000B

2.2.20.8 HIGH SPEED DMA (TPØF, TPIF)



HS DMA (TPØF, TPIF)