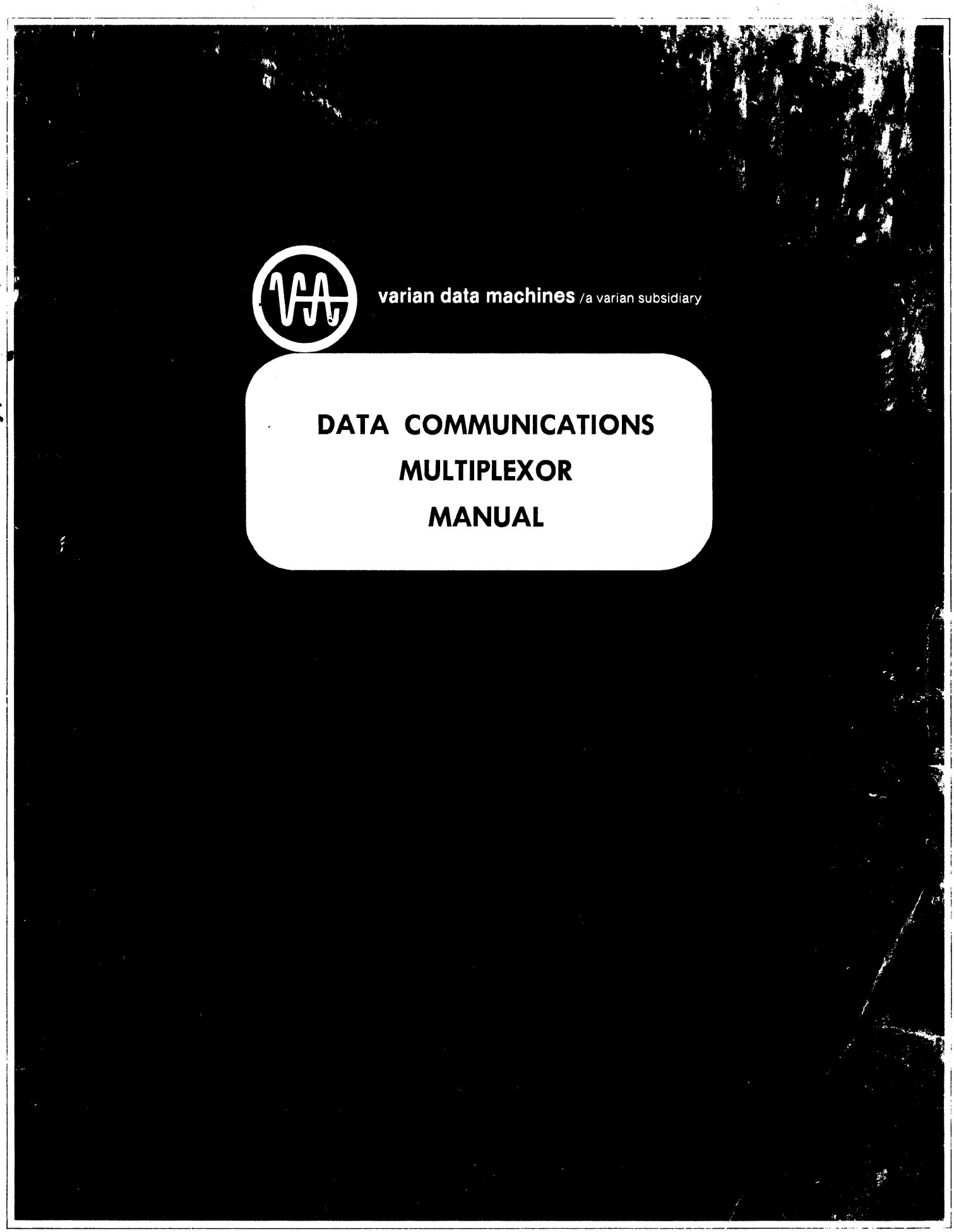

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DATA COMMUNICATIONS MULTIPLEXOR MANUAL

D. W. McCUTCHEON

DATA COMMUNICATIONS

MULTIPLEXOR MANUAL

Specifications Subject to Change Without Notice

NOTE

This manual covers the following models

5201 Right-hand 16-line multiplexor
5202 Left-hand 16-line multiplexor
5203 Right-hand 32-line multiplexor
5204 Left-hand 32-line multiplexor
5205 Maximum 64-line multiplexor
5301 Asynchronous RS232 modem line adapter
5302 Direct-connection RS232 line adapter
5303 Direct-connection current-loop line adapter
5304 Direct-connection relay line adapter
5305 Synchronous RS232 modem line adapter

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SECTION 2 MULTIPLEXOR UNIT

SECTION 5 SYNCHRONOUS RS232 MODEM LINE-ADAPTER

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SECTION 1
INTRODUCTION

The data communications multiplexor (DCM, figure 1-1) provides a low cost multiport interface between Varian Data Machines computers (with 620-type I/O) and up to 64 full-duplex serial devices. These devices can be serial peripherals and/or serial modems. The DCM consists of a multiplexor unit (MU), multiplexor buses, and several types of line adapter (LAD). The multiplexor bus scheme allows a wide variety of LADs to be added as new needs arise.

The DCM provides communication between the LADs and the computer via programmed I/O and direct-memory access (DMA). The multiplexor logic handles interrupts and trap requests (DMA) internally, and therefore does not require an external priority interrupt module (PIM) or a buffer interlace controller (BIC). For DMA operation, the DCM uses a control table stored in the computer memory. The table contains control characters, output and input block-lengths, output and input buffer-locations, and control information for each line. DCM accesses this table through the computer DMA with individual line addresses as pointers.

The individual lines are set up under program control to begin a transfer-in, transfer-out, or both (full duplex). Once the line is set up the multiplexor inputs or outputs data to/from the line on a demand basis using the DMA port of the computer. The program is interrupted only for a line error, control-character detection, or at completion of the transfer. The data are automatically packed or unpacked by the multiplexor hardware.

The character assembly, disassembly, parity generation, parity checking, modem control and buffering tasks are handled at the LAD level.

Communication between the line adapters and the multiplexor is via the multiplexor bus, which consists of an eight-bit bidirectional bus, 12 control lines, and 12 addressing lines. The multiplexor also provides six bit-rate lines for the asynchronous LADs. These lines go to all LAD locations, and are connected as needed. The frequency of these lines is determined by hardware jumpering options on the multiplexor.

The DCM is usually installed in a 620 or V73 I/O expansion chassis. It consists of the two multiplexor printed-circuit boards, the LAD complement, and one or two half-backplane assemblies. Systems that handle over 32 lines require two half-backplanes and consequently one entire I/O expansion chassis.

In this manual, section 2 describes the MU and associated buses. Each subsequent section describes one type of LAD.

Each section concludes with a subsection containing applicable programming information. General DCM programming is discussed at the end of section 2. In each LAD section, only programming peculiar to that line adaptor is discussed.

Logic diagrams and engineering drawings are contained in Volume 2 of this manual.

1.1 PHYSICAL DESCRIPTION

The DCM consists of two multiplexor printed circuit boards (MU), one or two special I/O backplanes, and up to 16 LAD boards (each LAD can handle four lines). Systems with 32 or fewer lines require only one backplane. See (figures 1-2 through 1-5). The DCM backplane(s) is (are) installed in a standard 620 or V73 I/O expansion chassis. A DCM system larger than 32 lines occupies the entire I/O chassis. If a single-backplane DCM occupies a chassis by itself, a righthand backplane should be used; but if the DCM is to share the chassis with an I/O backplane, a lefthand DCM backplane and a righthand I/O backplane must be used.

LADs are plugged into the backplane starting in slot 9 next to multiplexor board 1. The slot location of the LAD determines its addresses, i.e., the LAD in slot 9 handles lines 0 through 3 and the one in slot 10 handles lines 4 through 7 and so on. If the DCM systems is larger than 32 lines, slot 13 of the second backplane handles lines 32 through 35, etc. Interface to the modems or direct-connection terminals is through two connectors on the back of the LADs (see sections on individual LADs).

The DCM operates at 0 to 50 degrees C and 0 to 90 percent relative humidity (without condensation).

The MU requires a +5V dc ± 5 percent input at 3.5A while a typical LAD requires the following power inputs:

+ 5V dc ± 5 percent at 1.2 A

+ 12V dc ± 2.5 percent at 100mA

- 12V dc ± 2.5 percent at 150 mA

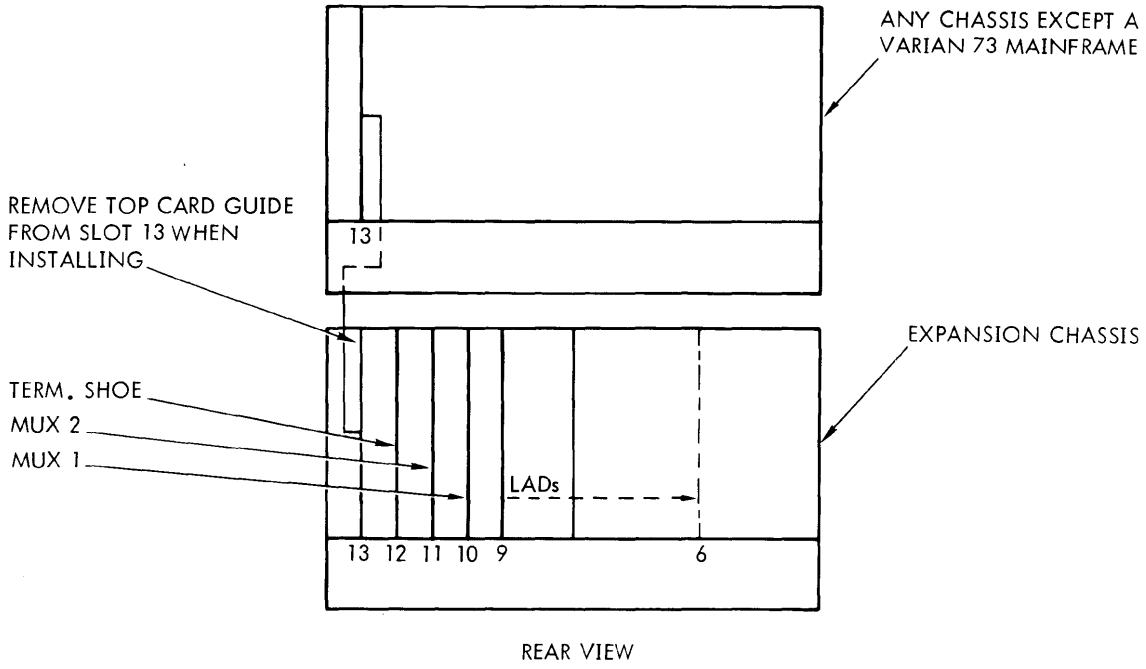
1.2 OPTIONS

The scan-length, scan-counter, and bit-rate lines can be hardwired to provide optimum performance for a particular system. There is also a priority scan in which the DCM resets to line 0 after the second service request. Details on these options are given in the applicable sections of the manual.

1.3 RELATED PUBLICATIONS

The following publications are aids to understanding the DCM and the systems to which it is applicable.

Varian 73 System Handbook	98 A 9906 010
Varian 620 100s Computer Handbook	98 A 9905 003



VTII-1751

Figure 1-2. Typical Installation

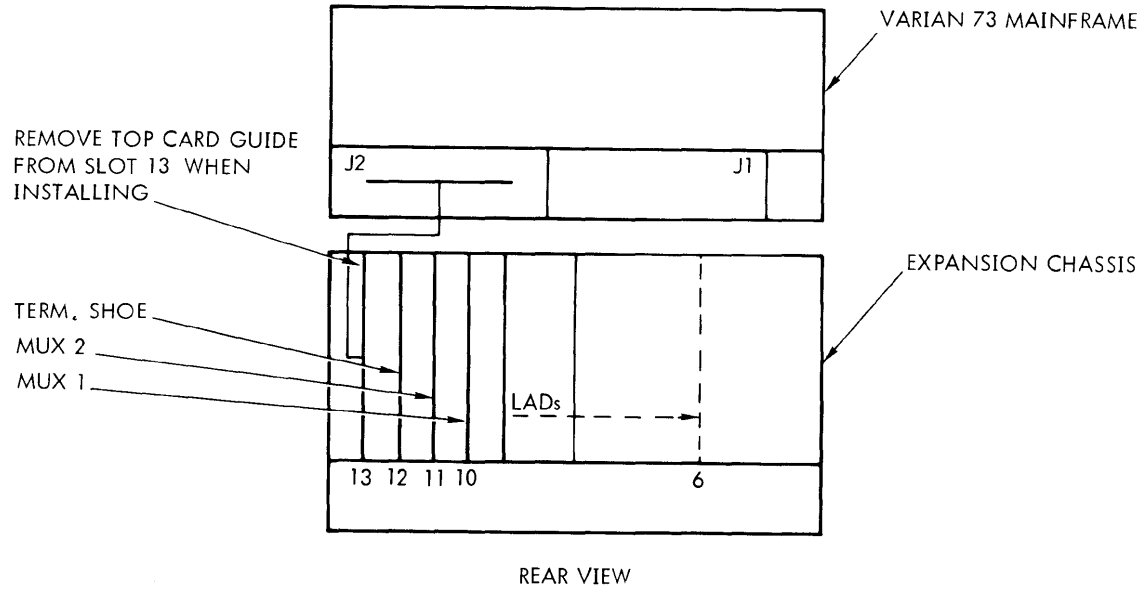


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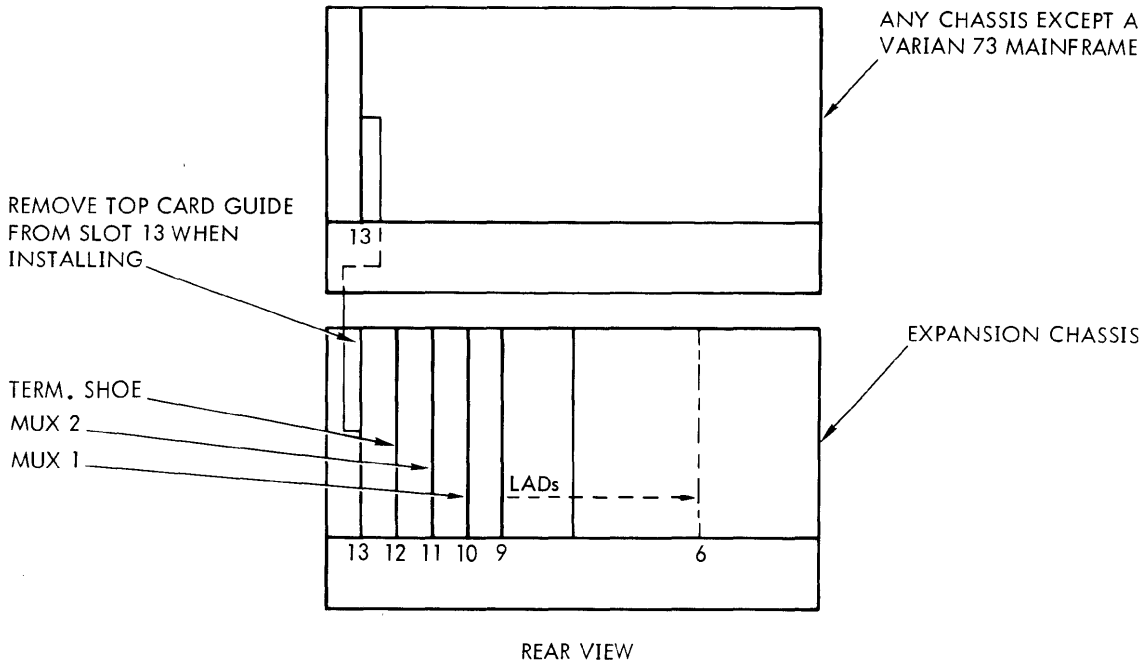
Figure 1-3. Installation with V73 Mainframe



VTII-1751

Figure 1-2. Typical Installation

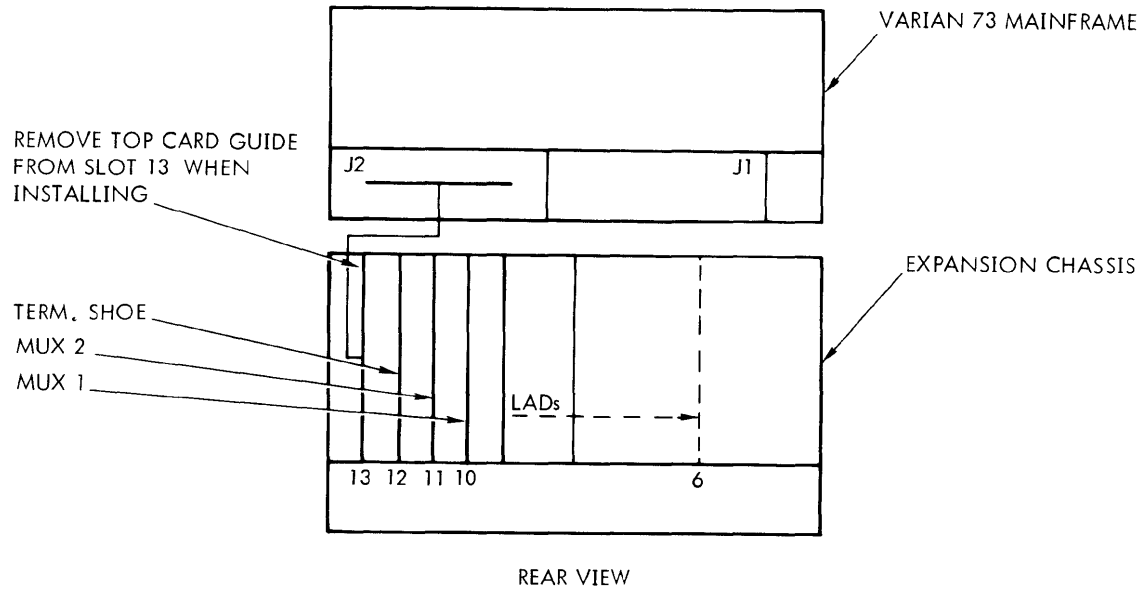


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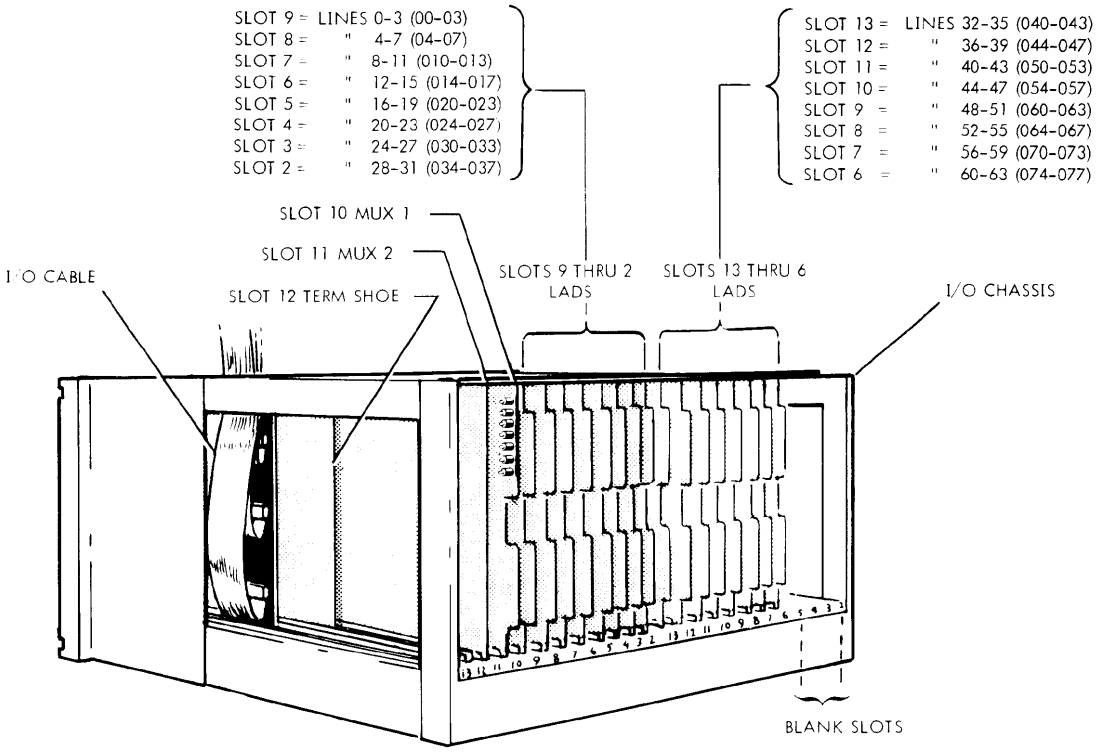
Figure 1-3. Installation with V73 Mainframe



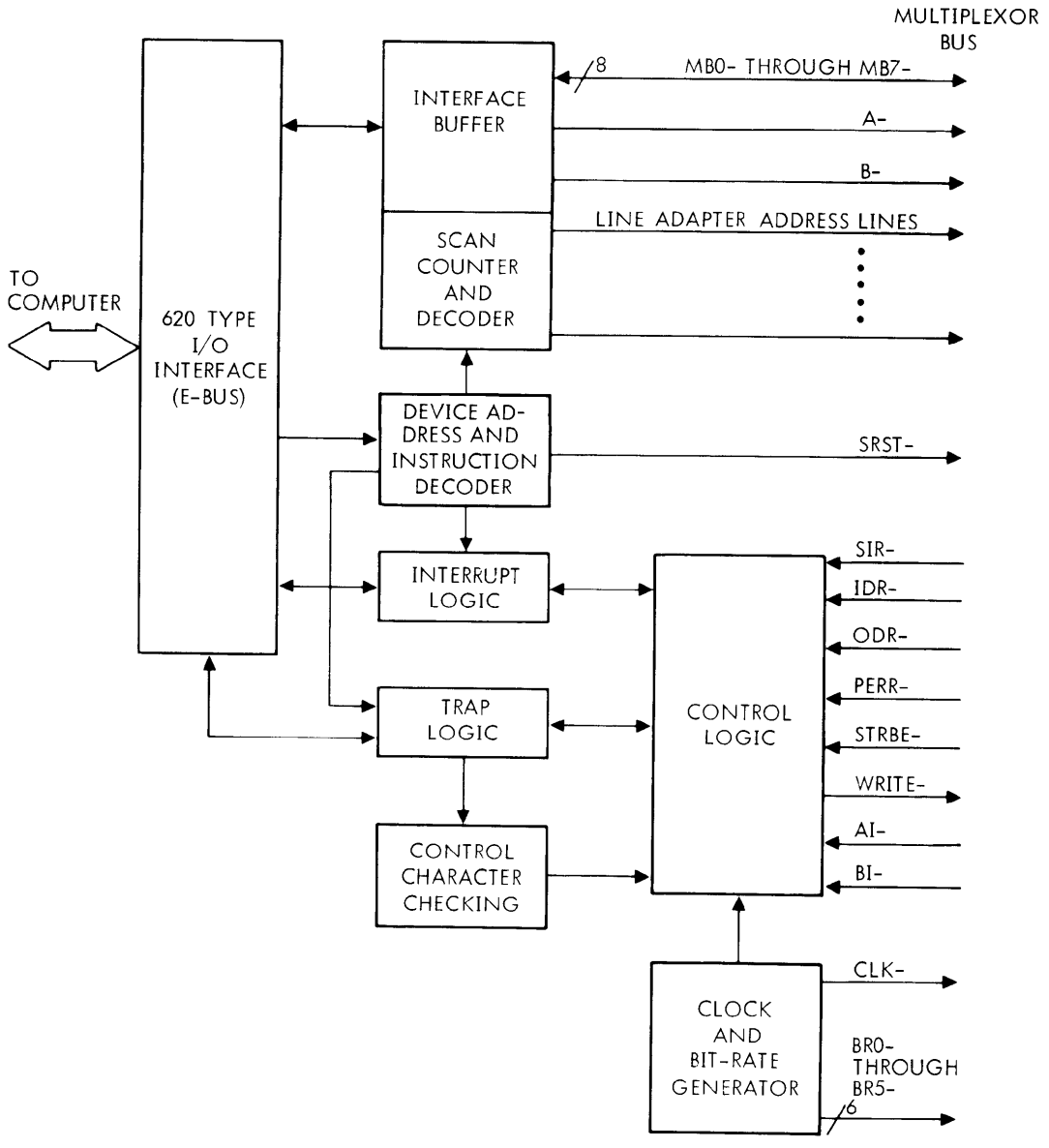
REAR VIEW

VTII-1910

Figure 1-5. 64-Line DCM Configurations

SECTION 2
MULTIPLEXOR UNIT

The multiplexor unit (MU, figure 2-1) is on two printed-circuit boards that fit slots in a special 620-type expansion chassis. It provides communication between the LADs and the computer via the programmed I/O and the DMA. The MU logic handles interrupts and (DMA) trap requests internally and therefore does not require an external priority-interrupt module (PIM) or a buffer-interlace controller (BIC). In DMA operations, the MU uses a control table in the computer memory. The control table contains control characters, output- and input-block lengths, output- and input-buffer addresses and control information for each line. MU access to this table is through the computer DMA, using the individual line addresses as pointers.



VTII-1679-1

Figure 2-1. DCM Multiplexor-Unit Simplified Block Diagram

circuit board that contains 88 integrated circuits. The following paragraphs describe the jumpering options on this board.

Bit-Rate Selection: Board 1 contains two odd-bit-rate counters (variable bit rate counters). Counter number one provides for dividing the input or base frequency by any even number from 2 to 8190, and counter number two divides the base frequency by any even number for 2 to 1022. The output of these counters can then clock the asynchronous LADs. The frequency of the output is varied by adding (or deleting) jumper clips corresponding to the set bits of a binary number determined by the formula:

$$n = \frac{\text{base frequency}}{2 \times \text{desired frequency}} - 1$$

where n is rounded to the nearest whole number and converted to binary; and is less than 4096 for counter one, and less than 512 for counter two.

Tables 2-2 and 2-3 give the jumper locations corresponding to the various bits and to the base-frequencies of counters 1 and 2, respectively. The outputs of counters 1 and 2 are at board-1 points X33 and X34, respectively. Table 2-4 gives values of n for some common frequencies.

Board 1 provides six clocks for the LADs. The frequencies of these clocks are determined by jumpers (table 2-5). The clocks are jumpered into the LADs at the backplane per system requirements.

Table 2-2 Odd-Bit-Rate Counter 1

Jumper Locations

Value of n (Binary Weight) Bit	Jumper Locations (Board 1)
0 (1)	X15 to W15
1 (2)	X16 to W16
2 (4)	X17 to W17
3 (8)	X18 to W18 *
4 (16)	X19 to W19
5 (32)	X20 to W20 *
6 (64)	X21 to W21 *
7 (128)	X22 to W22 *
8 (256)	X23 to W23
9 (512)	X24 to W24 *
10 (1024)	X25 to W25
11 (2048)	X26 to W26 *

Base-Frequency Selection

Base Frequency	Jumper Locations (Board 1)
9.8304 MHz	V19 A to V14 *
4.9152 MHz	V20 to V14
2.4576 MHz	V15 to V14
1.2288 MHz	V16 to V14
0.6144 MHz	V17 to V14
0.3072 MHz	V18 to V14

* Indicates standard configuration that provides an output frequency of 1760 Hz (16 times 110 Hz).

Note: Asynchronous LADs require a clock frequency that is 16 times the line bit-rate.

Table 2-3. Odd-Bit-Rate Counter 2

Jumper Locations

Value of n (Binary Weight) Bit	Jumper Locations (Board 1)
0 (1)	X7 to W7
1 (2)	X8 to W8
2 (4)	X9 to W9
3 (8)	X10 to W10
4 (16)	X11 to W11
5 (32)	X12 to W12
6 (64)	X13 to W13
7 (128)	X14 to W14

Base-Frequency Selection

Base Frequency	Jumper Locations (Board 1)
9.8304 MHz	V19B to V13 *
4.9152 MHz	V20 to V13
2.4576 MHz	V15 to V13
1.2288 MHz	V16 to V13
0.6144 MHz	V17 to V13
0.3072 MHz	V18 to V13

* Indicates standard configuration.

Note: Asynchronous LADs require a clock frequency that is 16 times the line-bit rate.

Table 2-5. Bit-Rate Selection (continued)

Line Adapter Clock Inputs (at Backplane)

Line	Input Pin	Remarks
0	92	Speed A for RS232 asynchronous LAD, input for direct-connection LAD, test clock for RS232 synchronous LAD
	94	Speed B for RS232 asynchronous LAD
1	93	Speed A for RS232 asynchronous LAD, input for direct-connection LAD
	91	Speed B for RS232 asynchronous LAD
2	98	Speed A for RS232 asynchronous LAD, input for direct-connection LAD
	95	Speed B for RS232 asynchronous LAD
3	97	Speed A for RS232 asynchronous LAD, input for direct-connection LAD
	96	Speed B for RS232 asynchronous LAD

The RS232 asynchronous LAD requires two clocks per line, the direct-connection LAD requires one clock per line, and the RS32 synchronous LAD requires only one clock input for testing.

Scan-length selection: The number of lines scanned by the multiplexor is adjustable (table 2-6). The standard configuration depends on the DCM model number (i.e., 16, 32 or 64).

Priority-mode selection: The DCM can be put in the priority mode by jumpering point W6 to W5 on board 1. This simply causes the DCM to begin scanning at line zero after alternate service requests (either from a line or from the computer). Normally the DCM continues to scan lines sequentially. When priority mode is selected, the higher-speed lines should have the numerically lower addresses. This mode should only be used when a few high-speed lines are being run concurrently with a large number of low-speed lines. If the line speeds are all relatively close together, this mode should not be used. In priority mode, the scan length should be as close to the actual number of lines in use as possible.

Table 2-6. Scan-Length Selection

Scan Length	Jumpers (Board 1)
4 lines	Points W4, W3, W2 and W1 open
8 lines	X3 to W3
16 lines	X3 to W3; X1 to W1
32 lines	X3 to W3; X1 to W1; X2 to W2
64 lines	X3 to W3; X1 to W1; X2 to W2; X4 to W4

2.1.1.2 Multiplexor Unit Board 2

Board 2 contains the interface to the computer I/O. It is packaged on a 7-3/4-by-12-inch multiplexor printed circuit board that contains 90 integrated circuits. The following paragraphs describe the jumpering options on the board.

Device-Address Selection: The standard device-address is 070, but can be changed to any address from 00 to 077 by jumpers (table 2-7).

Table 2-9. Control Table (LCB) Beginning-Address Selection

Beginning Address Octal	Jumpers (Board 2) W15 V15	W14 V14	W13 V13	W12 V12	W11 V11	W10 V10	W9 V9	Beginning Address Octal	Jumpers (Board 2) W15 V15	W14 V14	W13 V13	W12 V12	W11 V11	W10 V10	W9 V9
00000	X	X	X	X	X	X	X	40000	X	-	X	X	X	X	X
01000	X	X	X	X	X	X	-	41000	X	-	X	X	X	X	-
02000	X	X	X	X	X	-	X	42000	X	-	X	X	X	-	X
03000	X	X	X	X	X	-	-	43000	X	-	X	X	X	-	-
04000	X	X	X	X	-	X	X	44000	X	-	X	X	-	X	X
05000	X	X	X	X	-	X	-	45000	X	-	X	X	-	X	-
06000	X	X	X	X	-	-	X	46000	X	-	X	X	-	-	X
07000	X	X	X	X	-	-	-	47000	X	-	X	X	-	-	-
10000	X	X	X	-	X	X	X	50000	X	-	X	-	X	X	X
11000	X	X	X	-	X	X	-	51000	X	-	X	-	X	X	-
12000	X	X	X	-	X	-	X	52000	X	-	X	-	X	-	X
13000	X	X	X	-	X	-	-	53000	X	-	X	-	X	-	-
14000	X	X	X	-	-	X	X	54000	X	-	X	-	-	X	X
15000	X	X	X	-	-	X	-	55000	X	-	X	-	-	X	-
16000	X	X	X	-	-	-	X	56000	X	-	X	-	-	-	X
17000*	X	X	X	-	-	-	-	57000	X	-	X	-	-	-	-
20000	X	X	-	X	X	X	X	60000	X	-	-	X	X	X	X
21000	X	X	-	X	X	X	-	61000	X	-	-	X	X	X	-
22000	X	X	-	X	X	-	X	62000	X	-	-	X	X	-	X
23000	X	X	-	X	X	-	-	63000	X	-	-	X	X	-	-
24000	X	X	-	X	-	X	X	64000	X	-	-	X	-	X	X
25000	X	X	-	X	-	X	-	65000	X	-	-	X	-	X	-
26000	X	X	-	X	-	-	X	66000	X	-	-	X	-	-	X
27000	X	X	-	X	-	-	-	67000	X	-	-	X	-	-	-
30000	X	X	-	-	X	X	X	70000	X	-	-	-	X	X	X
31000	X	X	-	-	X	X	-	71000	X	-	-	-	X	X	-
32000	X	X	-	-	X	-	X	72000	X	-	-	-	X	-	X
33000	X	X	-	-	X	-	-	73000	X	-	-	-	X	-	-
34000	X	X	-	-	-	X	X	74000	X	-	-	-	-	X	X
35000	X	X	-	-	-	X	-	75000	X	-	-	-	-	X	-
36000	X	X	-	-	-	-	X	76000	X	-	-	-	-	-	X
37000	X	X	-	-	-	-	-	77000	X	-	-	-	-	-	-

* = Standard configuration.

Note: X indicates that a jumper is required.

Table 2-10. DMA Mode-Selection Jumpers

High-Speed DMA	Jumpers (Board 2)		Normal DMA	Jumpers (Board 2)	
1	S1 to S2	FTEN–	1	Z1 to Z2	FSTRP–
2	Z3 to Z2	FSTRP–	2	X1 to X2	FSTRP+
3	X3 to X2	FSTRP+	3	Y1 to Y2	FSTDP+
4	Y1 to Y2	FSTDP+			

Note: Remove all existing jumpers when switching from one mode to another.

2.1.2.1 E-Bus

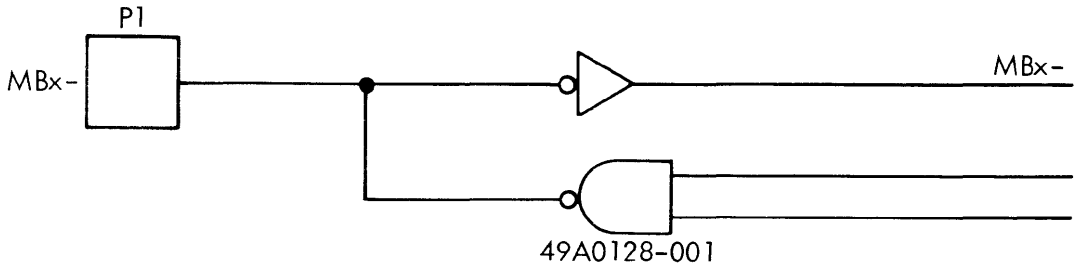
The DCM provides a standard interface to the 620-type I/O bus (see 620/f-100 Maintenance Manual 98 A 9908 150 for a description of the interface). Since the DCM generates the trap requests and interrupt requests, it must be assigned a position on the I/O priority line. The trap addressing for data is handled by software assignment, but the interrupt addresses, priority assignment, the device code, and the line-control-block addresses are determined by strapping.

2.1.2.2 Multiplexor Bus

The MU interfaces with the LADs over a 38-line common bus comprising an eight-bit bidirectional bus (figure 2-3), eight control lines, six bit-rate lines, twelve addressing lines, a clock line, two line-error lines, and a system-reset line (figure 2-1).

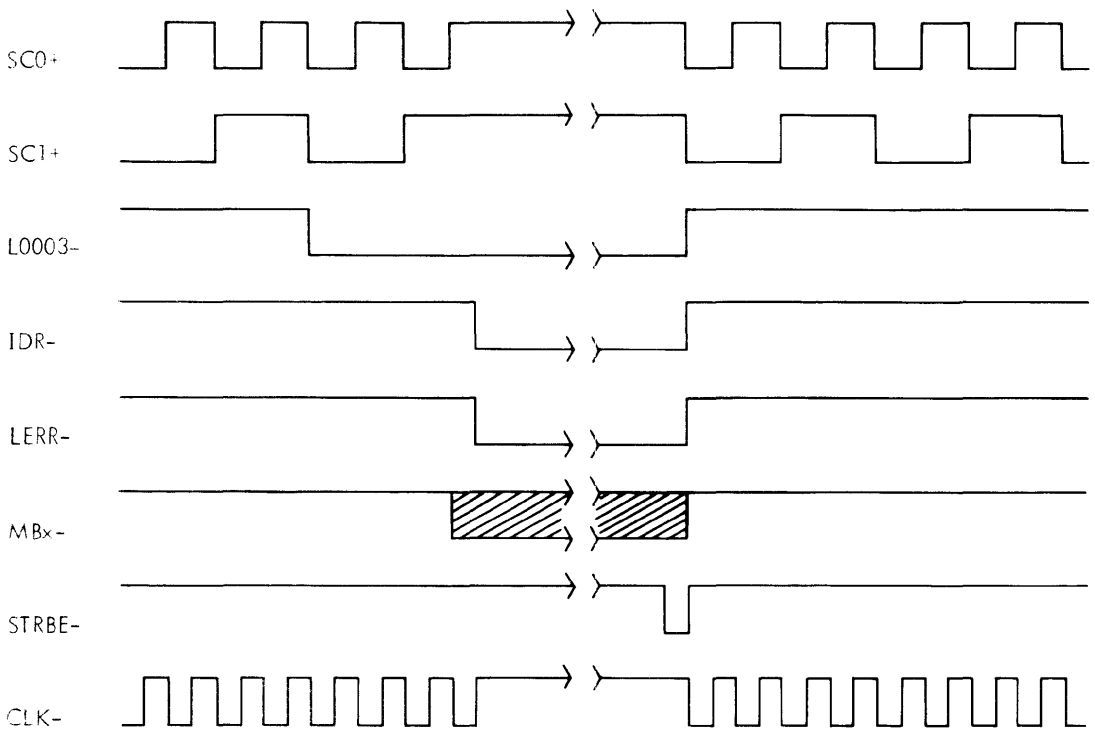
The LAD should present only one high-speed TTL load (2.0 milliamperes) to any of the MU output lines. Except for the bidirectional bus, which requires a 48-milliampere sink, all lines driven by the LAD are driven with open-collector gates capable of sinking 16 milliamperes in the low state.

Figures 2-4, 2-5, and 2-6 show the relative timing for a data-input request, a status-input request, and a data-output request, respectively. Data are stable before the leading edge of the STRBE– pulse.



VTII-1754A

Figure 2-3. LAD Interface to the Eight-Bit Bidirectional Bus



VTII-1755

Figure 2-4. Data-Input-Request Timing

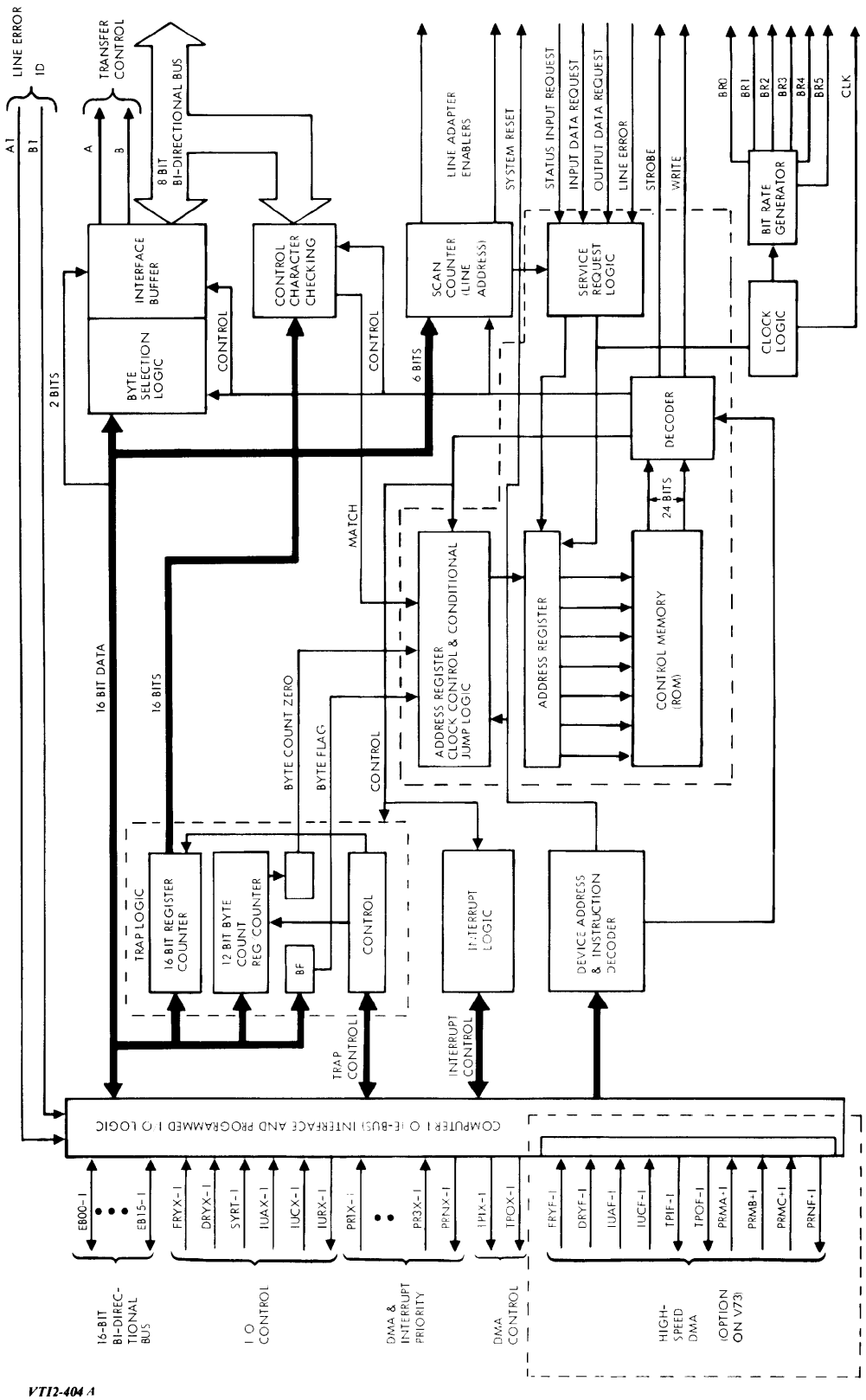


Figure 2-7. MU Detailed Block Diagram

(SCB0- and SCB1-) and the most-significant output (SCB5+ and SCB5-). Each LAD receives one of the enabling terms (the actual term depends on what slot it occupies) SCB0-, SCB1-, SCB5+ or SCB5-. SCB5+ enables the LADs below line number 32 and SCB5- enables those above 31. SCB0- and SCB1- are decoded on the LAD for the individual line scanning.

The scan counter is clocked at 614,400 Hz (SCCLK+) as long as the control memory is in idle (CMB00- low). Once CMB00- goes high, SCLKE+ is held low, holding the scan counter at the line number being serviced.

The scan counter is loaded by LSC-. In normal operation, when the control memory is in idle, the scan counter is parallel-loaded with zeros each time it reaches a predetermined count. If the priority mode is selected, the scan counter is loaded with zeros after every other service request (SSCN+). During a control sequence the scan counter is also loaded with a line address over the programmed I/O. In this case, DTOA- enables LSC-, DTOA+ gates the six least-significant bits of the E-bus to the counter, and the counter is clocked at FSDRY+ time.

2.2.4 Instruction Decoder (MU Board 2)

This block contains the data-transfer-out (DTO) and data-transfer-in (DTI) flip-flops for data-transfer control, as well as the gating for decoding the DCM external-control instructions.

The less-significant portion of the device address is decoded from EB01+, and EB02+ to obtain DVC0- through DVC7-. One of these signals is then jumpered to DVC05-. The more-significant portion is obtained by decoding EB03+, EB04+, and EB05+. The results of this are DVCE4- (device address 04x) and DVCE7- (device address 07x). Note that the decoded device-address is not enabled during IUAX+ or IUAF+. This prevents the DMA or interrupt address from being interpreted as an instruction. DVCDS- is gated with DVCE7- to form the DCM device address. DVC4- is gated with DVCE4- to form device-address 044 for common interrupt enable/disable instructions.

The programmed I/O data-transfer flip-flops are clocked by DVCFR+ (device address and FRYX+). If EB13+ or

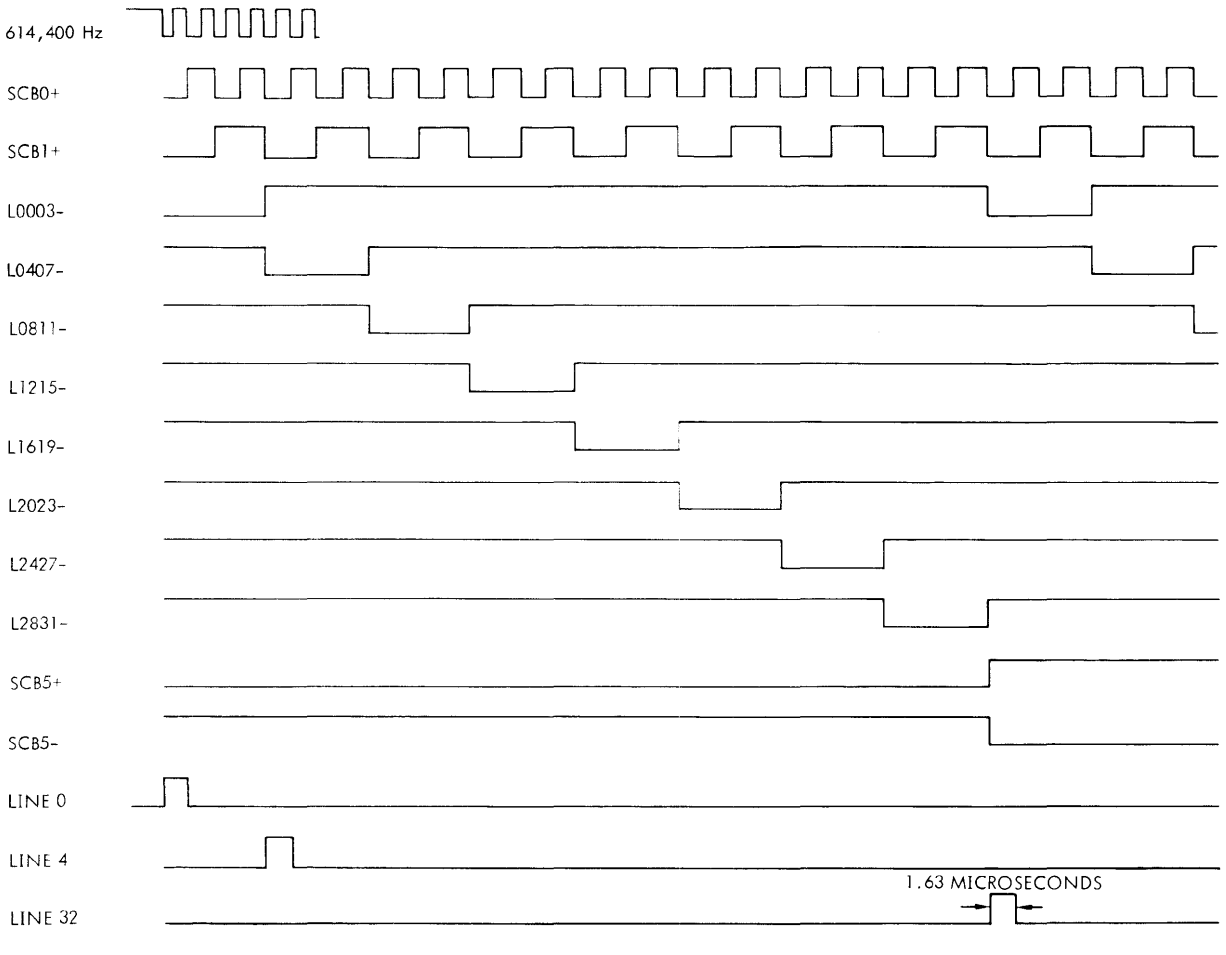
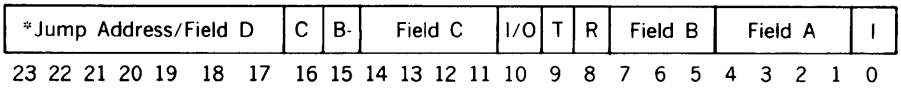


Figure 2-8. MU Scan-Counter Timing

Figure 2-9. DCM Control Memory Word Format



I = Idle bit: 0 = Not idle; 1 = Idle

R = Routine: 0 = Output request routine; 1 = Input request routine (true for entire routine)

T = Trap: 0 = No trap; 1 = Trap (enables field-B decoder)

I/O = Input/Output trap: 1 = Input trap; 0 = Output trap (valid for all trap instructions)

B = Enable B for status-change interrupt

C = Free-running address clock (set to zero when Field D is used)

* If Field C is all zeros, this field is used to control the ROM address counter clock (Field D).

Field A	Description
0 0 0 0	
0 0 0 1	Stop scanner
0 0 1 0	
0 0 1 1	Start strobe
0 1 0 0	Enable writing
0 1 0 1	Disable writing
0 1 1 0	Increment BA, decrement BC
0 1 1 1	
1 0 0 0	Input byte-count-zero interrupt
1 0 0 1	Output byte-count-zero interrupt
1 0 1 0	Line-error interrupt
1 0 1 1	Status-change interrupt
1 1 0 0	Control-character-detected interrupt
1 1 0 1	Control interrupt
1 1 1 0	
1 1 1 1	Start interrupt

Field C	Description
0 0 0 0	
0 0 0 1	Jump
0 0 1 0	Jump if byte count zero
0 1 0 0	Jump if control character detected
1 0 0 0	Jump if byte flag set

Field B	DMA Transfer
0 0 0	Fetch/store byte count
0 0 1	Fetch/store buffer address
0 1 0	Fetch control character
0 1 1	Fetch key bits
1 0 0	Fetch/store data
1 0 1	Fetch first byte (input)
1 1 0	Fetch line-control byte
1 1 1	Start trap

Field D	Clock Address Counter If:
0 0 0 0 0 0 0	
0 0 0 0 0 0 1	DTO set
0 0 0 0 0 1 0	DTO reset
0 0 0 0 1 0 0	DTI set
0 0 0 1 0 0 0	DTI reset
0 0 1 0 0 0 0	Trap/interrupt complete
0 1 0 0 0 0 0	No strobe (strobe complete)

mode gates the switches TS0 through TS6 or pins 26 through 32 of J1 to the counter. The test mode also enables CACL- and causes CACCL+ to run free. The test mode enables the counter to be forced to any control-memory address using the switches or the J1 inputs (Note: all the switches must be opened to use the J1 inputs).

2.2.8 Control-Character Checking Logic (MU Board 1)

This block contains data-comparison logic. The 16-bit register/counter is loaded via DMA with a specific line's two control characters. The two control characters are then compared to the data character in the interface buffer. If the buffered character is one of the control characters, a control-character interrupt is generated.

2.2.9 Clock and Bit-Rate Generator (MU Board 1)

This block contains a crystal controlled 9.8304 MHz clock, a standard bit-rate generator and two variable bit-rate generators. The standard bit-rate generator provides the following rates:

16 x 9600 = 153,600 Hz

16 x 4800 = 76,800 Hz

16 x 2400 = 38,400 Hz

16 x 1200 = 19,200 Hz

16 x 600 = 9,600 Hz

16 x 300 = 4,800 Hz

16 x 150 = 2,400 Hz

16 x 75 = 1,200 Hz

Any of these rates can be jumpered (section 2.1.3) to any of six buffer gates, which in turn distribute the bit-rates to the LADs. The variable bit-rate generators provide the capability of dividing 9.8304, 4.9152, 2.4576, 1.2288, 0.6144, or 0.3072 MHz by an integer from 1 to 256 to give a rate (150 kHz maximum) that can be jumpered to any of the six buffer gates.

The crystal-controlled 9.8304 MHz oscillator produces a square wave (CLKI+), which is immediately divided down to produce CLKB+, the DCM main clock. It is divided down by a synchronous counter to produce CLKC+, CLKD+, and CLKE+ (figure 2-11).

The standard bit rates are generated by simply continuing to count down CLKE+.

The odd-bit-rate counters consist of modulo-four synchronous counters. Counter 1 contains three modules and counter 2 contains two. The counters divide down the input frequency and count until they overflow. Upon overflow, they are loaded with the selected count and continue

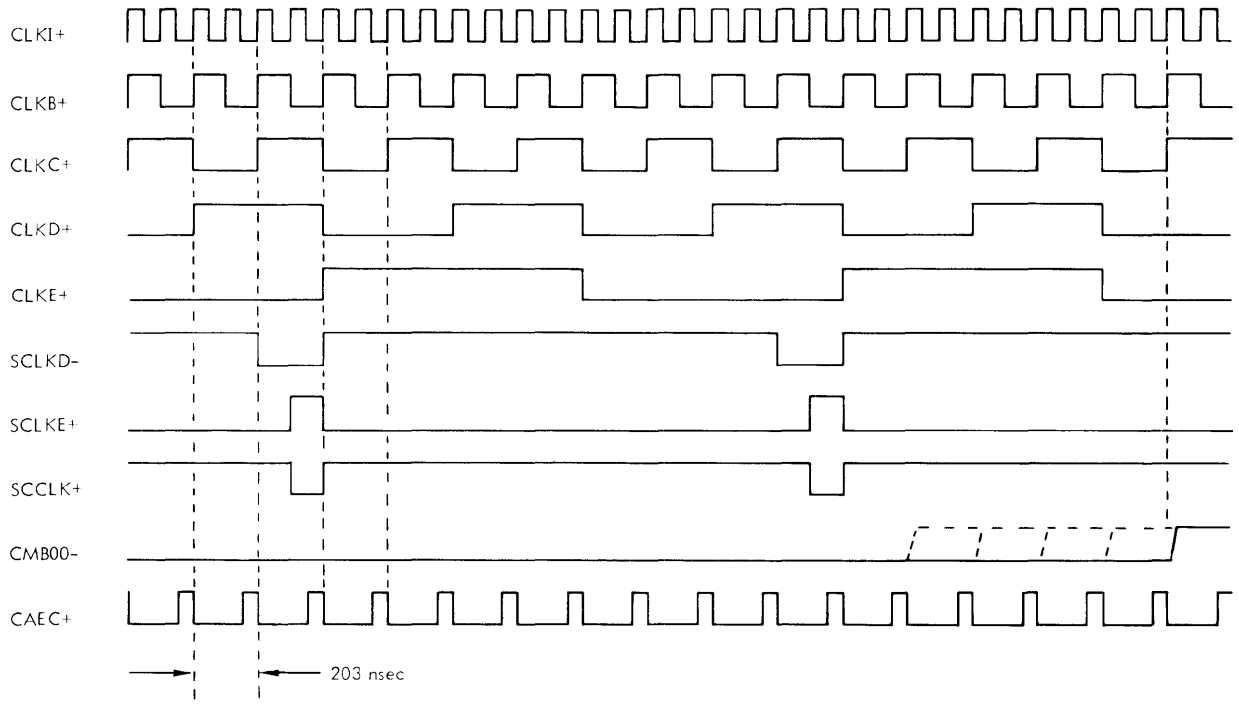


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Figure 2-11. MU Clock Timing Diagram

the SMB bit is set in memory, the DCM hardware forces the most significant bit to one on all input data. If it is not set, the data are stored as they come from the line. The SMB + flip-flop is held reset unless CMB08 + is true. CMB08 + is true only during an input sequence.

The DMA 16-bit register/counter is a 16-bit ripple counter with parallel-loading capability. It is parallel-loaded during a DMA cycle. It holds the input or output buffer address during an input or output sequence, and also holds the control characters during the control-character check phase of an input sequence. During the control-character check, the output of the counter is compared with the multiplexor bus bits and the signal CCM– goes true if there is a match. The counter also contains logic for incrementing its contents. If the byte flag flip-flop is reset (BF– true), the counter is incremented by CLKCS + . This increments the buffer address before it is transferred back to processor memory if the second byte has been input or output.

An interrupt is initiated by FA17– which set flip-flop INTR + . INTR + interrupt request) is then delayed by CLKB + to allow the interrupt address to settle (INTDL–). Once INTDL– is set, the interrupt flip-flop (INT +) is set on the next IUCX– clock if the interrupts are enabled (EINT–). INT + makes an interrupt request if the DCM has priority (PRMX +), and transfers the interrupt address onto the E-bus (iNTA + and INTB +) when the interrupt is acknowledged (IUAX +). INTA + clears the interrupt request (INTR + and INTDL–), and the INT + flip-flop clears on the first IUCX– clock after the interrupt is complete.

2.3 MAINTENANCE

The following equipment is required to test the MU:

a. Varian 620-series or V73 computer with at least 8K of memory

b. An I/O expansion chassis for the DCM backplane(s)

c. An I/O expansion power supply

d. One card extender (44 D 0015-000 or 44 D 0540-000)

e. Tektronix Type 547 or equivalent oscilloscope

f. At least one asynchronous RS232 interface line adaptor (01 A 1470-000) with two test connectors (burndy edge connectors 57 A 0036-000) wired as follows:

Line 0

1.	Pin 29 to pin 35	Data-terminal-ready to ring-indicator
	Pin 35 to pin 33	Ring-indicator to dataset-ready
	Pin 29 to pin 25	Data-terminal-ready to carrier-on
2.	Pin 27 to pin 37	Request-to-send to clear-to-send
3.	Pin 31 to pin 23	Transmit-data to receive-data
4.	Pin 21 to pin 18	Control-out to control-in

Line 1

5.	Pin 1 to pin 13	Data-terminal-ready to ring-indicator
	Pin 13 to pin 11	Ring-indicator to dataset-ready
	Pin 1 to pin 7	Data-terminal-ready to carrier-on
6.	Pin 3 to pin 19	Request-to-send to clear-to-send
7.	Pin 5 to pin 9	Transmit-data to receive-data
8.	Pin 6 to pin 8	Control-out to control-in

The following additional jumpers can be added so the test connector can also be used on a synchronous RS232 interface LAD.

Pin 38 to pin 39
Pin 39 to pin 41
Pin 38 to pin 17
Pin 17 to pin 15

These jumpers tie the test clock to the receive/transmit clock inputs.

When testing the MU, the asynchronous RS232 interface LAD lines should be set up for eight-bit data, two stop bits, no parity.

g. Software tapes

MAINTAIN II Test Executive	92 U 0107-001
DCM Test Program	92 U 0106-009C

The following system configuration features must be checked before testing:

a. Verify that the following features are jumpered according to special system specifications, if any, or to the standard configuration:

1. Odd-bit-rate counters 1 and 2
2. The source for the six bit-rate (line-speed) signals
3. Scan length
4. Priority mode
5. Device address
6. E-bus priority chain wiring
7. Base interrupt address
8. Base control table address (LCB)
9. High-speed or normal DMA selection

b. If the system term shoe is located in the DCM, verify that + 5V dc is wired to the term shoe slot on pins 118 and 121.

Scan Length	Mnemonic	Test Point	Frequency
4,8,16,32,64	SCB0–	P1 pin 97	307,200 Hz
4,8,16,32,64	SCB1–	P1 pin 96	153,600 Hz
4,8,16,32	SCB5–	P1 pin 99	High level
64	SCB5–	P1 pin 99	9,600 Hz
4,8,16,32	SCB5+	P1 pin 100	Low level
64	SCB5+	P1 pin 100	9,600 Hz
4	L0003–	P1 pin 23	153,600 Hz
8	L0003–	P1 pin 23	76,800 Hz
16	L0003–	P1 pin 23	38,400 Hz
32,64	L0003–	P1 pin 23	19,200 Hz
8	L0407–	P1 pin 22	76,800 Hz
16	L0407–	P1 pin 22	38,400 Hz
32,64	L0407–	P1 pin 22	19,200 Hz
16	L0811–	P1 pin 21	38,400 Hz
32,64	L0811–	P1 pin 21	19,200 Hz
16	L1215–	P1 pin 20	38,400 Hz
32,64	L1215–	P1 pin 20	19,200 Hz
32,64	L1619–	P1 pin 27	19,200 Hz
32,64	L2023–	P1 pin 26	19,200 Hz
32,64	L2427–	P1 pin 25	19,200 Hz
32,64	L2831–	P1 pin 24	19,200 Hz

Control-Memory Address Switches and Indicators: Ground J1 pin 25 or jumper pin X6 to X5 on MU board 1 and verify that the control memory address indicators (DS1 through DS7 on MU Board 1) can be turned on with the switches at location D10. When the side of the switch-rocker with the black dot is depressed, the switch is activated.

Control-Memory Output: Verify that the control-memory test-points at J1 (pins 1 through 24) are all high (except pins 24 and 8) when the DCM is in idle (control-memory address 000).

2.3.3 Suggested Methods

DCM test program - Test 0: Test 0 of the test program is a transmit-only test and is helpful in troubleshooting.

Sample program: The following program will be helpful in troubleshooting problems that cannot be found with the DCM test program. The program starts a transfer and at the end of the transfer (input or output byte-count zero), it initializes the DCM and begins again. If sense switch 3 is set, the program jumps back to the test executive at the completion of the transfer. Note that the output byte-count-zero interrupt occurs before the last two bytes have actually been transmitted, so these bytes are lost.

Interrupt Traps

000060	002000	JMPM
000061	000260	
000062	002000	JMPM
000063	000260	
000064	001000	JMP
000065	000270	
000066	001000	JMP
000067	000271	
000070	001000	JMP
000071	000272	
000072	002000	JMPM
000073	000240	

Address (Octal)	Code (Octal)	Instruction	Remarks

Interrupt Halts

000270	000004	Line error interrupt
000271	000006	Status change interrupt
000272	000001	Control-character-detected interrupt

* Change these instructions to reflect the correct device address if a nonstandard address is used.

LCB Address

The LCB addresses for the line under test are entered here.

Address (Octal)	Code (Octal)	Instruction	Remarks
000500	017000		Input block-length address
000501	017001		Input buffer-address address
000502	017004		Output block-length address
000503	017005		Output buffer-address address
000504	017006		Control-word address

Line Control Block (Line zero shown - base address 017000)

017000	107770	Input block-length
017001	000600	Input buffer-address
017002	177777	Control characters
017003	000000	Spare
017004	107770	Output block-length
017005	000650	Output buffer-address
017006	005500	Line control-word (includes line address)
017007	000000	Spare

Output Buffer

000650	125252
000651	125252
000652	125252
000653	125252

Table 2-12. Output Sequence

ADDRESS							REMARKS	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6	5	4	3	2	1	0		Jump Address/Field D							C	B	Field C				I/O	T	R	Field B			Field A				1
0	0	0	0	0	0	1	Stop scan; start trap; jump	0	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	1	1	0	0	0	1	0
0	0	0	1	0	0	0	Fetch byte count, enable write, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
0	0	0	1	0	0	1	Test byte count, start trap	0	0	1	0	1	1	0	1	0	0	0	1	0	0	1	0	1	1	1	0	0	0	0	0
0	0	0	1	0	1	0	Fetch buffer address, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
0	0	0	1	0	1	1	Start trap	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0
0	0	0	1	1	0	0	Fetch data, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
0	0	0	1	1	0	1	Start strobe	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	1	1	1	0	Start trap, test byte flag, inc.	0	0	1	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	1	0	1	1	0	0
0	0	0	1	1	1	1	Store buffer address, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	Start trap	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0
0	0	1	0	0	0	1	Store byte count, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	Test byte count zero	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	Wait for strobe complete	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	Back to zero, disable write	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0
0	0	1	0	1	1	0	Fetch line control byte, wait for trap complete	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0
0	0	1	0	1	1	1	Start strobe, jump	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0
0	0	1	1	0	0	1	Gen. int. (output byte-count zero)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
0	0	1	1	0	1	0	Wait for DTO set	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
0	0	1	1	0	1	1	Wait for DTO reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	Jump	0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0

Table 2-14. Status Input Sequence

ADDRESS							REMARKS	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6	5	4	3	2	1	0		Jump Address/Field D							C	B	Field C				I/O	T	R	Field B			Field A				1
0	0	0	0	0	1	1	Stop scan; jump; enable B	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	Generate interrupt enable	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
1	0	0	0	0	0	1	Status change interrupt, wait for DTO set	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
1	0	0	0	0	1	0	Strobe	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	0	0	1	1	Wait for strobe complete	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	Wait for DTO reset; set write	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	1	0	1	Strobe	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	0	1	1	0	Wait for strobe complete	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	Jump to zero; disable write	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0

Table 2-15. Processor Write Sequence

ADDRESS							REMARKS	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6	5	4	3	2	1	0		Jump Address/Field D							C	-	Field C				I/O	T	R	Field B			Field A				1
0	0	0	0	1	0	0	Stop scan; jump	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	Generate interrupt	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
1	0	0	1	0	0	1	Control int.; wait for DTO set	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
1	0	0	1	0	1	0	Wait for DTO reset, enable write	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	1	0	1	1	Start strobe	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
1	0	0	1	1	0	0	Wait for strobe complete	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	Disable write, jump to zero	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0

Table 2-18. Control Memory Contents

Address	49A0194-007	49A0194-006	49A0194-005
0000000	00000001	00000000	00000001
0000001	00010001	00001010	11100010
0000010	01000001	00001011	11100010
0000011	10000001	10001000	00000010
0000100	10010001	00001000	00000010
0000101	10100001	00001000	00000000
0000110	10101111	00001000	00000010
0000111	00000000	00000000	00000000
0001000	00100000	00000010	00001000
0001001	00101101	00010010	11100000
0001010	00100000	00000010	00100000
0001011	00000001	00000010	11100000
0001100	00100000	00000010	10000000
0001101	00000001	00000000	00000110
0001110	00100011	01000110	11101100
0001111	00100000	00000110	00100000
0010000	00000001	00000110	11100000
0010001	00100000	00000110	00000000
0010010	00110011	00010000	00000000
0010011	01000000	00000000	00000000
0010100	00000001	00001000	00001010
0010101	00000000	00000000	00000000
0010110	00100000	00000010	11000000
0010111	00100111	00001000	00000110
0011000	00000000	00000000	00000000
0011001	00000001	00000000	00011110
0011010	00000010	00000000	00010010
0011011	00000100	00000000	00000000
0011100	00100111	00001000	00000110
0011101	00000000	00000000	00000000
0011110	00000000	00000000	00000000
0011111	00000000	00000000	00000000
	↑ MSB		↑ LSB

Table 2-18. Control Memory Contents *(continued)*

Address	49A0194-010	49A0194-009	49A0194-008
0100000	00100000	00000011	00000000
0100001	01111011	00010001	00000110
0100010	00000001	00000011	11100000
0100011	00100000	00000011	00100000
0100100	01001111	01000011	11100000
0100101	00100000	00000011	10100000
0100110	00000001	00000111	11100000
0100111	00100000	00000111	10000000
0101000	01010111	01000111	11101100
0101001	00100000	00000111	00100000
0101010	00000001	00000111	11100000
0101011	00100000	00000111	00000000
0101100	00000001	00000011	11100000
0101101	00100000	00000011	01000000
0101110	01100101	00100001	00000000
0101111	01110011	00010001	00000000
0110000	00000001	00001000	00000000
0110001	00000000	00000000	00000000
0110010	00000001	00000001	00011110
0110011	00000010	00000001	00011000
0110100	00000100	00000001	00001000
0110101	00000001	00000001	00000110
0110110	01000000	00000001	00000000
0110111	01011111	00001001	00001010
0111000	00000000	00000000	00000000
0111001	00000001	00000001	00011110
0111010	00000010	00000001	00010000
0111011	00000100	00000001	00001000
0111100	00000001	00000000	00000110
0111101	01000000	00000000	00000000
0111110	00000001	00001000	00001010
0111111	00000000	00000000	00000000
	↑ MSB		↑ LSB

Table 2-19. DCM Instructions

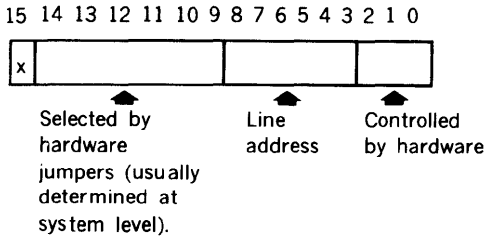
Octal	Mnemonic	Definition	Decription
100070	EXC 070	Initialize	Programmed system reset that clears the multiplexor and all associated LADs
100170	EXC 0170	Clear control logic	Aborts current sequence and returns multiplexor to scanning mode, but does not disable interrupts
100270	EXC 0270	Enable DCM interrupts	Enables the six DCM interrupts
100470	EXC 0470	Disable DCM interrupts	Disables the six DCM interrupts
100570	EXC 0570	Request control (write)	Permits computer to request use of multiplexor bus for LAD setup; the multiplexor generates a control interrupt upon completion of current operation
100670	EXC 0670	Request control (read)	Permits computer to request use of multiplexor bus for reading LAD status; the multiplexor generates a control interrupt upon completion of current operation
100244	EXC 0244	Enable interrupts (common)	DCM also responds to this general system interrupt-enabling instruction
100444	EXC 0444	Disable interrupts (common)	DCM also responds to this general system interrupt-disabling instruction
102070	IME 070	Input data from DCM to memory	Transfers a 16-bit character from the DCM, where the six least-significant bits come from the scan counter and the remainder from the interface buffer
102170	INA 070	Input data from DCM to A register	
102270	INB 070	Input data from DCM to B register	
102570	CIA 070	Clear A register and input data from DCM	Clears destination register, then transfers a 16-bit character from the DCM, where the six least-significant bits come from the scan counter and the remainder from the interface buffer
102670	CIB 070	Clear B register and input data from DCM	
103170	OAR 070	Output data from A register to DCM	Transfers a 16-bit character to the DCM, where the six least-significant bits go to the scan counter and the remainder to the interface buffer
103270	OBR 070	Output data from B register to DCM	
103370	OME 070	Output data from memory to DCM	

2.4.2.6 Control

This interrupt is explained in section 2.4.4.4 on DCM programming sequences.

2.4.3 DCM DMA Control Table

The DCM works from line control tables (figure 2-13) stored in computer memory for all DMA operations. Each line control table uses eight memory locations. Thus, for a maximum 64-line system, 512 memory locations are allocated for the DCM.



The byte-transfer flag in the control table is hardware-set and determines which byte is to be transferred. The initial

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
077000	f	s	x	x	ONE'S COMPLEMENT OF INPUT BLOCK-LENGTH IN BYTES											
077001	x	INPUT BUFFER ADDRESS														
077002	CONTROL CHARACTER 2								CONTROL CHARACTER 1							
077003	SPARE															
077004	f	x	x	x	ONE'S COMPLEMENT OF OUTPUT BLOCK-LENGTH IN BYTES											
077005	x	OUTPUT BUFFER ADDRESS														
077006	LINE-CONTROL BYTE								a	b	x	x	x	x	x	x
077007	SPARE															

x = UNUSED
f = BYTE-TRANSFER FLAG
0 FOR LOWER EIGHT BITS
1 FOR UPPER EIGHT BITS
ab = CODE FOR LINE-CONTROL BYTE
s = FORCES MSB BIT (8TH BIT) OF INPUT BYTE TO ONE

NOTE: ADDRESSES SHOWN ARE FOR LINE ZERO WITH THE SIX MOST-SIGNIFICANT BITS ALL STRAPPED ON

DATA BUFFER FORMAT

15 8	7 0
FIRST CHARACTER	SECOND CHARACTER
THIRD CHARACTER	FOURTH CHARACTER

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Figure 2-13. Line Control Table

byte flag is reset. If the flag is not set, it is now set and the characters stored in memory with the new character in the less-significant byte position. After the character is stored, the byte count is decremented and restored in memory.

If the byte flag was set, the input buffer address word is incremented and the new address stored in memory. After the input character is stored in the input buffer and all the housekeeping completed, the two control characters are input to the multiplexor and compared to the input character. If there is a match, a control-character-detected interrupt is generated. Upon completion of the control-character check, the multiplexor checks to see if the byte count went to zero during this input sequence. If the byte count is zero, an input byte-count-zero interrupt is generated. The byte-count check completes the input sequence, and scanning is resumed.

If there is an input request from a line whose byte count is already zero, the multiplexor clears the request and continues scanning (unless a line error is present, in which case the line error is reported).

Note: The DCM clears the less-significant byte whenever it loads data in the more-significant byte of a buffer word.

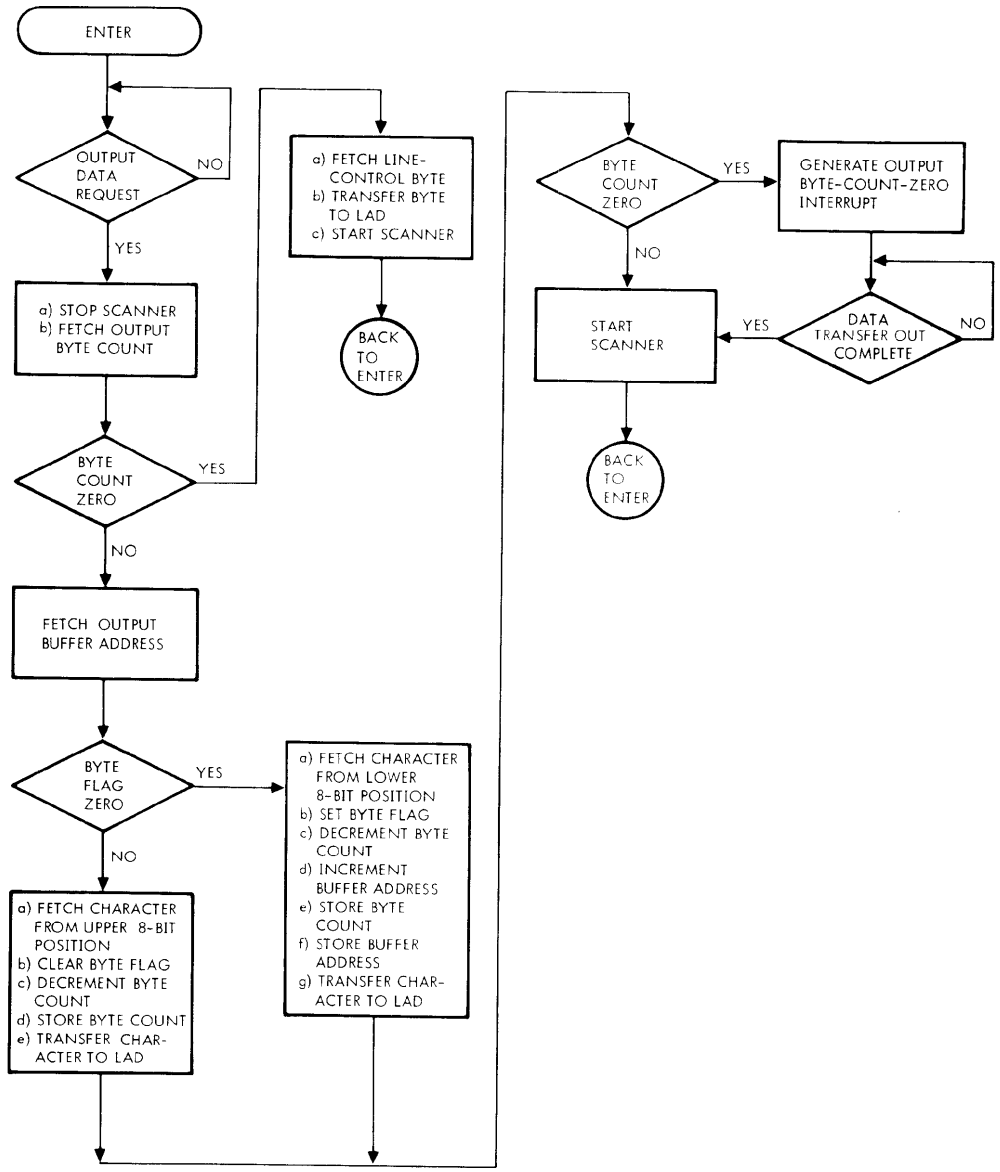

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Figure 2-15. DCM Output Sequence

waits for the data-transfer-out and then loads the indicated line and resumes scanning. For reading, the multiplexor waits for the data-transfer-out that identifies the line and the data to be transferred, then fetches the appropriate data and waits for the data-transfer-in. At the end of the sequence, scanning resumes.

Since the multiplexor stops scanning during a control sequence, control operations should be as fast as possible to prevent line overruns and consequent data loss.

Sample control sequences are given in this manual in the programming subsections of each LAD section.

2.5 MNEMONICS

MU Board One

Mnemonic	Definition
A–	Decoded along with B– to indicate the type of information being transferred to the LAD.
AC +	Source for A– from the interface buffer
AC10 + thru AC16 +	Parallel inputs to the control memory address counter
AD +	A input to the interface buffer (EB07 +)
B–	See A–
BC +	Source of B– from the interface buffer
BD +	B input to the interface buffer (EB06 +)
BFA +	Byte flag (buffered) from MU board 2
BR0– thru BR5–	Bit-rate sources for the LADs: Actual frequency determined by jumpers
CACCL +	Clock for the control memory address counter
CAC10 + thru CAC12 +	Three least-significant parallel inputs to the control memory address counter (before normal mode/test mode selection logic)
CACL–	Parallel-load signal for the control memory address counter
CAE +	Control memory address counter clock enabler
CCLG–	Clear-control-logic signal from MU board 2
CCM +	Control-character-match signal from MU board 2
CLK–	Clock for the LADs (nominally 614,400 Hz) (LADs place requests on line on the positive going edge of this clock)
CLKB + CLKBF +	4.9152 MHz clock (square wave)
CLKC +	2.4576 MHz clock (square wave)
CLKD +	1.2288 MHz clock (square wave)
CLKE +	614,400 Hz clock (square wave)
CLKF +	307,200 Hz clock (square wave)
CLKI +	Fundamental clock frequency 9.8304 MHz
CMA00 + thru CMA06 +	Outputs of the control memory address counter
CMB00 + thru CMB23 +	Outputs of the control memory
CME00–	Enable control memory addresses 000 to 037
CME32–	Enable control memory addresses 040 to 077
CME64	Enable control memory addresses 0100 to 0137
CPURA +	CPU read control request from MU board 2
CPURS +	CPUR4 + synchronized with CLKB +
CPUWA +	CPU write control request from MU board 2
CPUWS +	CPUWA + synchronized with CLKB +
CZ +	Byte count zero signal from MU board 2
DTIA +	Data transfer in signal from MU board 2
DTIS +	DTIA + synchronized with CLKB +
DTOA +	Data transfer out signal from MU board 2
DTOS +	DTOA + synchronized with CLKB +

Mnemonic	Definition
STRBE	Strobe to LADs
SYRTA–	System-reset from MU board 2
TEST–	Test (when grounded, allows control memory to be addressed by the test switches +S0 through S6 or via J1)
TOI	Trap or interrupt from MU board 2
TOIC +	Trap or interrupt complete
TST +	Test (allows a free running clock to the control memory address counter)
WRITE–	Indicates direction of data transfer on the multiplexor bus

MU Board Two

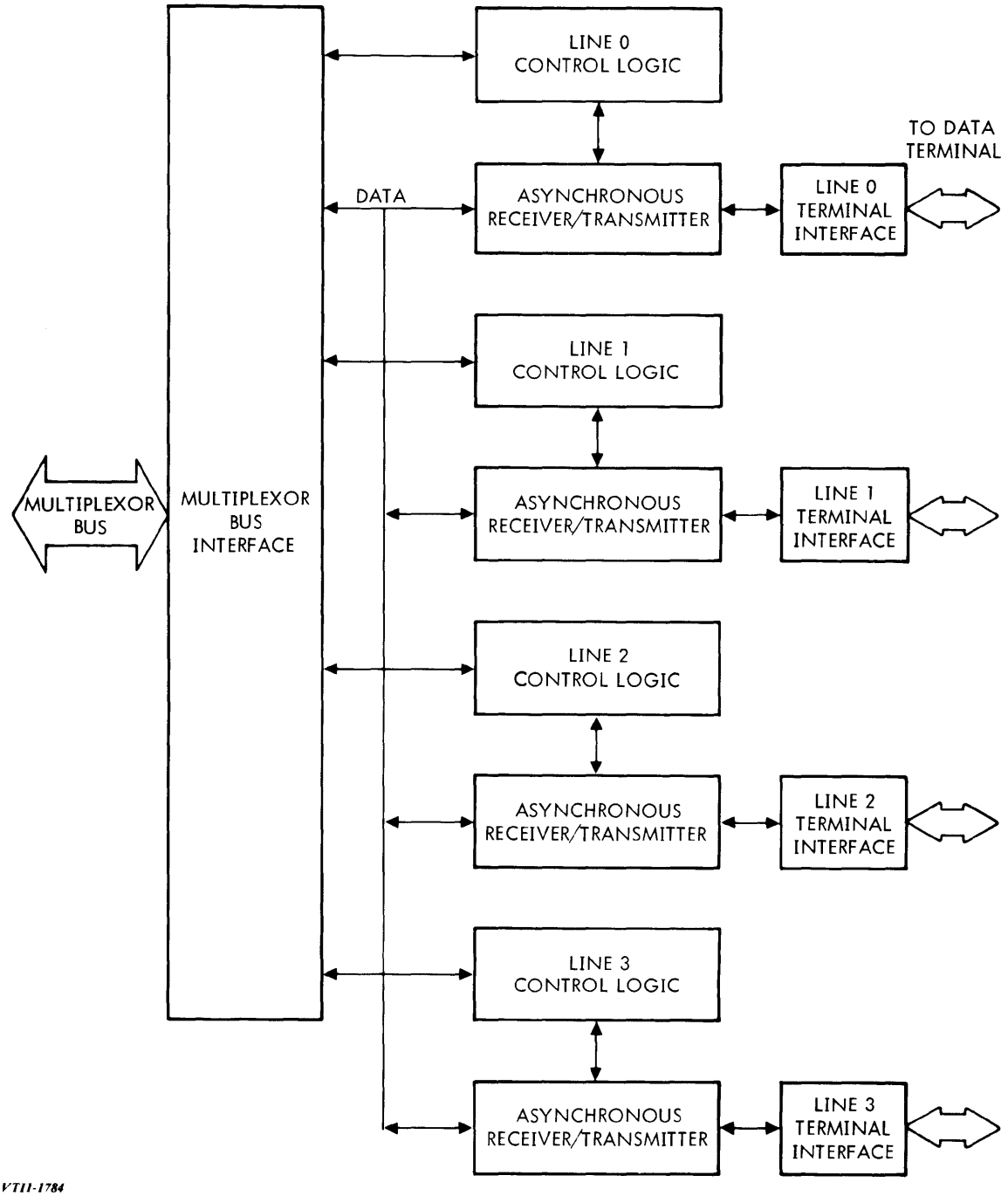
Mnemonic	Definition
AI–	Decoded with BI– to determine type of line error (from LADs)
BC00 + thru BC11 +	Outputs of the byte-count register/counter
BF +	Byte flag
BFA +	Byte flag buffered and sent to MU board 1
BI–	See AI–
CCLG–	Clear control logic
CCM–	Match control-character (sent to MU board 1)
CLKB +	4.9152-MHz square-wave from MU board 1
CLKCS +	Clock to decrement the byte count and increment the buffer address
CLKE +	614,400-Hz square-wave from MU board 1
CMB00 thru CMB23	Control memory output from MU board 1
CPURA +	CPU read control request to MU board 1
CPUWA +	CPU write control request to MU board 1

Mnemonic	Definition
CTA09 + thru CTA15 +	Control table (LCB) hardware selectable address bits
CZ +	Byte-count-zero indication to MU board 1
DRYF-I	High-speed DMA data-ready signal
DRYX-I	E-bus data-ready signal
DR00– thru DR15–	Outputs of the DMA 16-bit register/counter
DTI +	Data transfer in
DTIA +	Buffered DTI to MU board 1
DTO +	Data transfer out
DTOA +	Buffered DTO to MU board 1
DVCD +	Device code (address)
DVCFR +	Device address gated with FRYX +
DVC44 +	Device address 044 for common interrupt enable/disable
D44FR–	Device address 044 gated with FRYX +
EAB0 +	Enable AI and BI onto E-bus
EBC + thru EBCA +	Enable output of byte-count register/counter onto E-bus
EB00-I thru EB15-I	16-bit bidirectional E-bus signals
ECTA + thru ECTAA +	Enable control-table address onto E-bus
EDR thru EDRA +	Enable output of 16-bit DMA register/counter onto E-bus
EDRI–	Enable key bits during the address portion of a DMA cycle for data
EINT–	Enable interrupts
ELMBA	Enable multiplexor-bus signals onto less-significant portion of E-bus and interface buffer signals (IBx + E) onto the more-significant portion

Mnemonic	Definition
SCB0– thru SCB5–	Scan-counter outputs from MU board 1
STRAP +	Normal-DMA trap (data portion)
STRPD +	Normal-DMA trap (address portion)
SYRT-I	E-bus system-reset
SYRTA–	DCM system-reset
TOI–	Trap or interrupt complete (to MU board 1)
TPIF-I	High-speed DMA trap-in request
TPIX-I	Normal-I/O DMA trap-in request
TPOF-I	High-speed DMA trap-out request
TPOX-I	Normal-I/O DMA trap-out request
X0– thru X6–	Function decoded (EB06, EB07, EB08)

SECTION 3
DIRECT-CONNECTION LINE-ADAPTER

This LAD (figure 3-1) provides three direct-connection interfaces for the DCM. It can handle four terminals and its interface circuits can be RS232, current-loop, or relay model (table 3-2).



VTII-1784

Figure 3-1. Direct Connection LAD Simplified Block Diagram

Table 3-2. Direct-Connection LAD Line-Interface Comparison

Interface	RS232	Current-Loop	Relay
Bit Rate	45 to 9600 bps, depending on cable length (table 3-3)	45 to 9600 bps, depending on cable length (table 3-3)	45 to 300 bps, typically 75 or 110 bps (note that relays do not operate reliably above 300 bps)
Power requirements	+5V dc at 1A +12V dc at 100mA -12V dc at 100mA	+5V dc at 1A -12V dc at 50mA (exclusive of user-supplied loop-current battery power)	+5V dc at 1A -12V dc at 50mA (exclusive of user-supplied loop-current battery power)
Cable length	20 feet (6 meters) standard, 50 feet (15 meters) maximum	20 feet (6 meters) standard, more than one mile (1.6 km) maximum, depending on bit rate (table 3-3), e.g., 1,000 feet (300 meters) at 9600 bps	20 feet (6 meters) standard, more than one mile (1.6 km) maximum, depending on bit rate (table 3-3), e.g., 10,000 feet (3,000 meters) at 300 bps

Table 3-3. Cable Length vs. BPS Rate

Cable Length	Maximum Rate in BPS
Up to 1,000 feet (300 meters)	10,000
1,000 to 2,000 feet (300 to 600 meters)	4,800
2,000 to 3,500 feet (600 meters to 1 km.)	1,800
3,500 to 5,000 feet (1 to 1.5 km.)	900
5,000 to 10,000 feet (1.5 to 3 km.)	300

3.1 INSTALLATION

The LAD has been inspected and packed to ensure its arrival in good working order. To prevent damage, take reasonable care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If any is found:

a. Notify the transportation company

b. Notify Varian Data Machines

c. Save all packing material

3.1.1 Physical Description

The direct-connection LAD is on one printed-circuit board (figure 3-2) mounted in a specially-wired expansion chassis (figures 1-2 and 1-3).

3.1.2 Interfaces

The direct-connection LAD interfaces with the MU over the multiplexor bus (figures 1-1 and 2-1), and with the terminals directly over the line interfaces (section 3.1.2.2).

3.1.2.1 Multiplexor Bus

The 38-line multiplexor bus connects the LAD with the MU. It is described in section 2.1.2.2.

3.1.2.2 Line Interface

There is a line interface for each version of the direct-connection LAD:

- RS232
- Current-loop
- Relay

RS232 Interface: This interface drives peripherals with compatible interfaces. It also provides a DTL output that has an open-collector interface capable of sinking 70mA at

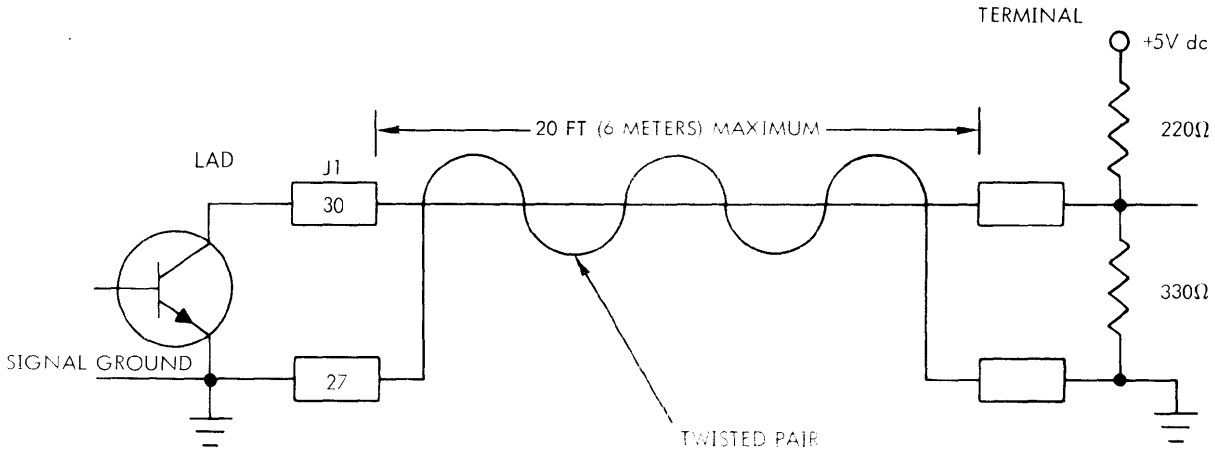


Figure 3-3. DTL Interface

Table 3-5. Current-Loop Interface Specifications

Driver Specifications

Collector emitter voltage	150V dc maximum
Collector current - continuous	500 mA maximum
Total dissipation at 25 degrees C	1 W maximum

Receiver Specification

Input forward voltage drop	1.5V dc maximum
Input forward continuous current	60 mA maximum

Isolation

Common-mode protection	500V dc
Common-mode resistance	10 megohms

Logic 0 = No loop current

Logic 1 = Loop current (20 mA minimum)

Table 3-6. Current-Loop Interface Pin Connections

Line	Signal	Pin	Definition
0	OUT0-	J1-029	Negative terminal of the output driver
0	OUT0+	J1-040	Positive terminal of the output driver
0	IN0-	J1-037	Negative terminal of the input receiver
0	IN0+	J1-034	Positive terminal of the input receiver
0	GND	J1-027	Ground
0	CS10	J1-039	Negative current source for testing only
0	CS20	J1-041	Negative current source for testing only
1	OUT1-	J1-003	Negative terminal of the output driver
1	OUT1+	J1-012	Positive terminal of the output driver
1	IN1-	J1-007	Negative terminal of the input receiver
1	IN1+	J1-006	Positive terminal of the input receiver

(continued)

Table 3-7. Relay Interface Specifications

Input	
Relay input-coil rating	12.5V dc maximum
Relay input-coil resistance	1250 ohms
Output	
Reed relay contact closure	Form A, form B, or form C
Maximum contact voltage	120V dc
Isolation	
Common-mode resistance	10 megohms at 400V dc

Table 3-8. Relay Interface Pin Connections

Line	Signal	Pin	Definition
0	NC0	J1-025	Form A contacts (closed for a logical 1)
0	NCS0	J1-038	Form A contacts (closed for a logical 1)
0	NOS0	J1-036	Form B contacts (open for a logical 1)
0	NO0	J1-029	Form B contacts (open for a logical 1)
0	RLY0+	J1-031	Positive receiver input
0	RLY0–	J1-037	Negative receiver input
1	NC1	J1-001	Form A contacts (closed for a logical 1)
1	NCS1	J1-010	Form A contacts (closed for a logical 1)
1	NOS1	J1-008	Form B contacts (opened for a logical 1)
1	NO1	J1-003	Form B contacts (opened for a logical 1)
1	RLY1+	J1-005	Positive receiver input
1	RLY1–	J1-007	Negative receiver input
2	NC2	J2-025	Form A contacts (closed for a logical 1)
2	NCS2	J2-038	Form A contacts (closed for a logical 1)
2	NOS2	J2-036	Form B contacts (opened for a logical 1)
2	NO2	J2-029	Form B contacts (opened for a logical 1)
2	RLY2+	J2-031	Positive receiver input
2	RLY2–	J2-037	Negative receiver input
3	NC3	J2-001	Form A contacts (closed for a logical 1)
3	NCS3	J2-010	Form A contacts (closed for a logical 1)
3	NOS3	J2-008	Form B contacts (opened for a logical 1)
3	NO3	J2-003	Form B contacts (opened for a logical 1)
3	RLY3+	J2-005	Positive receiver input
3	RLY3–	J2-007	Negative receiver input

3.1.3 Options

Parity (odd, even, or none), character length (5, 6, 7, or 8 bits), and the number of stop bits (1 or 2) are set on a line-by-line basis using the data-format toggle switches (figure 3-2) as follows:

	Switch	1 PS	2 WLS1	3 WLS2	4 SBS	5 PI
Parity	Odd	On				On
	Even	Off				On
	None					Off
Length	5		On	On		
	6		Off	On		
	7		On	Off		
	8		Off	Off		
Stop bits	1				On	
	2				Off	

3.1.3.1 Line Bit-Rate Selection

Each line can be jumpered for one of the six bit-rates provided by the multiplexor bus. The frequencies of these bit-rates are determined by jumpers on the DCM backplane at the individual LAD locations. One clock per line is jumpered into the LAD, and these clocks operate at 16 times the actual desired line bit-rate. Table 3-9 shows the jumper points for the inputs to the LAD and the pin location of the six bit-rates provided by the multiplexor (BR0 through BR5). The frequencies are determined by jumpers on MU board 1. If no bit rates are specified, the speed is 1760 Hz (16 x 110).

Table 3-9. Line Bit-Rate Selection Multiplexor Bus Bit-Rate Locations

Standard Frequencies	Mnemonic	Pin Location at LAD Slot
153,600 Hz (16 x 9600)	BR0	101
38,400 Hz (16 x 2400)	BR1	102
19,200 Hz (16 x 1200)	BR2	103
4,800 Hz (16 x 300)	BR3	104
2,400 Hz (16 x 150)	BR4	105
1,760 Hz (16 x 110)	BR5	106

Line Adapter Clock Inputs (at Backplane)

Line	Input Pin
0	92
1	93
2	98
3	97

3.1.3.2 Solid-State Current-Loop Clock

If the LAD is the 44 D 0654 001 version, a clock (CLKB +) is wired in at the DCM backplane. This clock is buffered on the LAD and brought out on P1 pin 42 for the next LAD of this type. The clock is picked up at slot 10 of the DCM main backplane (MU board 1) pin 50 and wired to pin 44 of the first solid-state current-loop direct-connection LAD. If another LAD of this type is used, a wire is added from pin 42 of the first LAD to pin 44 of the next LAD.

3.2 THEORY OF OPERATION

This section explains the operation of the direct-connection LAD, with each subsection corresponding to a block (or set of blocks) on the simplified LAD block diagram (figure 3-1). Figure 3-6 is a detailed block diagram. Refer to logic diagram 91B0414 for understanding this theory.

3.2.1 Multiplexor Bus Interface

This logic provides a common interface for the four lines of the LAD to the multiplexor bus (section 2.1.2.2). This interface includes provision for jumpering a different speed for each line and assigns the LAD an address on the multiplexor bus.

Data/status selection: This LAD output to the multiplexor eight-bit bus has two sources: the eight-bit receiver-data bus (RD0 + through RD7 +) from the four asynchronous receiver/transmitter devices, and the two status outputs (SB0 + and SB1 +). Selection of these outputs is accomplished with a quad-two-line-to-one-line data-selector device. The selection term is EDTA−, and the data-selector devices are enabled by EOB−. These terms are formed with half of a dual two-line-to-four-line decoder, which is enabled by LAD enabler (LAE1−) when the multiplexor is reading (WRITE + false). EOB− is true if the data-selection terms A− and B− are both false, or if A− and B− is true. EDTA− is true only when A− and B− are both false. EDTA− true gates the receiver data bus out.

LAD enabling logic: The LAD address input (LADA−) and the LAD address-enabler input (LADE−) are ANDed to form the LAD enabling terms LAE1− , LAE2− , and LAE3− .

3.2.2 Service-Request Logic

The three service-request terms IDRSD + , ODRSD + , and SIRSD + are clocked into the service-request register on the positive transition of CLK− . The outputs of the register are gated to form a priority structure where the input data-request has the highest priority and the input-status request has the lowest. When an input data-request is made, a line error may be reported (LERR−). If a line error has occurred, the AI− and BI− identify the type of error.

Input data-request (IDRSD +): An input data-request is made if the data ready flag is true (DR +) and the line is in receiving mode, or if the line is in transmission mode and a framing error occurs.

Output data-request (ODRSD +): An output data-request is made if the line is in transmission mode, echo mode is not selected, output-buffer and output-register conditions are not being reported (U− and SB5 +), and the output buffer is empty (TBREA +).

Input-status request (SIRSD +): An input-status request is made under the following conditions:

a. The lines ICS + signal is true and a change of state in the control-line-in is detected.

b. The I + bit is set in the line-control byte and the transmission buffer and transmission register are both empty.

3.2.3 Control Logic

The control logic for each line (zero through three) is identical. It provides steering logic for data/control transfer to and from the line, storage flip-flops for the control and status bytes, break-transmitting logic, and service-request generation logic (i.e., input or output data requests, etc.).

The control bits are stored in quad-D flip-flop modules with tristate outputs. The tristate outputs allow the corresponding bits of each line to be tied together and only one register at a time is enabled as the lines are sequentially scanned. Each control bit function is described below.

Transmission: T + indicates that the selected line is in transmission mode. T + is gated with the LAD enabler to produce SMT + , which enables output and input data requests in the event of a framing error.

Receive: R + indicates that the line is in receiving mode. R + enables input data requests as data are received, and enables the data strobe to the asynchronous receiver/transmitter device when a line is in echo mode.

Echo: E + inhibits output data requests and causes all received data to be transmitted automatically.

Break: TB + enables the transmit-break logic.

Control Line: ICS + controls the control-line-in change-of-state detection logic.

Interrupt on underflow: The MT + output of the control registers are used to enable a status change request when the lines' output buffer and output register are both empty.

3.2.4 Strobe Distribution Logic

A strobe pulse is sent from the multiplexor as a load pulse or a reset pulse, depending on the sequence taking place.

Reset data available (RDA +): This signal clears the data-available flag (DR +) of the four asynchronous transmitter/receiver devices. RDA + is distributed to the devices via one-half of a dual demultiplexor device. The device provides four outputs, one for each line, that are individually selected by SCB0 + and SCB1 + decoded. The device is enabled by a LAD enabler. RDA + is a function of the strobe pulse, WRITE + , and input-data-request. Note that DRDA− inhibits the RDA + strobe if an overrun error occurs (OEB +) after the input data-request sequence has begun. RDA + is also enabled when a line is first put in receving mode to clear the data ready flag, so that erroneous data are not transferred to the computer.

Reset status input (RSI +): This signal clears the individual control-channel edge-detectors after a input status-request has been made. RSI + is distributed to the edge detectors in the same manner as RDA + . RSI + occurs when the ICS bit is first enabled. This ensures that the edge-detectors are cleared when a line is first enabled. RSI + also occurs

Table 3-10. Pin Functions of the Asynchronous Receiver/Transmitter (continued)

Pin	Symbol	Name	Function
15	ROR	Receiver overrun	This tristate output (enabled by SWE) is high if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer-register
16	SWE	Status word enabler	A low-level input enables the outputs (RPE, RFE, ROF, RDA, and TBMT) of the status-word buffer-register
17	RCP	Receiver clock	This input is a clock whose frequency is 16 times the desired receiver baud rate
18	RDAR	Receiver data-available reset	A low-level input forces the RDA output low
19	RDA	Receiver data available	This tristate output (enabled by SWE) is high when an entire character has been received and transferred into the receiver buffer-register
20	RSI	Receiver serial input	This input accepts the serial-bit input stream; a high-(mark) to-low (space) transition is required to initiate data reception
21	MR	Master reset	This input is pulsed to a high level after power turn-on, setting TSP, TEOC, and TMBT high and resets RDA, RPE, RFE, and ROR low
22	TBMT	Transmitter buffer empty	This tristate output (enabled by SWE) is high when the transmitter buffer-register can be loaded with new data
23	TDS	Transmitter data strobe	A low input strobe enters the data bits into the transmitter buffer-register
24	TEOC	Transmitter end-of-character	This output appears high each time a full character is transmitted, and remains high until the start of transmission of the next character (or for one-half of a TCP period in the case of continuous transmission)
25	TSO	Transmitter serial output	This output provides the entire transmitted character serially, and remains high when no data are being transmitted
26 through 33	TD1 through TD8	Transmitter data inputs	Eight data input lines (strobed by TDS) are available; unused data input lines, as selected by NDB1 and NDB2, may be in either logic state (LSB should always be placed on TD1)
34	CS	Control strobe	A high input enters the control bits (NDB1, NDB2, NSB, POE, and NPB) into

(continued)

generate RDCX+, which is applied to the MOS receiver and the control line logic. In addition, a DTL/TTL-compatible open-collector negative-true serial output (SDX–) is provided.

3.2.8.2 Current-Loop Interface

This version provides an isolated 20-60 mA., maximum 120V dc interface. Isolation exceeds 10 megohms at 50V dc common mode. The interface requires a user-supplied line battery power source.

SDX is ANDed with high-speed clock CLK-B via jumper Y-Z and driven through a current-driver as SDX+D. This serrated serial-data signal is applied to one side of T1 for isolation from the discrete driver Q1. While data are true (marking), Q1 is kept on by the half-wave rectified output of T1. OUTX– and OUTX+ form the driving half of the current loop. The current-loop receiver is an optically isolated IC. 20 to 60 mA of current flowing between INX+ and INX– cause the LED in the receiver to turn on the phototransistor driver. The output of the transistor is buffered to generate ROCX+.

3.2.8.3 Relay Interface

SDX+D (buffered SDX+) is applied to the coil of K1. The outputs available are a normally closed pair (NCX and NCSX), a normally open pair (NOX and NOSX). A form C closure may be emulated by tying NOSX and NCSX together. The receiver (RLYX+ and RLYX–) are the two sides of a relay coil. If R33 is shorted out, 12V dc will activate the relay to make RDCX true.

3.2.8.4 TTL/DTL Interface

The direct-connection LAD can serve as a TTL/DTL interface. There is an open-collector TTL driver with 70 mA sinking capacity, and the RS232 receiver can be used as a DTL receiver presenting a 8.3 mA load to the input line. The maximum cable length is 20 feet (6 meters).

3.3 MAINTENANCE

The following equipment is required to maintain the LAD:

a. Varian 620-series or V73 computer with at least 8K of memory

b. Data communications multiplexor

c. An I/O expansion chassis for the DCM backplane

d. An I/O expansion power supply

e. One card extender (44 D 0015 or 44 D 0540 000)

f. Two test connectors (burndy edge connectors 57 A 0036 000) wired for the applicable interface:

1. RS232 interface (44 D 0654 002): Install jumpers as follows:

Pin 2 to pin 22
Pin 4 to pin 24

2. Current-loop interface: (44 D 0654 001): Install jumpers as follows:

Pin 3 to pin 11
Pin 29 to pin 39
Pin 37 to pin 40
Pin 27 to pin 34 to pin 6
Pin 12 to pin 7

Note: R27, R30, R39, R42, R51, R54, R63, and R66 must be shorted across when using this test connector.

3. Relay interface (44 D 0654 000): Install jumpers as follows:

Pin 1 to pin 25 to pin 44
Pin 10 to pin 5
Pin 31 to pin 38
Pin 7 to pin 27 to pin 37

Note: R33, R29, R45, R41, R53, R57, R65, and R69 must be shorted across, and jumpers placed where R22 and R46 are mounted in order to use this test connector.

g. Software tapes:

MAINTAIN II Test Executive	92 U 0107 001
DCM Test Program	92 U 0106 009B

h. One oscilloscope, Tektronix 547 or equivalent

The following system configuration features must be checked before testing:

a. Data format (this will be changed during testing and thus must be to the original configuration after testing is completed)

b. If the current-loop LAD is being tested, ensure that CLKB+ is wired to P1 pin 44 of the LAD slot.

c. Line bit-rate selection (ensure that each line has an input clock; reset the rates to system specifications if they have been changed during testing)

3.3.1 Functional Tests

The following tests use portions of the DCM test program. The specific test required is called out in each section.

Input/output test: Verify that each line can transmit and receive a binary data pattern without errors. Run test 1

where the bits, when set, indicate:

u = Both output buffer and output register empty (this bit, when set, causes a status-change interrupt if the i-bit, bit 14, is set in the line control byte)

c = The control-line-in from the terminal is on (this control line is usually tied to the receive-data line and any change of state in this line causes a status-change interrupt to be generated if the c-bit was set in the control word.
Note: When this function is used, the receiver is not active to receive data)

x = Not used (zero)

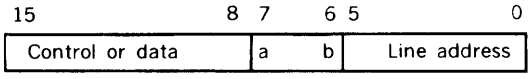
3.4.2 Programming Sequences

This section describes the line setup and status-reading control sequences used with the direct-connection LAD. General DCM programming sequences are given in section 2.4.4.

3.4.2.1 Line Setup Sequence

This sequence begins with an EXC 0570 instruction. The DCM generates a control interrupt as soon as it is free. The program responds with OAR 070. The DCM loads the specified line and resumes scanning.

The character output by OAR 070 has the format:

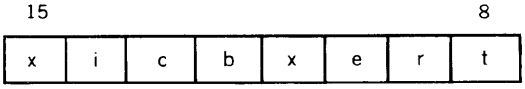


where a and b indicate the contents of the more-significant byte as follows:

ab	
00	Data to output buffer
01	Control
10	Not used
11	Not used

DATA BYTE FORMAT (ab = 00): When ab = 00, the more-significant byte contains data, which are right-justified (i.e., bit 8 is the least-significant data bit regardless of character-length, and unused bits, if any, are zeros).

CONTROL BYTE FORMAT (ab = 01): When ab = 01, the more-significant byte contains control information in the format:



3.5 MNEMONICS

Mnemonic	Description
AI through BI	Decoded to indicate type of line error
CCx	Control-line input change
CCM	Multiplexed line from CC0 through CC3
CLK	614,400 Hz clock from MU
CS1x CS2x	20 mA current source from – 12V dc for testing
CST	Control strobe
CSTx	Control strobe for line control registers
DR	OR-tied data-ready line from the UARTs
E	Enable echo bit
EDTA	Enable input
ENOUT	Enable output
EOB	Enable status input
FE	Framing error
ICS	Input control-status enabling bit is control register
IDR	Input data-request to MU
IDRS	Stored input data request
IDRSD	Input data request to service request register
INx + INx–	Current loop input (20-60 mA = 1; 1 mA or less = 0)
LADA	LAD address input
LADE	Enable LAD address input
LAE	Enable LAD
LERR	Line error to MU
LERRS	Stored line-error status
MB0 through MB7	Multiplexor data bus
MT	Underflow
NCx	Form B relay serial output (closed = 1; open = 0)
NCSx	Form B relay serial output (closed = 1; open = 0)
NOx NOSx	Form A relay serial output (open = 1; closed = 0)
OBRKx	Output break
ODR	Output data request to MU
ODRSD	Output data request to service-request register
OE	Overrun error
OUTx + OUTx–	Current loop serial output (20 mA = 1; 1 mA or less = 0)
PE	Parity error
R	Enable receiving mode
RD0 through RD7	Received data
RDA	Reset data available
RDAx	Reset data available strobes
RDCx	Serial received data lines
RDDSx	RS232 serial input
RDSTRB	Read strobe
RLYx + RLYx–	Relay serial input
RSI	Reset status input request
RSIx	Reset status input request strobe
SB0	Underflow status bit
SB1	Control-line output (read data) status bit
SBRKx	Strobe break logic
SCANx	Individual line enablers for tristate output devices
SCB0 SCB1	Decoded to address one of four lines
SDx	DTL serial data

(continued)

SECTION 4
ASYNCHRONOUS RS232 MODEM LINE-ADAPTER

This LAD (figure 4-1) provides an EIA RS232C interface for the DCM. It can handle four asynchronous modems (datasets), specifically the Bell 103 and 202 datasets or their equivalents. Since its interface circuits are compatible with the CCITT V24 specification, this LAD can also interface with European datasets compatible with the Bell 103 and 202.

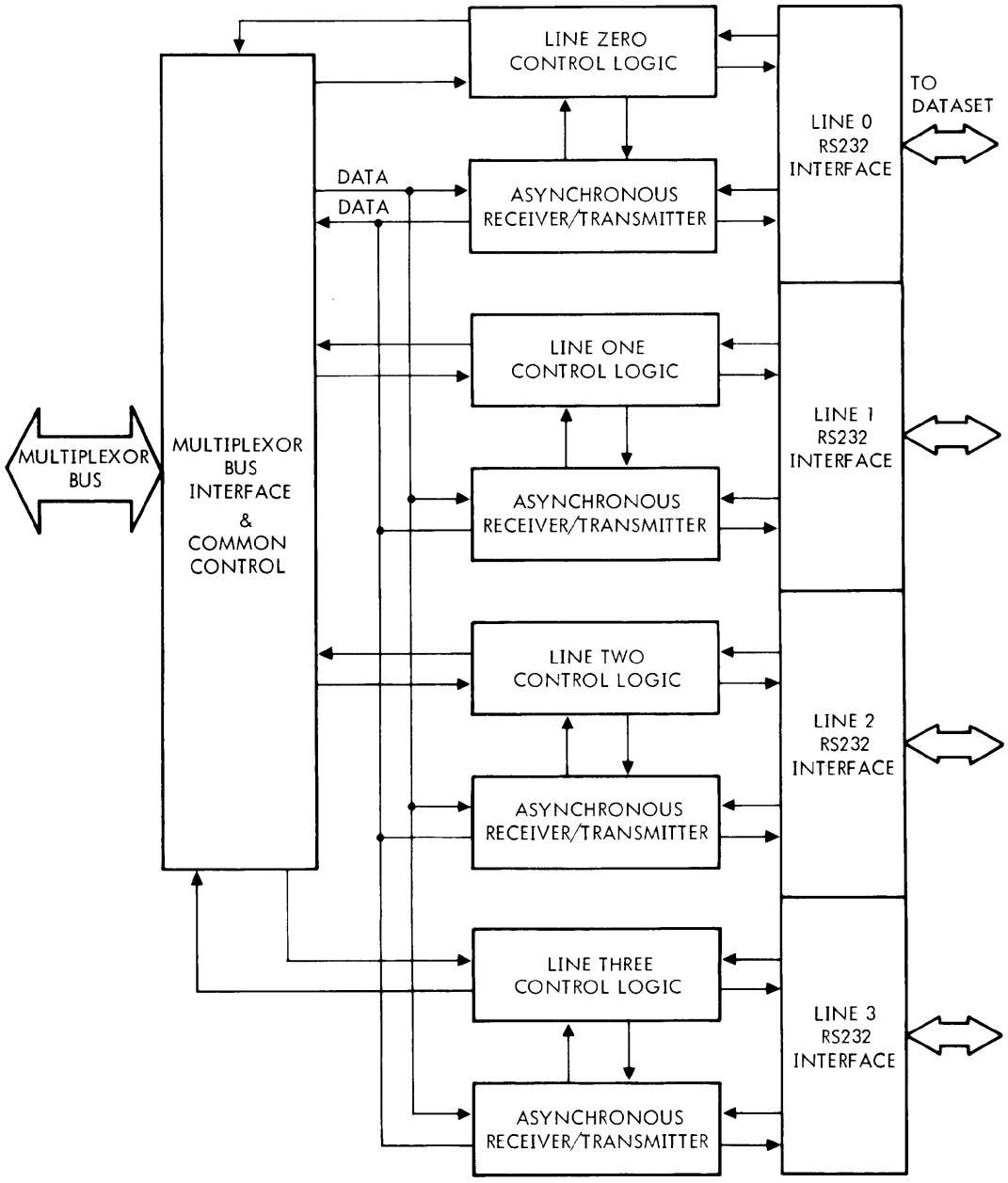


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Figure 4-1. Asynchronous RS232 LAD Simplified Block Diagram

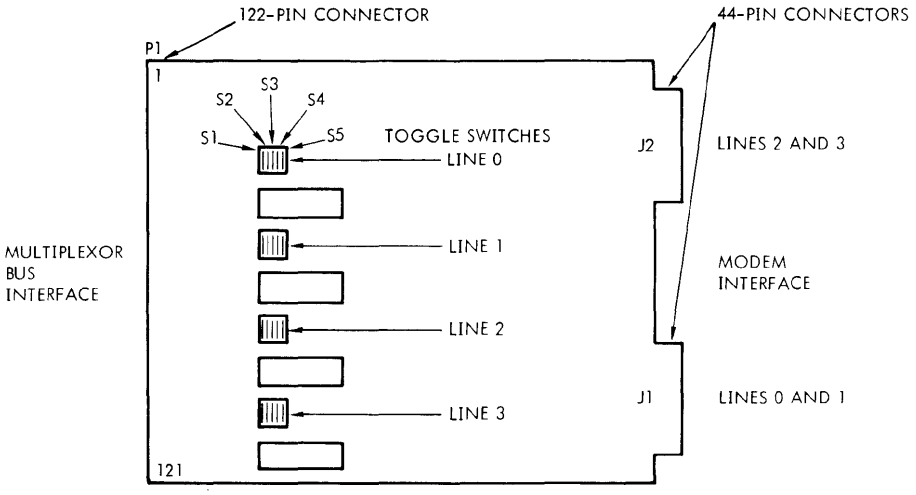

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Figure 4-2. Asynchronous RS232 Modem LAD

4.1.2 Interfaces

The LAD interfaces with the MU over the multiplexor bus (figures 1-1 and 2-1), and with the datasets over the RS232 modem interface (section 4.2.4).

Pin assignments are given on the logic diagrams in Volume 2 of this manual.

4.1.2.1 Multiplexor Bus

The 38-line multiplexor bus connects the LAD with the MU. It is described in section 2.1.2.2.

4.1.2.2 RS232 Modem Interface

This interface is described in section 4.2.4.

4.1.3 Options

Parity (odd, even, or none), character length (5, 6, 7, or 8 bits), and the number of stop bits (1 or 2) are set on a line-by-line basis using the data-format toggle switches (figure 4-2) as follows:

	Switch	1 PS	2 WLS1	3 WLS2	4 SBS	5 PI
Parity	Odd	On				On
	Even	Off				On
	None					Off
Length	5		On	On		
	6		Off	On		
	7		On	Off		
	8		Off	Off		
Stop bits	1				On	
	2				Off	

The standard automatic echo of received characters can be disabled by removal of a jumper.

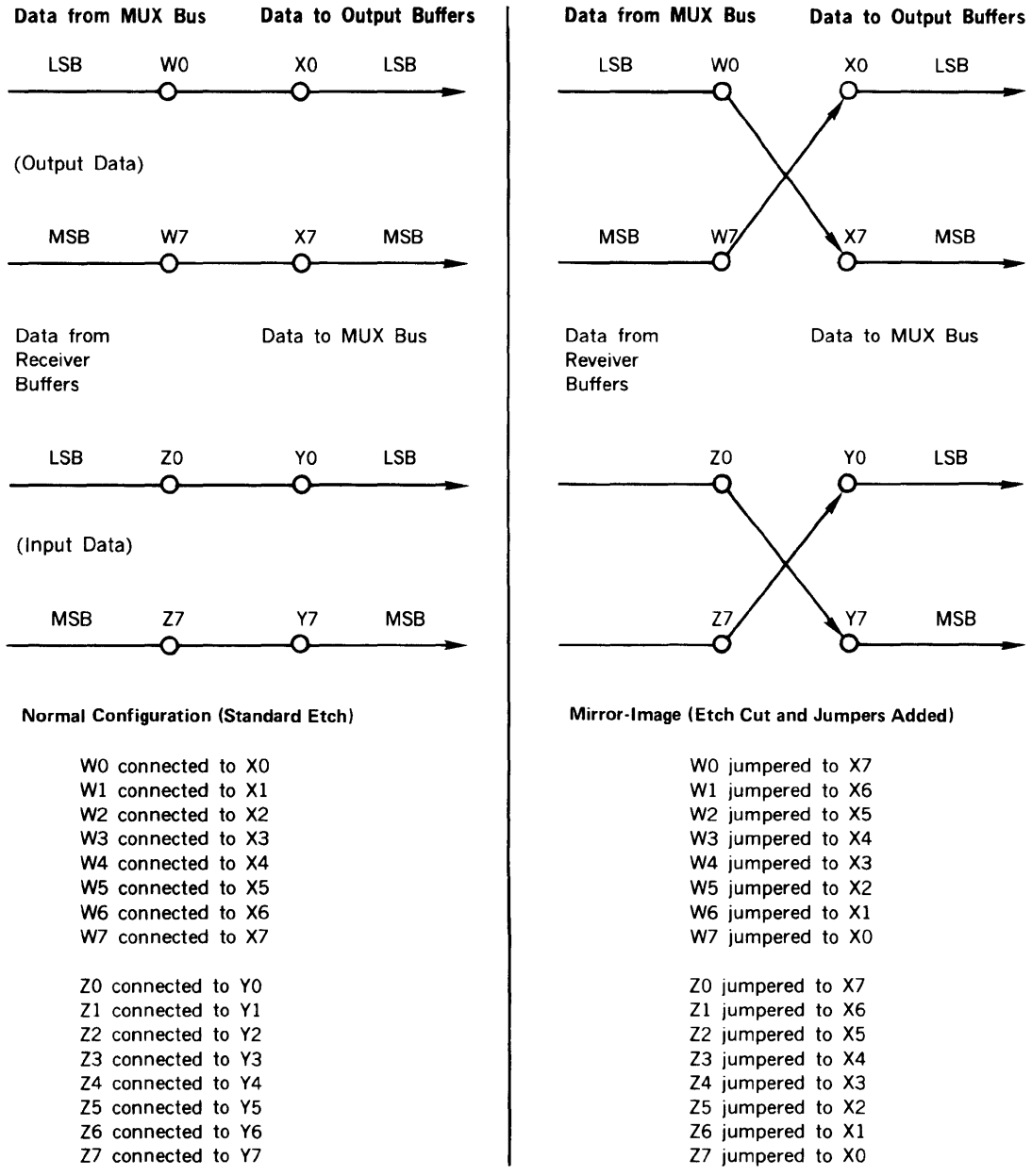

Figure 4-3. Normal Mirror-Image Data Transmission

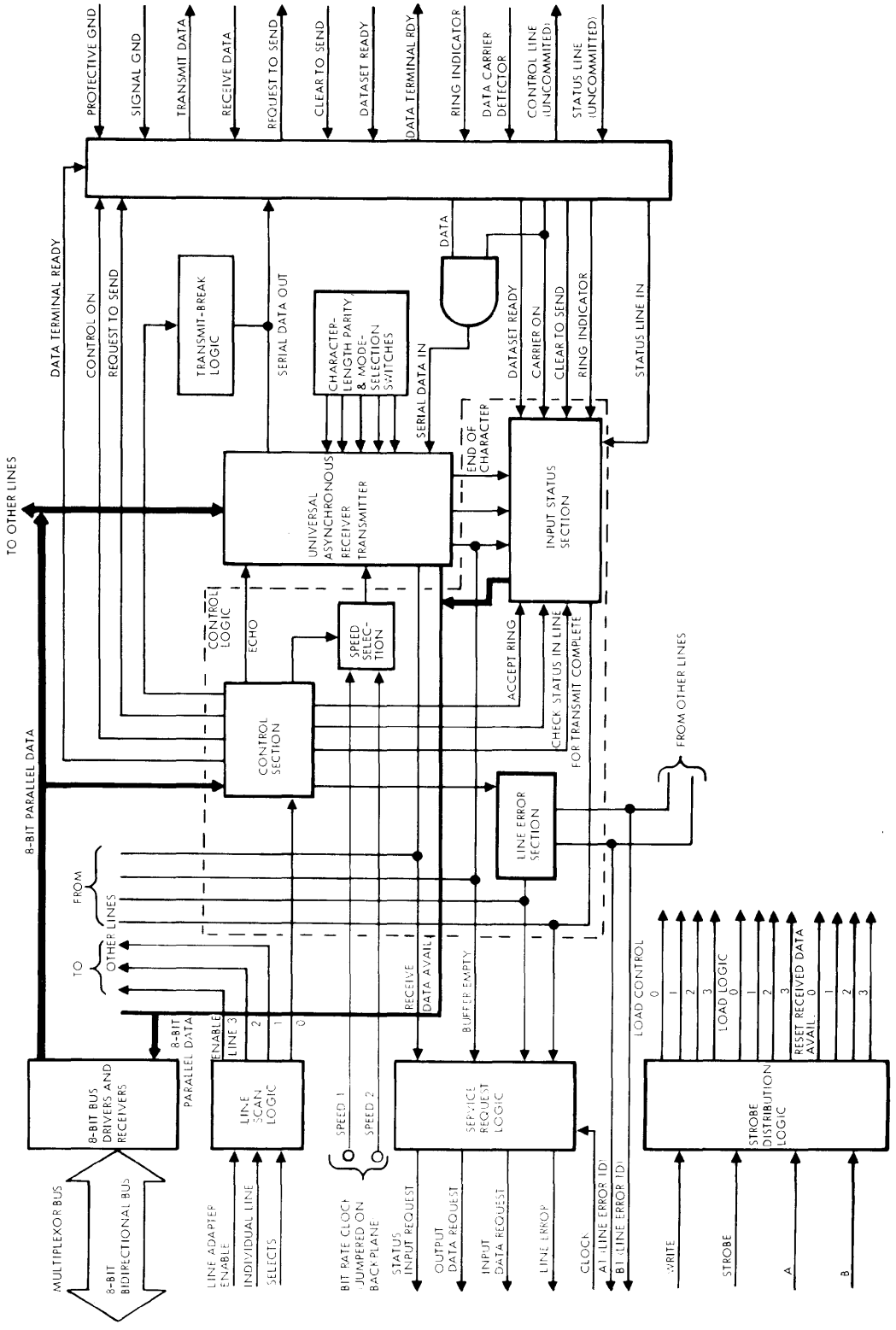

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Figure 4-5. Asynchronous RS232 Modem Line Adapter Detailed Block Diagram (One Line Shown)

CCM + (multiplexed CCR0 +, CCR1 +, CCR2 +, and CCR3 +) is sent to the input status-request logic. A strobe causes the flip-flop to go to the state of the control-channel input after the input status-request has been acknowledged.

4.2.7 Asynchronous Receiver/Transmitter

The asynchronous receiver/transmitter section for each line (zero through three) are identical. They are general purpose, programmable MOS/LSI devices for the transmission and receipt of asynchronous serial data. The transmitter converts parallel data into a serial word that contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data and verifies proper code transmission by checking parity and the receipt of a valid stop bit. Both receiver and transmitter are character-buffered. The line toggle-switches can be set up for a word length of 5, 6, 7, or 8 bits; even, odd or no parity; and one or two stop-bits (section 4.1.3). Table 4-4 gives the individual signal descriptions.

Table 4-4 Pin Functions of the Asynchronous Receiver/ Transmitter

Pin	Symbol	Name	Function
1	VSS	Power supply	+5V supply
2	VDD	Power supply	-12V supply
3	GND	Ground	Ground
4	RDE	Receiver data enabler	A low-level input enables the outputs (RD8 through RD1) of the receiver buffer-register.
5 through 12	RD8 through	Receiver data outputs	These are the 8 tristate data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right-justified, i.e., the LSB always appears on the RD1 output.
13	PRE	Receiver parity error	This tristate output (enabled by SWE) is high if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver framing error	This tristate output (enabled by SWE) is high if the received character has no valid stop-bit.
15	ROR	Receiver overrun	This tristate output (enabled by SWE) is high if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer-register.
16	SWE	Status word enabler	A low-level input enables the outputs (RPE, RFE, ROF, RDA, and TBMT) of the status-word buffer-register.
17	RCP	Receiver clock	This input is a clock whose frequency is 16 times the desired receiver baud rate.
18	RDAR	Receiver data-available reset	A low-level input forces the RDA output low.

(continued)

Table 4-4 Pin Functions of the Asynchronous Receiver/ Transmitter (continued)

Pin	Symbol	Name	Function
37 through 38	NDB2, NDB1	Number of data bits/ character	These two inputs are decoded internally to select 5, 6, 7, or 8 data-bits/ character as follows: NDB2 NDB1 Data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Select odd/even parity	The logic levels on this input and on NPB, determine the parity mode for both the receiver and transmitter, as follows: NPB POE L L Odd parity L H Even parity H No parity
40	TCP	Transmitter clock	This input is a clock whose frequency is 16 time the desired transmitter baud rate.

4.2.8 Transmit-Break Logic

Each line has logic to transmit break characters. This circuitry consists of two flip-flops and an exclusive-NOR gate. The first flip-flop is set by the data strobe when AR + is true. The second is set when the transmission-register-empty flag goes false (TREO– for line zero) and the first flip-flop cleared. The output of the second flip-flop forces the data transmission line to a space condition for one character. At the end of that character, the transmission-register-empty flag momentarily goes true while a new character is loaded into the transmission register, causing the break flip-flop to be clocked again. If the first flip-flop had been set again while the previous break character was being output, the second flip-flop remains set after the clock. Note that the data being input to the asynchronous receiver/transmitter have no effect; the device is only used while transmitting breaks for timing.

The LAD also has two general-purpose lines that can be used to indicate that the reverse channel is on ("input control line") and to turn on the reverse channel ("output control line"). Note that the LAD does *not* provide data communications capability over the reverse channel.

These general-purpose lines can also be used for input and output speed selection (RS232C circuits CH– and CI–).

4.2.9 RS232 Modem Interface

This interface conforms to the RS232C and CCITT V24 standards and provides for the following signals for each line (pin numbers are indicated in table 4-5):

AA–	Protective ground
AB–	Signal ground
BA–	Transmitted data
BB–	Received data
CA–	Request to send
CB–	Clear to send
CC–	Dataset ready
CD–	Data terminal ready
CE–	Ring indicator
CF–	Data carrier detector

The LAD also has two general-purpose lines that can be used to indicate that the reverse channel is on ("input control line") and to turn on the reverse channel ("output control line"). Note that the LAD does *not* provide data communications capability over the reverse channel.

These general-purpose lines can also be used for input and output speed selection (RS232C circuits CH– and CI–).

The interface provides +12V dc and –12V dc through 1K resistors to hardwire certain leads on for testing or for non-standard datasets. Thus, to use this LAD without a dataset (direct connection): Tie CB–, CC–, and CF– to the +12V dc provided.

4.3 MAINTENANCE

The following equipment is required to maintain the LAD:

a. Varian 620-series or V73 computer with at least 8K of memory

b. Data communications multiplexor

c. An I/O expansion chassis for the DCM backplane

d. An I/O expansion power supply

e. One card extender (44 D 0015 or 44 D 0540 000)

f. Two test connectors (burndy edge connectors 57 A 0036 000) wired as follows:

Line 0	1.	Pin 29 to pin 35	Data-terminal-ready to ring-indicator
		Pin 35 to pin 33	Ring-indicator to dataset-ready
		Pin 29 to pin 25	Data-terminal-ready to carrier-on
	2.	Pin 27 to pin 37	Request-to-send to clear-to-send
	3.	Pin 31 to pin 23	Transmit-data to receive-data
	4.	Pin 21 to pin 18	Control-out to control-in
Line 1	5.	Pin 1 to pin 13	Data-terminal-ready to ring-indicator
		Pin 13 to pin 11	Ring-indicator to dataset-ready
		Pin 1 to pin 7	Data-terminal-ready to carrier-on
	6.	Pin 3 to pin 19	Request-to-send to clear-to-send
	7.	Pin 5 to pin 9	Transmit-data to receive-data
	8.	Pin 6 to pin 8	Control-out to control-in

The following additional jumpers can be added so the test connector can also be used on a synchronous RS232 interface LAD.

Pin 38 to pin 39
Pin 39 to pin 41
Pin 38 to pin 17
Pin 17 to pin 15

These jumpers tie the test clock to the receive/transmit clock inputs.

g. Software tapes:

MAINTAIN II Test Executive	92 U 0107-001
DCM Test Program	92 U 0106-009B

h. One oscilloscope, Tektronix 547 or equivalent

The following system configuration features must be checked before testing:

a. Data format (this will be changed during testing and thus must be reset to the original configuration after testing)

b. Mirror-image mode or normal-data mode

c. Hardware echo, if required

d. Line bit-rate selection (ensure that each line has two input clocks; reset the rates to system specifications if they have been changed during testing)

4.3.1 Functional Tests

The following tests use portions of the DCM test program. The specific test required is called out in each section.

Input/output test: Verify that each line can transmit and receive a binary data pattern without errors. Run test 1 using all possible data formats (i.e., 5-, 6-, 7-, and 8-bit data, with and without parity, and with one or two stop bits). While running test 1, verify that the serial data out of each line (TDA0– through TDA3–) is in the range +9V to +12V for set bits and –9V to –12V for reset bits.

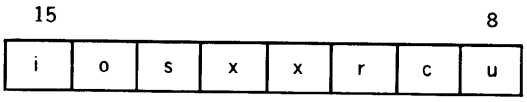
Speed-selection test: Verify that each line can transmit and receive data with speed B selected. Use test 3.

Break test: Verify that each line can transmit break characters and detect break characters on input. Test 4 checks these features.

Parity-error detection test: Verify that each line can detect input parity errors. This can be accomplished by switching from the one to two stop-bit data pattern, or by switching the parity enabler on and off while running test 1. The test prints out the error, if detected.

4.4.1.2 Status Change

This interrupt is explained in section 2.4.2.4. For the asynchronous RS232 modem LAD, the status bits have the format:



where the bits, when set, indicate:

u = Both output buffer and output register empty (this bit, when set, causes a status-change interrupt if the i-bit, bit 14, is set in the line control byte)

c = The control-line-in from the modem is on (this control line is usually tied to the modem secondary receive-data line, i.e., reverse channel, and any change of state in this line causes a status change interrupt to be generated if the line is in transmit or receive. Note: no matter what state this line is in when a line is first activitated, i.e., put in transmit and/or receive, no interrupt will be generated)

r = Ring indicator: indicates that the ring indicator line from the modem is on (if the control byte is set up correctly, this bit causes a status-change interrupt). Note: a R true and T false in the control byte.

x = Not used (zeros)

s = The clear-to-send line from the modem is on (does not initiate an interrupt)

o = The carrier-on line from the modem is on (does not initiate an interrupt)

i = The interlock line from the modem is on (does not initiate an interrupt)

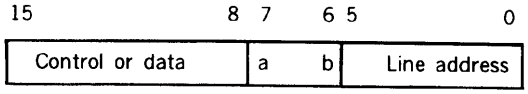
4.4.2 Programming Sequences

This section describes the line-setup and status-reading control sequences used with the asynchronous RS232 modem LAD. General DCM programming sequences are given in section 2.4.4.

4.4.2.1 Line Setup Sequence

This sequence begins with an EXC 0570 instruction. The DCM generates a control interrupt as soon as it is free. The program responds with OAR 070. The DCM loads the specified line and resumes scanning.

The character output by OAR 070 has the format:



where the bits, when set, indicate:

t = Transmission - (puts the line in transmission mode and enables the modem request-to-send line, the line begins making output-data requests as soon as clear-to-send is enabled by the modem, reports line breaks if the modem enables carrier-on. Note: A line must be kept in transmission mode until the last character to be transmitted is in the output register to prevent data loss).

r = Receiving - (puts the line in receiving mode; when carrier-on is enabled by the dataset, the line begins making input-data requests as data are received and reports line errors as they occur)

e = Echo mode - (allows the line to remain in the transmission mode and consequently leaves the modem request-to-send line enabled, but suppresses output-data requests, hardware automatically echos data as received unless this feature is disabled)

d = Data terminal ready - (enables the modem data-terminal-ready line, which allows automatic answer-back and automatic call-termination)

a = Accept ring/transmit break - (when the transmission bit is not set this bit causes a status-input-request interrupt when the ring-indicator line from the modem is enabled. When the transmission bit is set, this bit causes break characters to be transmitted. Note: this bit should be cleared by software upon receipt of the status-change-interrupt ring indicator mode to prevent repetitive interrupts)

c = Control line - (Enables the control line to the modem. Note: This line will usually be tied to the modem's secondary transmitted data line, i.e., the reverse channel)

i = Interrupt - (Causes a status-input request to be generated when both the output buffer and the output register are empty. Note: The software should clear this bit upon receipt of the status-change interrupt to prevent repetitive interrupts. It normally will be enabled when the multiplexor detects the byte count has gone to zero and automatically reloads the control byte). The line must not be in transmission mode unless the echo bit is set. The sequence to set the interrupt bit is:

a. Set up the control table with the buffer size; the control byte stored in the control table resets the transmission bit and sets the interrupt bit set

b. Put the line in transmission mode via a control sequence; the line sequentially outputs the data buffer, the byte count goes to zero, the line makes another output-data-request, the multiplexor transfers the control byte to the line, the line goes out of transmission mode, but keeps request-to-send high until the character in the output register is completely transmitted, then a status input request is made indicating the output buffer and the output register are empty

s = Speed selection - (Each line can operate at one of two hardwire selectable speeds; this bit selects speed B, which should be the higher of the two software-selectable speeds. Note: The bit should not be manipulated while a line is transmitting or receiving)

Mnemonic	Description
MB0– MB1–	8-bit multiplexor data bus
OBRKx–	Output break
ODR–	Output data request to MU
OE +	Overrun error from asynchronous receiver/transmitter
PE +	Parity error from asynchronous receiver/transmitter
P.GNDx	Power ground or chassis ground from modem
R +	Receive bit from the control registers
RDA +	Reset data available (data ready)
RDAx–	Reset data available to four asynchronous receiver/transmitters
RDCx +	Receive-data gated with carrier-on
RDSx–	Receive-data from modem
RD0 + through RD7 +	Parallel receive-data bus from asynchronous receiver transmitter
RIDx +	Ring indicator from modem
RIx–	Internal ring indicators
RSIx–	Reset status-input request to control channel edge-detector logic
RSI +	Reset status-input request
RTSx +	Request-to-send to modem
SBRK–	Start break
SBRKx–	Start break signals for the individual lines
SB0 + SB1 + SB2 + SB5 + SB6 + SB7 +	Status bits

Mnemonic	Description
SCANx–	Enables lines
SCB0 + SCB1 +	2 least-significant bits of the MU scan counter
SIR–	Status input request to MU
SIRSD +	Status input request to service request register
SPDAx–	Clock inputs from the multiplexor bus
SPDx +	Clocks to asynchronous receiver/transmitters
SRST–	System reset
STDD–	Strobe data
STDx–	Strobe data to asynchronous receiver/transmitters
STRBE–	Strobe from MU
Sx +	Speed-selection bit from control register
TBRE +	Transmission buffer empty from asynchronous receiver/transmitter
TDAx–	Transmit data to modem
TDx +	Transmit data from asynchronous receiver/transmitters
TM +	Multiplexed transmission
TOR–	Transmit or receive
TREAx +	Transmission register empty from asynchronous receiver/transmitters
TREM +	Multiplexed transmission-register-empty
Tx +	Transmission bits from control registers
WRITE–	Write line from MU

x = line number.

SECTION 5
SYNCHRONOUS RS232 MODEM LINE-ADAPTER

The LAD (figure 5-1) provides an EIA RS232C interface for the DCM. It can handle four synchronous modems (datasets), specifically the Bell 201, and 208 data sets or their equivalents. Since its interface circuits are compatible with the CCITT V24 specification, the LAD can also interface with European datasets compatible with the Bell 201, and 208.

The LAD interfaces with four full-duplex synchronous data communication lines at a maximum data rate of 20,000 bits per second. It provides character buffering for both input and output, can under program control automatically delete synchronization characters from the incoming data stream and add them to the output data stream when output data is not available to maintain line-synchronization, generates output parity (if any), and checks incoming data for correct parity (if any). The parity can be odd, even, or not used; the character length can be 5, 6, 7, or 8 bits; and separate synchronization character storage is provided for transmission and receipt.

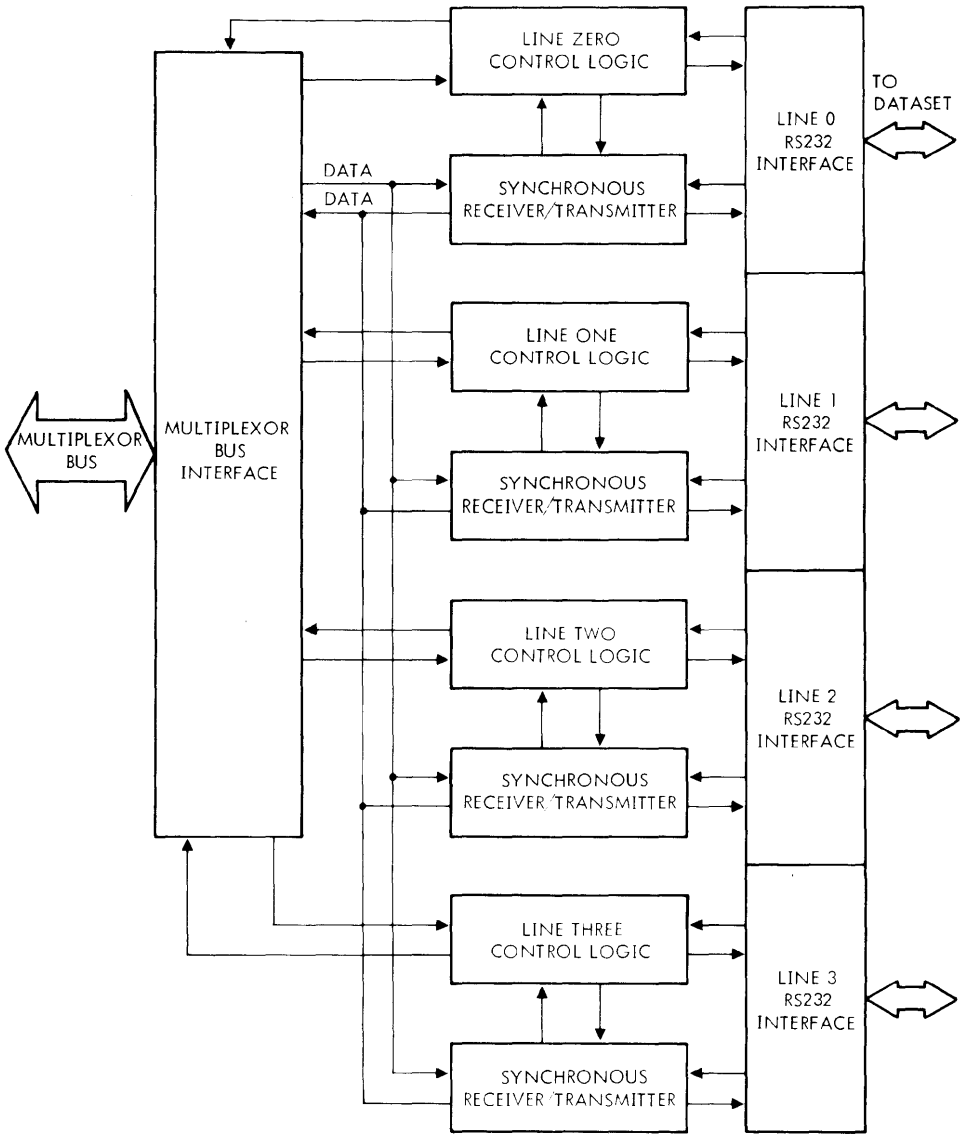


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Figure 5-1. Synchronous RS232 LAD Simplified Block Diagram

5.1 INSTALLATION

The LAD has been inspected and packed to ensure its arrival in good working order. To prevent damage, take reasonable care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If any is found:

a. Notify the transportation company

b. Notify Varian Data Machines

c. Save all packing material

5.1.1 Physical Description

The synchronous RS232 modem LAD is on one printed-circuit board (figure 5-2) mounted in a specially-wired expansion chassis (figures 1-2 and 1-3).

5.1.2 Interfaces

The LAD interfaces with the MU over the multiplexor bus (figures 1-1 and 2-1), and with the datasets over the RS232 modem interface (section 5.2.4).

5.1.2.1 Multiplexor Bus

The 38-line multiplexor bus connects the LAD with the MU. It is described in section 2.1.1.1.

5.1.2.2 RS232 Modem Interface

This interface is described in section 5.2.7.

5.1.3 Options

Parity (odd, even, or none), and character length (5, 6, 7, or 8 bits), are set on a line-by-line basis with jumpers (figure 5-2) set according to tables 5-2 and 5-3.

5.1.4 Test Clock Selection

This LAD provides a test clock input from the DCM backplane. This test clock is used when testing the LAD without a modem. The frequency of the clock should be at least 4800 bits per second. Table 5-4 shows the multiplexor bit-rate locations and the standard frequencies. The input pin number for the test clock is 92. (Note: The test clock is used "as is" and not divided down by 16 as in asynchronous LADS.)

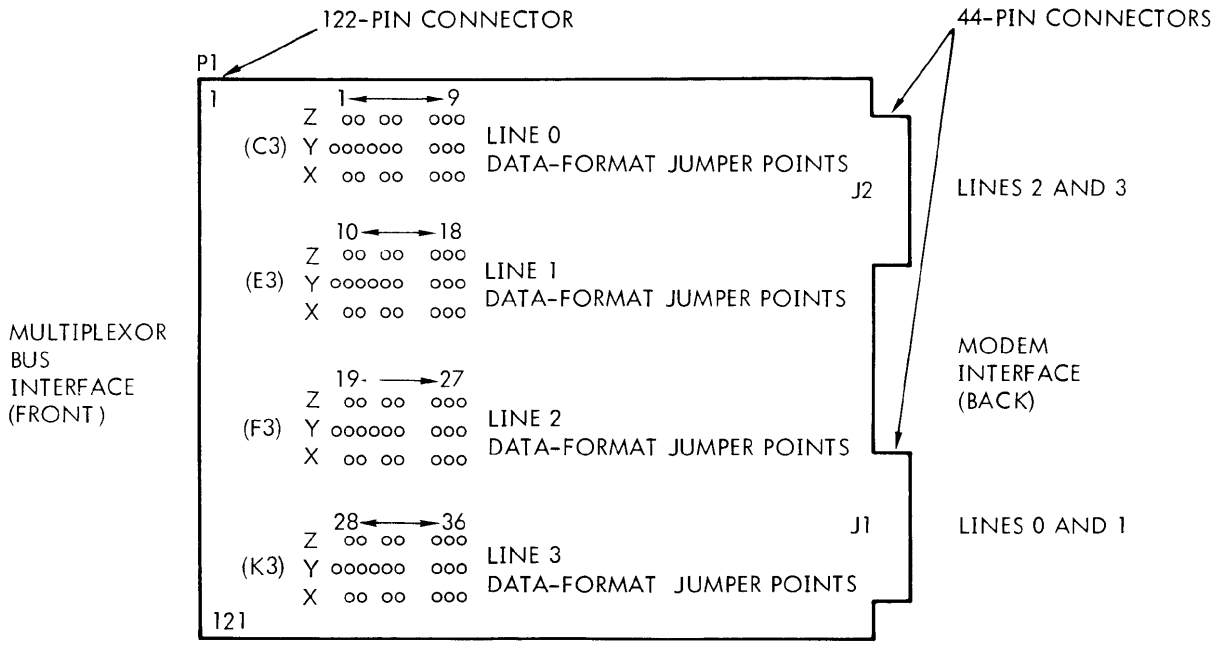

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Figure 5-2. Synchronous RS232 Modem LAD

5.1.5 Protective Ground (RS232C Circuit AA)

The protective ground lines are not normally wired. If these signals are to be used, jumpers must be added as indicated in table 5-5. These jumpers bring the protective ground lines from the modem out to free pins on the DCM backplane where they should be routed to power ground. They should not be tied to signal or DC ground.

Table 5-5. Protective Ground Jumpers

Line	Jumper	Mnemonic	Backplane Pin
0	M to M	P. GND 0	69
1	N to N	P. GND 1	67
2	R to R	P. GND 2	65
3	S to S	P. GND 3	63

5.2 THEORY OF OPERATION

This section explains the operation of the synchronous RS232 modem LAD, with each subsection corresponding to a block (or set of blocks) on the LAD block diagram (figure 5-1). Figure 5-3 is a detailed block diagram. Refer to logic diagram 91B0414 for understanding this theory.

5.2.1 Multiplexor Bus Interface

This logic provides a common interface for the four lines of the LAD to the multiplexor bus (section 2.1.2.2). This interface includes provision for jumpering an internal clock for testing and assigns the LAD an address on the multiplexor bus.

5.2.2 Service Request Logic

The three service-request terms IDRSD+, ODRSD+, and SIRSD+ are clocked into the service-request register on the positive transition of CLK−. The outputs of the register are gated to form a priority structure where the input data-request has the highest priority and the input status-request has the lowest. When an input data-request is made, a line error may be reported (LERR−). If a line error has occurred, the AI−, and BI− identify the type of error.

Input data-request (IDRSD+): An input data-request is made if the input-data-request flag from the lines sync-detection logic is true.

Output data-request (ODRSD+): An output data-request is made if the transmission buffer is empty (TBMTM+), the line is in transmission mode (TM+), the accept-ring/stop-output bits is not set (ARM−), and a input status-request is not pending to report an underflow (SIRS3−).

Input status-request (SIRSD+): A input status-request is made under the following conditions:

a. The line is in transmission or receiving mode and a change of state in the control-line-in is detected (SIRS2−).

b. The line is not in transmission mode and a ring occurs (SB2+) and the accept-ring/stop-output bit is true (SIRS1−).

c. The interrupt bit is true (IM+) and a sync-character is transmitted from the sync-character-register (SB0+), (SIRS2−).

5.2.3 Control Logic

The control logic for each line (zero through three) is identical. It provides steering logic for data/control transfer to and from the line, storage flip-flops for the control and status bytes, break-transmitting logic, and service-request generation logic (i.e., input or output data requests, etc.).

Control of each line is through four eight-bit control registers (one for each line). The register is loaded by software via a control sequence and the outputs enable the various line functions. Each control-bit function is described below.

Delete synchronization: The DS0, DS1, DS2, and DS3 bits are distributed to the appropriate line sync-detection logic. When set, they suppress the input data requests on received characters that match the contents of the receive-sync-character register.

Interrupt on underflow: The I0, I1, I2, and I3 bits are multiplexed together to form IM+. IM+ causes status-input-request whenever an underflow condition exists (sync-character transmitted).

Control-line: C0−, C1−, C2−, and C3− enable and disable individual output control lines.

Accept ring/stop output: The AR0, AR1, AR2, and AR3 bits are multiplexed together to form ARM. ARM enables a

status-input-request if the line is not in transmission or receiving mode and a ring occurs (SB2+). ARM inhibits output requests if the line is in transmission mode.

Data terminal ready: DTR0–, DTR1–, DTR2–, and DTR3– enable the data-terminal-ready signal to the modems.

Parity enabler: P0, P1, P2, and P3 enable the seven-bit data with parity format. The function in only operational if the line is set up for eight-bit data without parity.

Receiving: R0, R1, R2, and R3 enable receiving mode.

Transmission: T0, T1, T2, and T3 enable transmission mode.

5.2.4 Synchronous Receiver/Transmitter

The synchronous receiver/transmitter is a general purpose, programmable MOS/LSI device for the transmission and receipt of synchronous serial data. The transmitter converts parallel data into serial words that contain both data and parity (if any). The receiver converts serial words into parallel data and verifies proper transmission by checking parity (if any). Both the receiver and the transmitter are character-buffered. The line jumpers can be set up for a word length of 5, 6, 7, or 8 bits; and even, odd, or no parity (section 5.1.3). Table 5-6 describes the pin functions of the device.

The synchronous receiver/transmitter also provides storage for a receiver synchronization-character (RSC) and a transmitter synchronization-character (TSC). The RSC obtains character-synchronization at the beginning of a message and deletes synchronization-characters that are embeded in the incoming message. TSCs are inserted in the outgoing data stream whenever data is not provided fast enough to maintain synchronization on the line.

The input clock frequency for the receiver is set by the modem and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the receiver-reset input goes from a high to a low, the receiver enters search mode (bit phase). In search mode, the serially received data-bit stream is examined on a bit-by-bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync-register and the receiver shift-register are identical. When this occurs, the sync-character-received output goes high. This character is then loaded into the receiver buffer-register and the receiver enters character mode. In this mode, each character received is loaded into the receiver buffer-register. The receiver provides flags for receiver-data-available, receiver-overrun, receiver-parity-error, and sync-character-received. Full double buffering eliminates the need for precise external timing by allowing one full character period for received data to be read out.

The input clock frequency for the transmitter is set by the modem and the desired transmitter sync-character is loaded into the transmitter sync-register. Internal logic decides if the character to be transmitted out of the transmitter shift-register is extracted from the transmitter data-register or the transmitter sync-register. The next character transmitted is extracted from the transmitter data-register provided a transmitter-data-strobe pulse occurs during the presently transmitted character. If there is no pulse, the next character transmitted is extracted from the transmitter sync-register and the sync-character-transmitted output is set high. Full double buffering eliminates the need for precise external timing by allowing one full character period to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tristate receive-data-output levels are provided for the bus structure oriented signals.

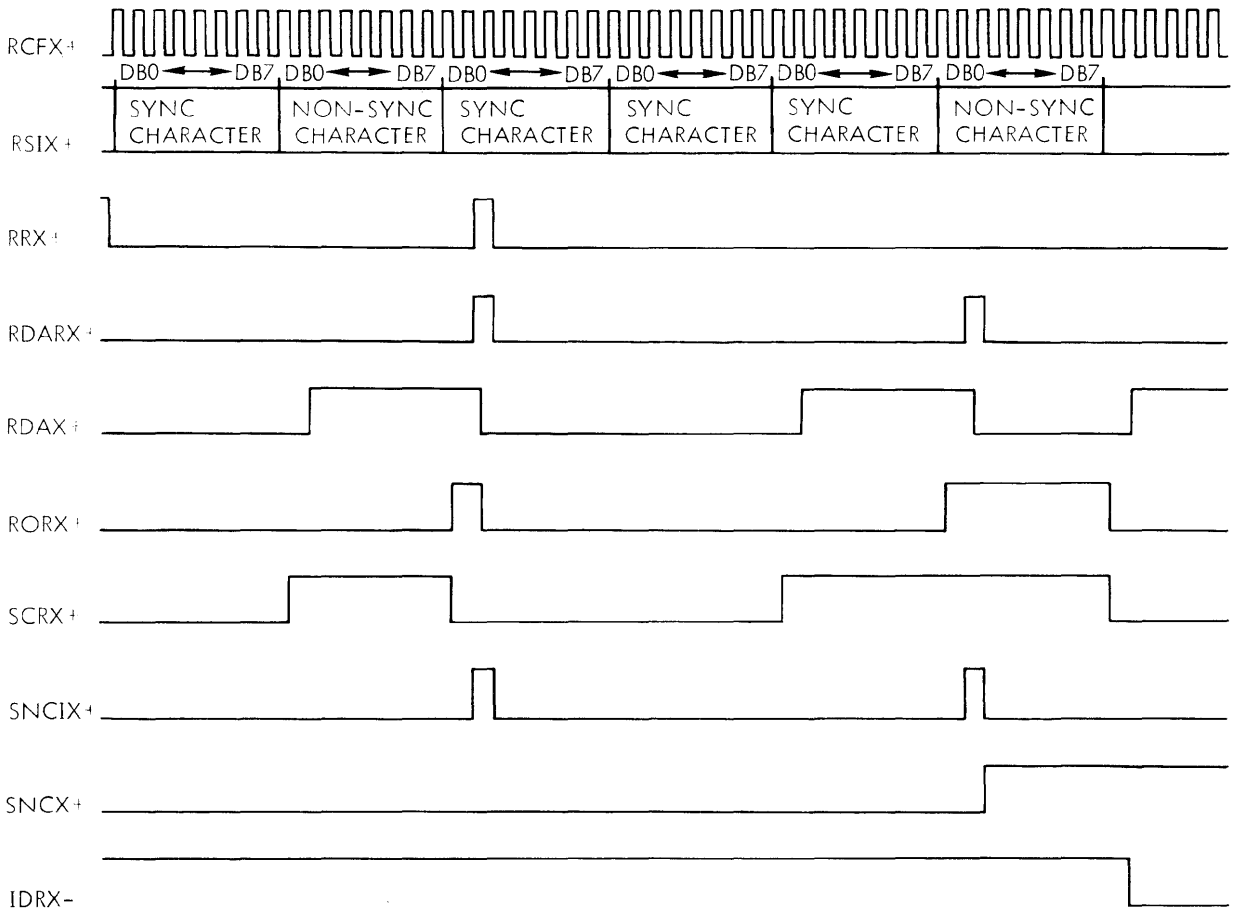
Table 5-6. Pin Functions of the Synchronous Receiver/Transmitter *(continued)*

Pin	Symbol	Name	Function
			the receiver is set into the character mode. In this mode, each character received is loaded into the receiver buffer-register
16	RPE	Receiver parity error	This output is high if the received character parity bit does not agree with the selected parity
17	SCR	Sync character received	This output is high whenever a character loaded into the receiver buffer-register is identical to the character in the receiver sync register. This output goes low the next time the receiver buffer-register is loaded with a character that is not a sync character
18	TSS	Transmitter sync strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register
19	TCP	Transmitter clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency
20	TDS	Transmitter data-buffer strobe	A high input strobe loads the character on the DB1-DB8 lines into the transmitter data-buffer register
21	RSS	Receiver sync strobe	A high input strobe loads the character on the DB1-DB8 lines into the receiver sync register
22	RSI	Receiver serial input	This input accepts the serial bit-input stream
23	RCP	Receiver clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency
24	RDAR	Receiver data available reset	A high input resets the RDA output to a low
25	RDE	Receiver data enable	A high input enables the outputs (RD8-RD1) of the receiver buffer-register
26	RDA	Receiver data available	This output is high when an entire character has been received and transferred into the receiver buffer-register
27	ROR	Receiver overrun	This output is high if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register

one more character. At the detection of the overrun, the detection logic sets the SNC1 flip-flop on the next negative clock transition. One clock period later, the SNC flip-flop sets if the second character was a sync character (SCRA true) and enables the input data request signal for succeeding characters. If the second character was not a sync character, the receiver is reset (SNF0−) and begins, once again, checking for synchronization in bit mode. Note that the SNC1 flip-flop causes the reset data available signal (RDAR+) to go true so that the first two sync detection characters are not transferred to the computer. If the delete-sync bit is set (DS+), RDAR goes true for every sync-character received and IDR is inhibited. RDS causes receiver-data-available to be reset in normal operation after the character is transferred to the computer.

5.2.6 Control-Channel Edge-Detectors

This logic consists of four separate identical sections (one for each line). Each section contains a flip-flop to store the state of the control line, and an exclusive NOR gate compare the control channel input state with the flip-flop state. If a difference is detected, a high signal (CCM+ - multiplexed term of CCR0+, CCR1+, CCR2+, and CCR3+) is sent to the status-input-request logic. A strobe causes the flip-flop to go to the state of the control-channel input after the status-input request has been acknowledged.



VTII-1914

Figure 5-4. Sync Detection Logic Timing Diagram

Table 5-7. RS232 Signal Locations *(continued)*

LAD Line Number	RS232 Signal	DCM Mnemonic	Pin
1	-	CCO1 +	J1-8
1	-	- 12V	J1-4
1	-	+ 12V	J1-2
1	DB	TSET1 +	J1-15
1	DD	RSET1 +	J1-17
2	AA	PGND2	J2-24
2	BA	TDA2-	J2-31
2	BB	RDS2-	J2-23
2	CA	RTS2 +	J2-27
2	CB	CS2 +	J2-37
2	CC	ILK2 +	J2-33
2	AB	GRD	J2-20,22
2	CF	CO2 +	J2-25
2	CD	DTRY2 +	J2-29
2	CE	RID2 +	J2-35
2	-	CC2 +	J2-21
2	-	CCO2 +	J2-18
2	-	- 12V	J2-36
2	-	+ 12V	J2-40
2	DB	TSET2 +	J2-39
2	DD	RSET2 +	J2-41
3	AA	PGND3	J3-10
3	BA	TDA3-	J3-5
3	BB	RDS3-	J3-9
3	CA	RTS3 +	J3-3
3	CB	CS3 +	J3-19
3	CC	ILK3	J3-11
3	AB	GRD	J3-14,12
3	CF	CO3 +	J3-7
3	CD	DTRY3 +	J3-1
3	CE	RID3 +	J3-13
3	-	CL3 +	J3-6
3	-	CCO3 +	J3-8
3	-	- 12V	J3-4
3	-	+ 12V	J3-2
3	DB	TSET3 +	J2-15
3	DD	RSET3 +	J2-17

The LAD also has two general-purpose lines that can be used to indicate that the reverse channel is on (" input control line") and to turn on the reverse channel (" output control line"). Note that the LAD does *not* provide data communications capability over the reverse channel.

These general-purpose lines can also be used for input and output speed selection (RS232C circuits CH- and CI-).

The interface provides + 12V dc and - 12V dc through 1K resistors that can be used to hardwire certain leads on for testing or for non-standard datasets. Thus, to use this LAD without a dataset (direct connection): tie CB-, CC-, and CF- to VS- and connect the receive-and-transmit clock DB, DD (external source).

5.2.8 Strobe Logic

There are four strobes to transfer data to the LAD:

A	B	Mnemonic	Description
0	0	TDS-	Transfer data to the transmitter
0	1	CST-	Control strobe (loads control register)
1	0	TSS-	Load transmit sync-character register
1	1	RSS-	Load receive sync-character register

Parity-error detection test: Set up the LAD for 8 bit data - no parity - parity mode odd for this test (standard configuration). This test is performed on one line at at a time. Run test 14 continuously and momentarily ground the serial-data output pin. This should cause a parity error that will be reported by the test program.

Overrun-error reporting test: Verify that each line can report an overrun condition by running test 5.

Status-input request test: Verify that each line will make a status input request if a change-of-state of the control-line-in, a ring indication, or an underflow condition (output buffer and register empty) is detected. Test 5 checks all of these.

Modem status lines: Use test 6 to verify that the three modem status lines can be read (interlock, carrier-on, and clear-to-send). Ensure that the clear-to-send status-bit is set if the line is put in transmission mode and reset if the line is not. The interlock status-bit and the carrier-on status-bit should be under control of the data-terminal-ready bit in the line-control byte.

Synchronization test: Verify that each line can obtain synchronization with any valid synchronization character. Test 11 accomplishes this by sequentially transmitting a group of sync-characters that tests all bits. (Test 11 will fail on a line set for five-bit data with odd parity and should be deleted for that configuration.)

Resynchronization test: Verify that each line can be resynchronized in the middle of a message by loading the line receive-sync-character register with a new sync-character. Test 12 accomplishes this.

Transmission sync test: Verify that each line can transmit any bit pattern from its transmit-sync-character register by running test number 13.

Auto parity test: Verify that each line set up for 8-bit data and no parity can be switched under software control to 7-bit data plus parity. Test 14 verifies this.

Burn-in test: Run test 77 for at least 2 passes. (Bypass this test for lines not set up for 8-bit data and no parity.)

5.3.2 Other Problems

To eliminate problems not solved by the above tests, use the program below:

Line Setup

```
        000240  000000
        000241  006050  STAI    Save A
        000242  000000
        000243  010320  LDA     Load A with Control Word
*       000244  103170  OAR     Output to DCM
        000245  006010  LDAI
        000246  000001
        000247  001010  JAZ
        000250  000300
        000251  006010  LDAI
        000252  017504
        000253  050243  STA
        000254  005001  TZA
        000255  050246  STA
        000256  001000  JMP
        000257  000203

        000300  006010  LDAI
        000301  010320
        000302  050243  STA
        000303  006010  LDAI
        000304  000001
        000305  050246  STA
        000306  010242  LDA     Restore A
        000307  100270  EXC     Enable Interrupts
        000310  001000  JMP
        000311  100240          Return
**      000320  113300          Receive Synchronous Character
                                Word

        000650  113226          Synchronous characters
```

* Change to reflect correct Device Address

** Change to reflect correct Synchronous Character and line number.

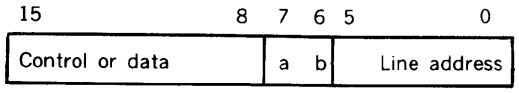
5.4.2 Programming Sequences

This section describes the line-setup and status-reading control sequences used with the synchronous RS232 modem LAD. General DCM programming sequences are given in section 2.4.4.

5.4.2.1 Line Setup Sequence

This sequence begins with an EXC 0570 instruction. The DCM generates a control interrupt as soon as it is free. The program responds with OAR 070. The DCM loads the specified line and resumes scanning.

The character output by OAR 070 has the format:



where a and b indicate the contents of the more-significant byte as follows:

ab	Selected byte
00	Data to output buffer
01	Control
10	Transmitter synchronization character (TSC)
11	Receiver synchronization character (RSC)

DATA BYTE FORMAT (ab = 00): when ab = 00, the more-significant byte contains data. For data characters containing fewer than eight bits, the data are right-justified (bit 8 is the least-significant data bit) and the unused bits are zeros.

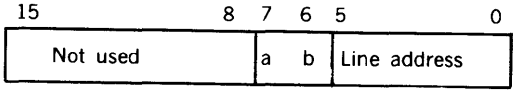
TSC FORMAT (ab = 10): when ab = 10, the more-significant byte contains the TSC that is transmitted by the LAD whenever a line is about to go into an underflow condition to maintain line synchronization. The TSC is right-justified in the control-byte field (unused bits = 0).

RSC FORMAT (ab = 11): when ab = 11, the more-significant byte contains the RSC used to obtain initial line synchronization in receiving mode (the LAD requires at least two consecutive RSCs to obtain line synchronization). If the s bit is set in the line control-byte, every input character that matches the RSC is deleted from the input data stream. The RSC right-justified within the control-byte field (unused bits = 0). To drop synchronization or to resynchronize a line, the program transfers a new RSC to the line.

5.4.2.2 Read Line-Status Sequence

This sequence begins with an EXC 0670 instruction. The DCM generates a control interrupt as soon as it is free. The program responds with OAR 070 and CIA 070.

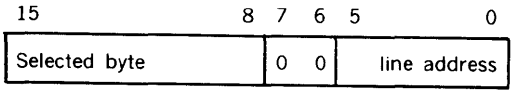
The character output by OAR 070 has the format:



where a and b select one of two possible bytes;

ab	Selected byte
00	Data
01	Line status
10	Not used
11	Not used

The character input by CIA 70 has the format:



DATA BYTE FORMAT (ab = 00): when ab = 00, the selected byte contains data in the same format as in the line-setup sequence (section 5.4.2.1).

LINE-STATUS BYTE FORMAT (ab = 01): when ab = 01, the selected byte contains line-status information in the same format as the status bits in a status-change interrupt (section 5.4.1.2).

5.5 MNEMONICS

Mnemonic	Description
A–	Decoded with B– to indicate the type of information being transferred to the LAD
A1–	Decoded with B1– by software to determine the type of line error
ARx +	Accept-ring/stop output bits from the control registers
ARM +	Multiplexed term of the four accept-ring/stop output bits
B–	See A–
B1–	See A1–
Cx–	Control channel from the control registers
CCHx–	Control channel inputs from the modem (can be used for reverse channel)
CCM +	Control channel change request multiplexed
CCRx–	Control channel change request
CLK–	614,400 Hz clock from MU
COx +	Carrier-on from modems
CSx +	Clear-to-send from modems
CST–	Control strobe
CSTx–	Control strobes to individual control registers
DSx +	Delete sync bits from control registers
DTRx–	Data-terminal-ready bits from control registers
EDTA–	Enable-data onto MUX bus
EOB–	Enable output to MUX bus
Ix +	Enable interrupt-on-underflow bit from control registers
IDR–	Input data request to the multiplexor
IDRx–	Line input-data requests
IDRS +	Input-data request synchronized with CLK–
IDRSD +	Input-data request into the service request register
ILKx +	Interlock or data-set-ready from modem
IM +	Multiplexed term of the four interrupt bits
LADA–	LAD address
LADAE–	Enable LAD address
LAE1– LAE2– LAE3–	Enable LADs
LERR–	Line error signal to the multiplexor
LERRS–	Line error synchronized with CLK–

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