PRIORITY INTERRUPT MODULE

an option for the

Varian Data Machines

Computer Systems

Specifications Subject to Change Without Notice

varian data machines/a varian subsidiary

98 A 9902 424

JANUARY 1973

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SECTION 1
GENERAL DESCRIPTION

The **Priority Interrupt Module** is an I/O option available with Varian 73 and 620 computer systems. This manual is divided into six sections:

- Features and specifications
- Installation and interconnection
- Operation
- Theory of Operation
- Maintenance
- Mnemonics list

Volume 2 of this manual is assembled when the hardware is shipped, and contains engineering documents such as logic diagrams, parts list, and, installation drawings.

The priority interrupt module (PIM) provides for the orderly servicing of peripheral-initiated interrupts of a program in progress. It does so by:

a. Establishing up to eight levels of interrupt priority for selected peripheral controllers.

b. Storing interrupt requests originated by associated peripheral controllers and placing the requests on the I/O bus in the order of the established priority.

In effect, the PIM organizes a "priority-within-a-priority" system. Peripheral controllers that cannot normally initiate an interrupt because of their inability to generate memory addresses can do so when connected to the PIM. PIM-controlled priority assignments are prewired at the factory to user specifications.

Table 1-1 lists the PIM specifications.

Table 1-1. PIM Specifications

Parameter	Description
Organization	Contains line, synchronization, and mask registers; an interrupt address generator; priority and control logic; and line drivers and receivers
Control Capability	Establishes and implements eight levels of interrupt priority (user-assigned) for system peripheral controllers.
I/O Capability	Five external control and three transfer instructions
Standard Device Address	040 through 043
Interrupt Addresses	First PIM: 0100 through 0117 Second and succeeding PIMs: 0120 through 0177
System Priority Assignment	Determined by location in the system priority chain (user-selected)
Logic levels (internal)	High = +2.4 to +5.0V dc Low = 0 to +0.4V dc
Logic levels (I/O bus)	High = +2.8 to +3.6V dc Low = 0 to +0.5V dc
Size	Contained on one 7-3/4-by-12-inch (19.7 x 30.3 cm) printed-circuit board.
Power	5V dc at 0.45A
Operating Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

SECTION 2
INSTALLATION

2.1 INSPECTION

The PIM has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. If damage exists:

a. Notify the transportation company.

b. Notify Varian Data Machines.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The PIM circuits are contained on a single printed-circuit (PC) board (p/n 44P0172). As illustrated in figure 2-1, the board contains three connectors P1, J1, and J2. Connectors J1 and J2 each contain eight interrupt lines (IL00– through IL07–) that can be connected to selected peripheral controllers. Connector P1 also contains the same eight interrupt lines as well as all I/O bus control signals for the PIM.

2.3 PIM INTERRUPT LINES

The PIM has eight interrupt lines that enable up to eight peripheral controllers to be connected in the desired order of priority. The interrupt lines are designated IL00– through IL07–, where IL00– has the highest priority and IL07– the lowest. For controllers that are installed in the same chassis as the PIM, the interrupt lines are connected at the computer backplane connector that mates with P1 of the PIM board. For controllers in a different chassis, the interrupt lines are contained in either an I/O expansion cable that connects to P1 of the PIM (via computer backplane) or in an interrupt cable that connects to J1 or J2 of the PIM. Pin assignments for the interrupt lines are listed in table 2-1.

Interrupt Lines	P1	J1	J2	Interrupt Lines	P1	J1	J2
IL00–	108	3	3	IL04–	102	11	11
IL01–	114	13	13	IL05–	88	5	5
IL02–	104	9	9	IL06–	112	1	1
IL03–	110	15	15	IL07–	86	7	7

2.4 DEVICE ADDRESS ASSIGNMENT

The device address for each PIM is implemented with jumper wires installed on the computer backplane connector that mates with P1 of the PIM board. Device addresses 040 through 044 are reserved for PIM. Normally 040 is assigned to the first PIM, 041 to the second, 042 to the third, etc. Figure 2-2 shows the required connections for address 042.

2.5 INTERCONNECTION

In the Varian 73 system, the PIM can be installed in the mainframe using either a single controller adapter or a dual controller adapter. The PIM can also be installed in a designated slot of an I/O expansion chassis. Refer to the Varian 73 System Handbook (document number 98 A 9906 010) for further installation information.

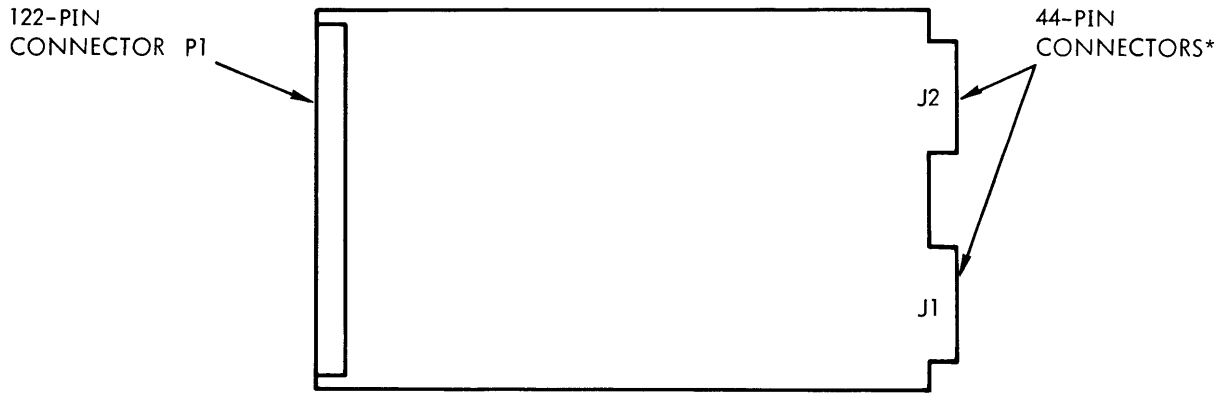

Figure 2-1. PIM Board (Component Side)

INSTALLATION

The PIM can be installed in designated slots of the mainframe and expansion chassis for 620/L systems, and in designated slots of the memory and I/O expansion chassis for 620/f-100 systems. Further installation information for these computer systems, can be found in the 620/L Maintenance Manual (document number 98 A 9905 155) and the 620/f-100 Maintenance Manual (document number 98 A 9908 150).

The pin assignments for the connectors on the PIM board are provided in logic diagram 91D0016 (volume 2).

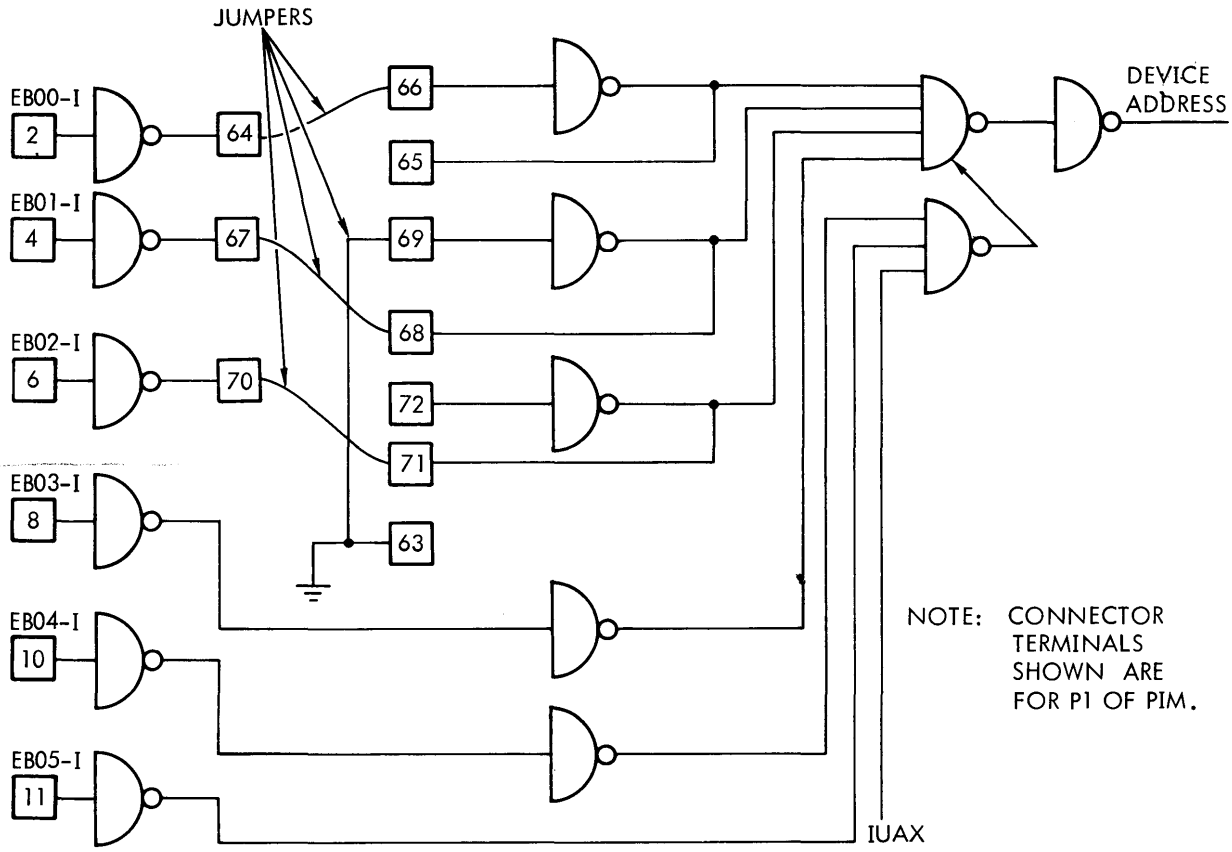

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Figure 2-2. Jumper Connections for Device Address 042

SECTION 3
OPERATION

The PIM has no operating controls or indicators. It operates under program control.

3.1 I/O INSTRUCTIONS

The PIM responds to the five external control and three data transfer commands listed in table 3-1.

loops. Two NOP instructions are required after an external control (EXC) instruction.

For computer systems containing the memory protection (MP) option in addition to the PIM, the MP is disabled everytime an interrupt is serviced. Therefore at the end of the PIM service program, the MP must be enabled again.

Table 3-1. I/O Instructions

Mnemonic	Program Code	Functional Description
External Control		
EXC 014X*	10014X*	Clear interrupt registers.
EXC 024X	10024X	Enable PIM.
EXC 0244	100244	Enable all PIMs in a system.
EXC 034X	10034X	Clear interrupt registers and enable PIM.
EXC 044X	10044X	Disable PIM.
EXC 0444	100444	Disable all PIMs in a system.
EXC 054X	10054X	Clear interrupt registers and disable PIM.
Data Transfer		
OME 04X	10304X	Transfer memory to mask register.
OAR 04X	10314X	Transfer A register contents to mask register.
OBR 04X	10324X	Transfer B register content to mask register.

* X represents the last octal digit of the device address.

3.2 PROGRAMMING CONSIDERATIONS

When preparing a PIM program, clear the interrupt registers to establish initial conditions. To mask peripheral controllers, write a mask word in the program. The eight least significant bits of the mask work correspond to the eight priority interrupt lines. Setting bit 0 inhibits the highest priority line, setting bit 1 inhibits the second-highest priority line, etc. The mask register must be loaded by the program after any power-up sequence, including the power-up cycle of the power failure/restart (PF/R) feature. System reset does not clear the PIM mask register.

When program loops contain only uninterruptable instructions, interrupts cannot occur. Thus, when recognition of an interrupt is imperative (such as with the PF/R), at least one No-Operation (NOP) instruction must be added to such

3.3 UNINTERRUPTABLE INSTRUCTIONS AND CONDITIONS

An interrupt can only be detected during the last cycle of an instruction execution. In Varian 73 and 620/f-100 systems using the memory protection feature, interrupts can be detected immediately following all instructions except:

a. Halt (HLT) instructions

b. Any external control (EXC) I/O instruction

c. Any execution instruction. If the condition is met, interrupts are inhibited between executions of an execution instruction and the instruction at the execution address. If the condition is not met,

interrupts are inhibited between executions of an execution instruction and the instruction following in sequence.

d. Any instruction executed in the step mode.

In Varian 73 and 620/f-100 systems without the memory protection feature, detection of an interrupt is inhibited during the following types of instructions:

a. Halt (HLT) instructions

b. All shift instructions

c. All I/O instructions

d. All double-word instructions

e. All multiplication or division instructions

f. Any instruction executed in the step mode

In all 620/L systems, detection of an interrupt is inhibited during the following types of instructions and conditions:

a. Halt (HLT) instructions

b. All jump, jump and mark, or execution instructions when the jump condition is met. (When the jump condition is not met these instructions are interruptable).

c. All I/O instructions

d. All shift or rotation instructions

e. All multiplication or division instructions

f. During the processor cycle immediately following an external control (EXC) I/O instruction.

g. During the processor cycle immediately following a shift, rotation, multiplication, or division instruction during which a trap occurred (DMA operation).

h. During the first instruction executed after entering run mode if that instruction is a single-word instruction.

i. During a manual step operation

j. During a halt condition

3.4 PROGRAM EXAMPLE

Table 3-2 shows a typical program using the PIM. In this program, 256 descending binary frames are transferred to the high-speed paper tape punch. Memory locations 01000 to 01023 are used in the program as are computer mnemonic codes with corresponding machine language codes.

Table 3-2. Program Example

Machine Code		Source Code			
Location	**Instruction**	**Label**	**Mnemonic**	**Operand**	**Description**
001000		STRT	,ORG	,01000	
001000	011011		,LDA	,MASK	FETCH INTERRUPT MASK
001001	103140		,OAR	,040	AND STORE IN REGISTER
001002	006010		,LDAI	,0377	INITIALIZE OUTPUT DATA
001003	000377				
001004	103137		,OAR	,037	PRIME INTERRUPT MODULE
001005	100240		,EXC	,0240	ENABLE PIM
001006	005000		,NOP	,	
001007	001000		,JMP	,*-1	DELAY FOR INTERRUPTS
001010	001006				
001011	000376	MASK	,DATA	,0376	
*		INTERRUPT	PROCESSING	SUBR	
001012	000000	INTR	,ENTR	,	
001013	005311		,DAR	,	DECR OUTPUT DATA
001014	103137		,OAR	,037	OUTPUT DATA TO PUNCH
001015	100240		,EXC	,0240	RE-ENABLE PIM
001016	001010		,JAZ	,*+4	
001017	001022				
001020	001000		,JMP*	,INTR	EXIT
001021	101012				
001022	100440		,EXC	,0440	CLEAR PIM
001023	000000		,HLT	,	END OF PROGRAM
		INTERRUPT	ADDRESS		
000100			,ORG	,0100	
000100	002000		,JMPM	,INTR	
000101	001012				
	000000		,END	,	

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

Communication between the PIM and the processor is similar to that of any peripheral controller except that the PIM can request a program interrupt. When the computer acknowledges the interrupt, the PIM specifies the memory location of the instruction to be executed.

The PIM scans the interrupt lines with every cycle of the interrupt clock (IUCX-I). If signals are detected on more than one line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored in the PIM interrupt-line register until acknowledged. The PIM has an 8-bit mask register that selectively inhibits interrupt requests from the interrupt-line register. When a given flip-flop of the mask register is set, corresponding interrupt requests from the interrupt-line register are inhibited. When the mask register flip-flop is reset, the interrupt request is not inhibited. The mask register is unaffected by system reset and must be loaded under program control using data-transfer instructions.

Acknowledgment of an interrupt by the processor causes execution of the instruction located at the memory address specified by the PIM. Any instruction can be executed except an I/O type. An interrupt is thus serviced in one instruction period.

4.2 FUNCTIONAL DESCRIPTION

The following subsections describe the five functional circuits of the PIM (figure 4-1). Refer to the timing

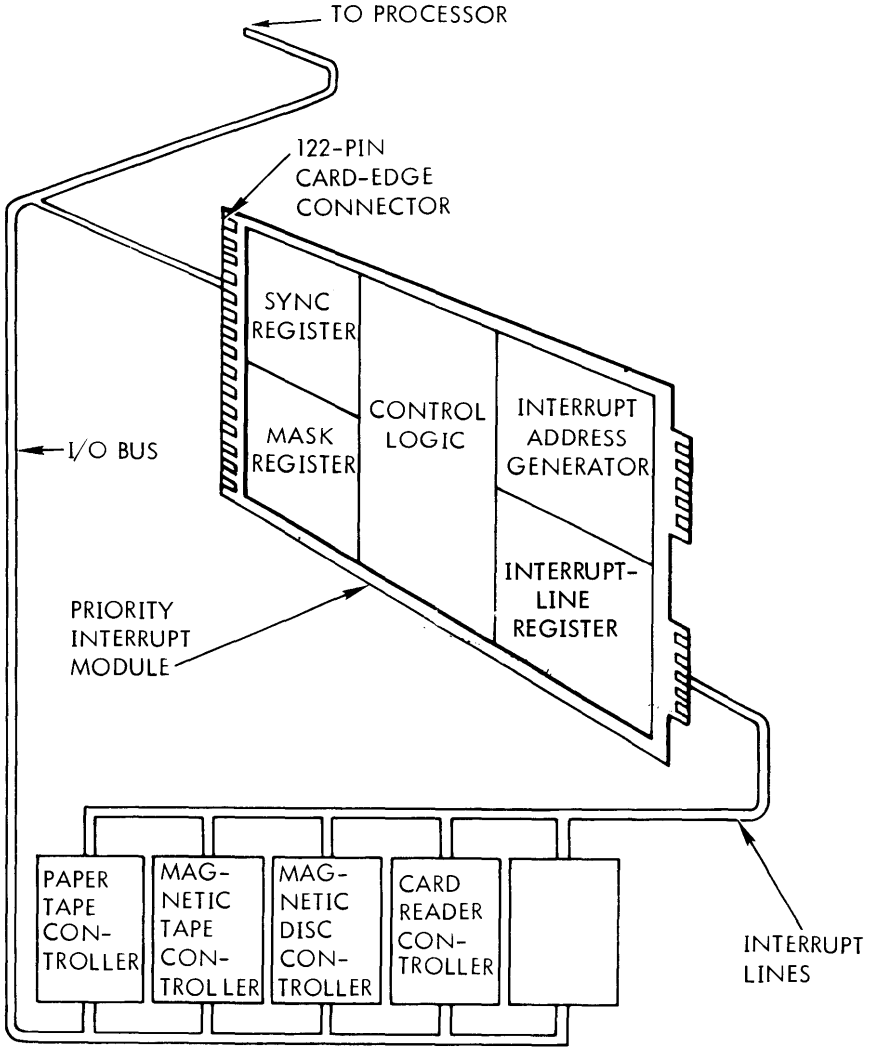

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Figure 4-1. PIM Functional Block Diagram

waveforms of figure 4-2 and the PIM logic diagram 91D0016 in volume 2. Three-digit numbers in parentheses indicate the location of circuit elements on the logic diagram. The first number locates the sheet; the following letter and number indicate the area on that sheet. For locating large areas, X and i stand for the locating letter and number respectively. For ease of reading some mnemonics are written with the variable n in place of the actual bit numbers.

4.2.1 Control Logic

The control logic circuit directs and sequences the response of the PIM to external control, data transfer, and interrupt operations. When a computer program interrupt is requested, the processor requests the PIM to place the interrupt address on the I/O bus. If the PIM has system priority, the address line drivers are enabled. The PIM interrupt-request signal will remain active until all interrupts stored (but not inhibited) by the PIM have been acknowledged, or until PIM priority is lost.

The control logic circuit consists of flip-flops PRME, DTOX, IURM and associated gates. During the execution of an output data transfer command, signals FRYX (1B8) and DA (1D5) set flip-flop DTOX (1B4). FF set signal DTOX + high and pulse signal DRYX + generate signal SMR1− low (1B3) which causes the mask word to be transferred from the I/O bus to the mask register (2Di). At the end of the transfer, signal DRYX + resets flip-flop DTOX. Signal DA (1D5) in conjunction with signal FRYX + indicates that the central processor is communicating with the PIM.

External control commands for the PIM are indicated by signal EXCX + low (1B6). Signals EB06 +, EB07 +, and EB08 + (1C8) are combined with signal EXCX + to actuate the five external control commands.

Flip-flop PRME (1C4) provides master enable/disable for the entire PIM. When flip-flop PRME is reset, computer program interrupts cannot be requested by the PIM; however, the PIM continues to receive and store interrupts from external devices. When FF set signal PRME + is high, flip-flop IURM (1C3) is set by signal INR1 + high (2C2) one IUCX-I clock period after an interrupt is clocked into the sync register. FF set signals IURM + and PRME + high with signal PRMX-I low (1A8) generate signal IURX-I low (1A1), requesting an interrupt.

When a computer program interrupt is requested by the PIM, the processor responds with signal IUAX-I low (1B8). This signal requests that PIM place the interrupt instruction address on the I/O bus.

If the PIM has system priority, the address line drivers (1C1) are enabled as long as signal IUAX-I is low. When signal IUAX-I goes low, signal IUCX-I (1B8) is held low. Interrupt conditions are therefore held static during the time that signal IUAX-I is low. Flip-flop IURM is cleared when all interrupts received by the PIM have been acknowledged by the central processor.

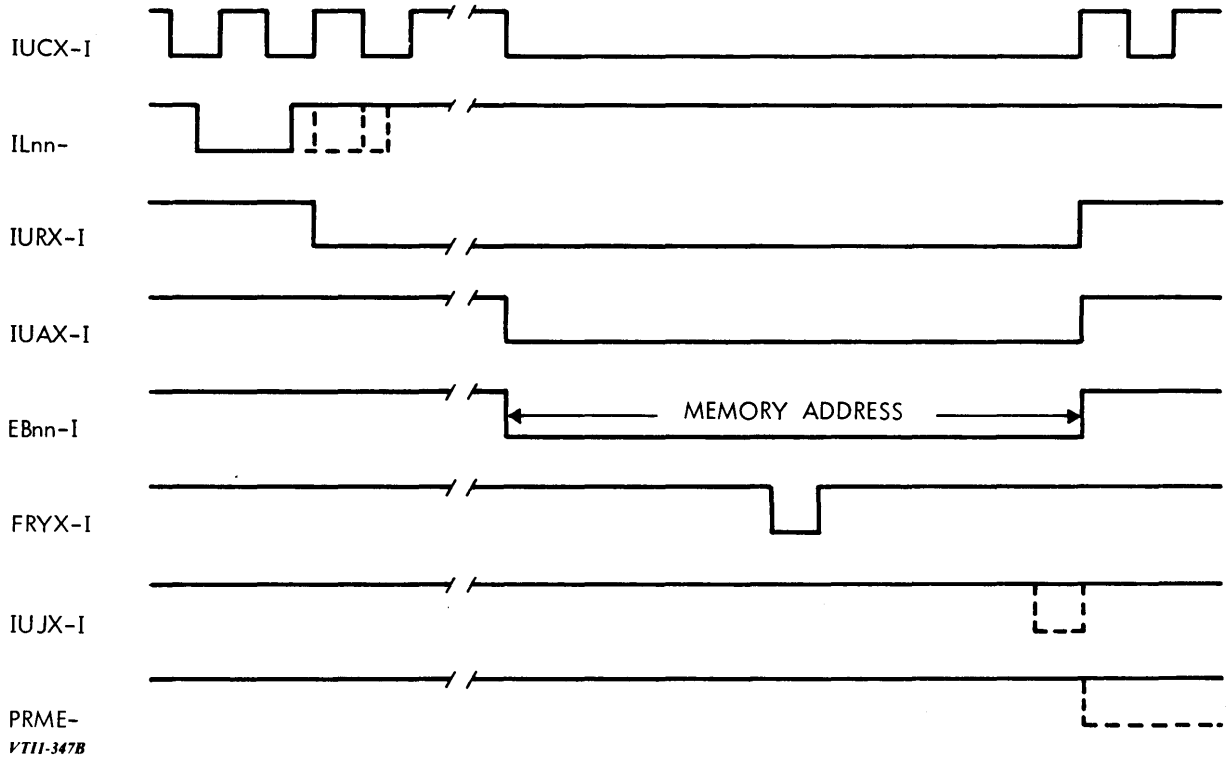


Figure 4-2. Timing for Reception and Servicing of a Single Interrupt

4.2.2 Interrupt Address Generator

The interrupt address generator consists of coding logic that generates the binary number of the interrupt line requesting the interrupt. A pair of memory locations is reserved for each interrupt line. The interrupt addresses are normally in memory locations 0100 through 0117. However, the 16 interrupt addresses can be placed anywhere within the first 128 memory locations except 040 through 047 and may be placed at other addresses by special request.

The interrupt address generator consists of three gates (1D4) which use line priority signals to generate signals A0XX+, A1XX+, and A2XX+. These signals consititute three bits of the address code for the interrupt line to be serviced. They are placed on the I/O bus by signal IAEX+ low. The least significant bit of the address code is always low, resulting in an even address. This bit is supplied by the processor when the second word of a double-word interrupt instruction is accessed.

Signal IAEX+ low is generated by signals PRMX-I and IUAX-I low and FF set signal PRME+ and IURM+ high. These four signals indicate, respectively, that: the PIM has priority; the PIM interrupt has been acknowledged; the PIM is activated; and interrupt awaits on one of the interrupt lines.

4.2.3 Interrupt-Line Register

The interrupt-line register consists of eight flip-flops that asynchronously accept interrupt inputs. An interrupt is stored in the register until the interrupt is serviced or until the entire register is cleared by command.

The interrupt-line register consists of flip-flops LR00 through LR07 (2Ai). An interrupt is generated when an interrupt line signal, ILnn−, goes low. Signals IL00− through IL07− (2Ai) are each connected to the clock input of an interrupt-line register flip-flop. Signal ILnn− may remain low for any period of time greater than 0.2 microseconds; a constantly low signal does not produce repetitive interrupts. If the interrupt is serviced, the flip-flop is reset by signal IUCP+ (2B8) and a line priority signal, LPnn+. Although signal IUCP+ is sent to all register flip-flops, only the flip-flop that was serviced is reset.

4.2.4 Sync Register and Line Priority

The sync register consists of eight flip-flops. At each interrupt clock period, the outputs of the interrupt-line register are clocked into the sync register. The sync register, therefore, samples the status of the eight interrupt lines synchronously with the computer interrupt clock. The sync register outputs activate the priority logic used to generate the interrupt address.

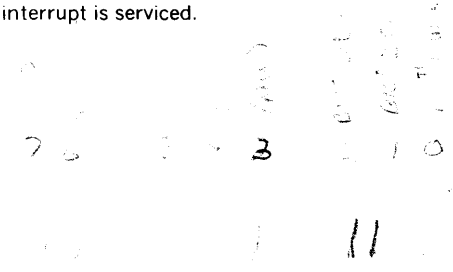
If two or more interrupts occur simultaneously, the line with the highest priority is given precedence and all other lines are temporarily inhibited. An interrupt line may request a computer program interrupt only if the line has not been inhibited and a higher-priority line is not active.

The sync register consists of flip-flops IR00 through IR07 (2Bi). Signal IUC1− clocks the contents of the interrupt-line register into the sync register. The outputs of the sync register are fed into a network of gates that determine the priority of each interrupt line signal. The line priority circuit generates signal INR1+ (2C2) which enables the generation of signal IURX-1. In addition, signals LP00+ through LP07+ determine the interrupt address and the interrupt-line register flip-flop to be reset after servicing its interrupt. Signal IL00− has the highest priority, and signal IL07− has the lowest priority.

4.2.5 Mask Register

The mask register inhibits interrupt requests from selected interrupt lines to be disarmed while other lines are permitted to cause a program interrupt. The eight flip-flops of the mask register inhibit corresponding interrupt requests from the interrupt-line register. The mask register must be loaded under program control to establish which interrupts are to be inhibited.

Signals EB00+ through EB07+ are loaded into the mask register (2Di) when a particular interrupt is to be masked (inhibited). Signal SMR1+ clocks this mask word into the register at the time. The register outputs are fed into the line priority circuit. If one or more interrupts are inhibited by the mask register, the highest-priority unmasked interrupt is serviced.



SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting PIM troubleshooting. The Varian MAINTAIN II test program system (Test Programs Manual, 98 A 9952 060) contains a PIM test program used to test various phases of PIM operation. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommeded for maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 39-watt pencil type.

d. Card extender VDM p/n 44P0540

5.2 CIRCUIT-COMPONENT IDENTIFICATION

All reference designations used in the logic diagram appear on the PIM board adjacent to each component. Component part numbers can be found in the parts list in volume 2.

5.3 CIRCUIT-BOARD REPAIR

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

SECTION 6
MNEMONICS

Table 6-1 provides an alphabetized list of the signal mnemonics used in the PIM.

Table 6-1. Mnemonics

Mnemonics	Description
AnXX	Address code of device with priority interrupt.
CACR	Clear ac register. Generates signal CILR on receipt of signal EXCX.
CILR	Clear line register. Clears the line and sync registers.
DA	Decoded device address.
DRYX	Data ready pulse that resets flip-flop DTOX; enables signal SMR1.
DTOX	Data transfer out flip-flop. Stores the occurrence of an output command from the processor.
EBnn-I	Address or function code bit from I/O bus.
EXCX	Enables initialization of PIM upon external control command.
FRYX	Function ready pulse that sets flip-flop DTOX.
IAEX	Interrupt address enable. Gates address of interrupt line onto I/O bus.
ILnn	Interrupt line from peripheral controller.
INRn	Interrupt request. Indicates a request from one or more interrupt lines.
IRnn	Sync register outputs. Stores the status of the line register in synchronism with the interrupt clock signal.
IUAX	Interrupt acknowledgment. Enables servicing of PIM interrupts.
IUCP	Interrupt completion resets line register flip-flop after interrupt is serviced.
IUCX	Interrupt clock. Provides timing for servicing of PIM interrupt request.
IUCI	Interrupt clock inverted. Clocks contents of line register into sync register.
IUDX	Interrupt detection. Sets flip-flop IURM.
IUJX	Interrupt jump. Inhibits the PIM after a jump and mark command.
IURM	Interrupt request memory flip-flop. Stores a request for an interrupt from an interrupt line.
IURX-I	Interrupt request. Sent to the processor to request signal IUAX-I.
LPii	Line priority signals. Indicates the eight PIM priorities.
LRnn	Line register flip-flop outputs. Stores request for an interrupt from a device connected to an interrupt line.
PRME	PIM enabling flip-flop. Stores the activation of the PIM.
PRMX	Priority input. Gives priority to PIM.
PRNX	Priority output. Passes priority to next in line after interrupts are serviced.
SMR1	Clocks mask word into mask register.
SYRT	System reset. Clears flip-flops DTOX and PRME and generates signal CILR when control-panel reset switch is pressed.

NOTES

NOTES

EVALUATION QUESTIONNAIRE

TITLE _____

MANUAL NUMBER _____

The purpose of this questionnaire is to provide suggestions about how the manual can be improved when it is revised. It is the goal of the Technical Publications Department to make each manual as useful as possible and at the same time eliminate material that is of no practical value to the user or Customer Service Representative in acquiring initial knowledge of, and in maintaining, the equipment in the field. You, as the person working most closely with the manual and the equipment, can best provide the input needed by the writer to make the best possible manual for your use.

1. Please complete the following chart.

CHAPTER/SECTIONS		MOST USEFUL			NEEDS MORE				NEEDS LESS		
		Field Reference	Training	Big Picture Description	Illustration	Detailed Description	Detailed Description	Detailed Description			

2. Please list any errors, omissions, or difficult areas noticed in the manual. _____

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4. In an overall evaluation of this manual, how do you rate it in the following?

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