VARIAN 70 SERIES

CORE MEMORY MANUAL

Specifications Subject to Change Without Notice

varian data machines /a varian subsidiary
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SECTION 1
GENERAL DESCRIPTION

The **Varian 70 Series Core Memory Manual** describes the memory and its interface with a Varian 70 series computer.

The manual is divided into six sections:

- Introduction to the memory and its relation to the system
- Installation and interface information
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

There is also a Volume 2 to this manual. Volume 2 is assembled when the hardware is shipped, and reflects the configuration of a specific system. It contains engineering documents, such as logic and installation drawings.

The following list contains the part numbers of other manuals pertinent to the Varian 70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9):

Title	Manual Number
System Handbook	98 A 9906 01x
Processor Manual	98 A 9906 02x
Semiconductor Memory Manual	98 A 9906 04x
Option Board Manual	98 A 9906 05x
Power Supply Manual	98 A 9906 06x
Microprogramming Guide	98 A 9906 07x
Writable Control Store Manual	98 A 9906 08x
Memory Map Manual	98 A 9906 10x
Test Programs Manual	98 A 9952 06x
VORTEX II Reference Manual	98 A 9952 24x

This expandable, random-access, three-wire/three-dimensional magnetic-core memory has an internal cycle time of 660 nanoseconds.

The basic memory module has 8,192 (8K) words of 16 or 18 bits each. The core memory is expandable in 8K increments to 65,536 (64K) words. With the memory map option, the memory can be expanded to 262,144 (256K) words.

The standard 16-bit words contains two 8-bit bytes that can, in some systems, be manipulated independently. The optional 18-bit word provides a parity bit for each byte. Unless otherwise specified, further references in this manual are to 16-bit words.

The dual-port memory can have two independent sets of I/O terminals for simultaneous access to different memory modules from different sources, e.g., main and peripheral processors. Port B has a higher access priority than port A. Furthermore, port B can obtain continuous access by locking out port A with a priority-modification signal (MHGY −, section 4). An optional priority-modification signal (MHMY −) can also be used to lock out port B.

In systems containing both a semiconductor memory (Semiconductor Memory Manual, 98 A 9906 04x) and a core memory, the former is normally assigned the lower address area. However, in special applications semiconductor memory can be located above or between core memory areas. By using jumpers (section 2.3), the core and semiconductor memories can be assigned in 8K increments to the desired address areas. These jumpers can also provide for odd/even address interleaving between 8K modules of core memory.

Table 1-1 lists the specifications of the core memory.

Table 1-1. Core-Memory Specifications

Parameter	Specification
Speed (address lines must be stable 12 nanoseconds before leading edge of the start pulse)	Cycle time: 660 nanoseconds maximum Access time: 350 nanoseconds maximum Write data available from 150 (maximum) to 330 (minimum) nanoseconds after the start pulse (see figure 4-4)
Logic levels (CPU bus)	True: -0.4 to +0.8V dc False: +2.4 to +5.oV dc
Address and control lines	Unidirectional
Data lines	Bidirectional
Word length	16-bit word containing two 8-bit bytes (optional 18-bit word has a parity bit for each byte)
Capacity	8,192 (8K) to 65,536 (64K) words in increments of 8K words
Dimensions	Each 8K increment is 15.6 by 19 by 1.1 inches (39.6 by 48.3 by 2.79 cm)
Interconnection	Over very short signal paths to the processor via one 132-pin connector
Priority	Port B has priority over port A to the dual-port memory (a priority-modifier permits complete disabling of port A and an optional priority-modifier disables port B)
Power	8K 16K 32K (Values in amperes) +20.6V dc 1.3 1.4 1.6 +5V dc 2.0 4.0 8.0 -12V dc 7.0 7.4 8.2 The nominal current requirements shown are for memory systems in which only one module is operating at a time (memory not interleaved).
Operating limits	Power-supply voltages ± 5 percent from nominal
Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation
Forced-air cooling	For each 3W dc power, one cubic foot of air per minute applied crosswise above and below each memory module

SECTION 2
INSTALLATION

2.1 INSPECTION

The core memory has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. Ascertain that wires and cables are neither loose nor broken, and that hardware is secure. If damage exists:

a. Notify the transportation company.

b. Notify Varian Data Machines.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

An 8K memory module (figure 2-1) consists of a 15.6 by 19 inch printed-circuit (PC) card (p/n 44P0613) and two 4K stack cards. One side of the PC card has two 130-pin connectors (J1 and J2) to accommodate the two 4K stack cards. The other side of the PC card contains the electronic components of the memory module. In most cases, components of a functional circuit are grouped together. The PC card also has a 132-pin card-edge connector (P1) that connects the memory module to the processor. The height of the memory module is 1.1 inch.

2.3 ADDRESS-JUMPER CONNECTIONS

Each memory module is assigned a module address determined by jumper connections on the PC card. These connections are normally made at the factory. This description is for the information of the user who wishes to expand or change a memory system.

Figure 2-2 illustrates the module-address terminals as they appear on the core memory PC card. The jumpers shown

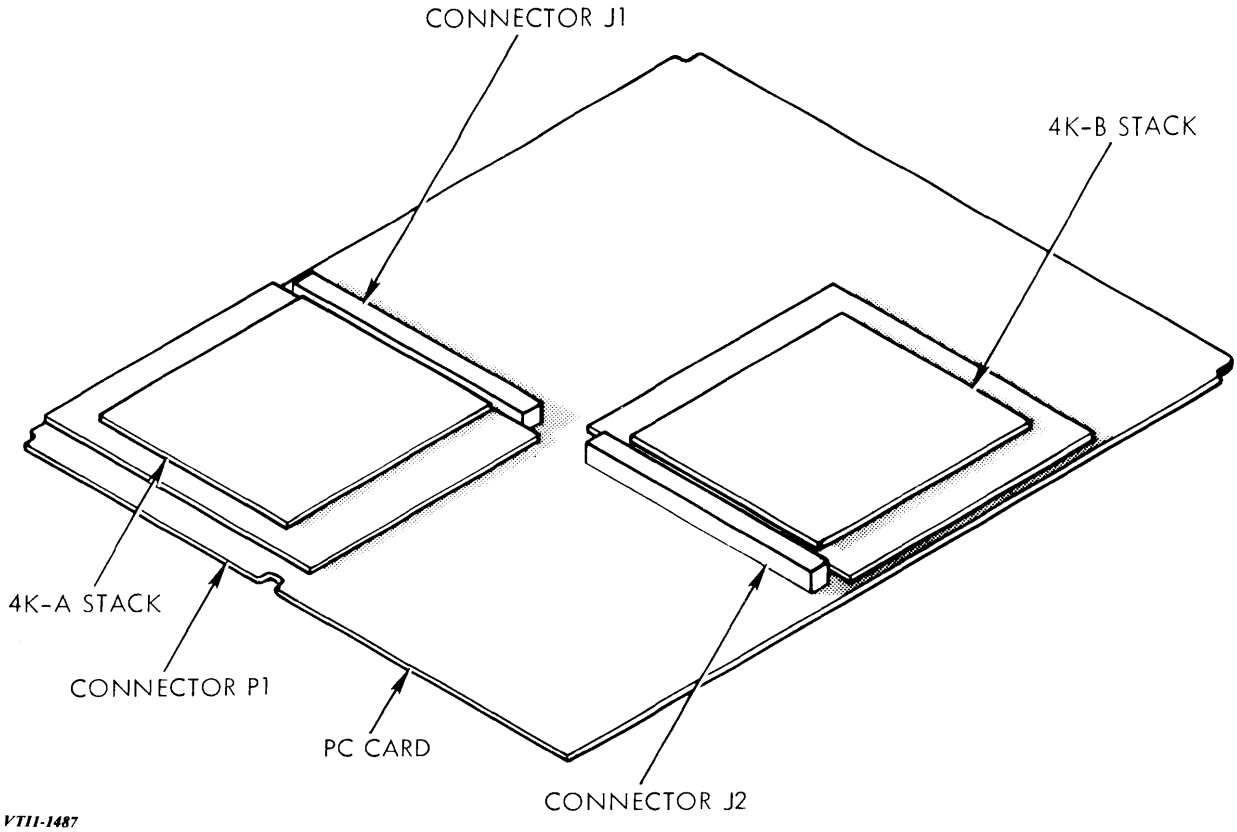
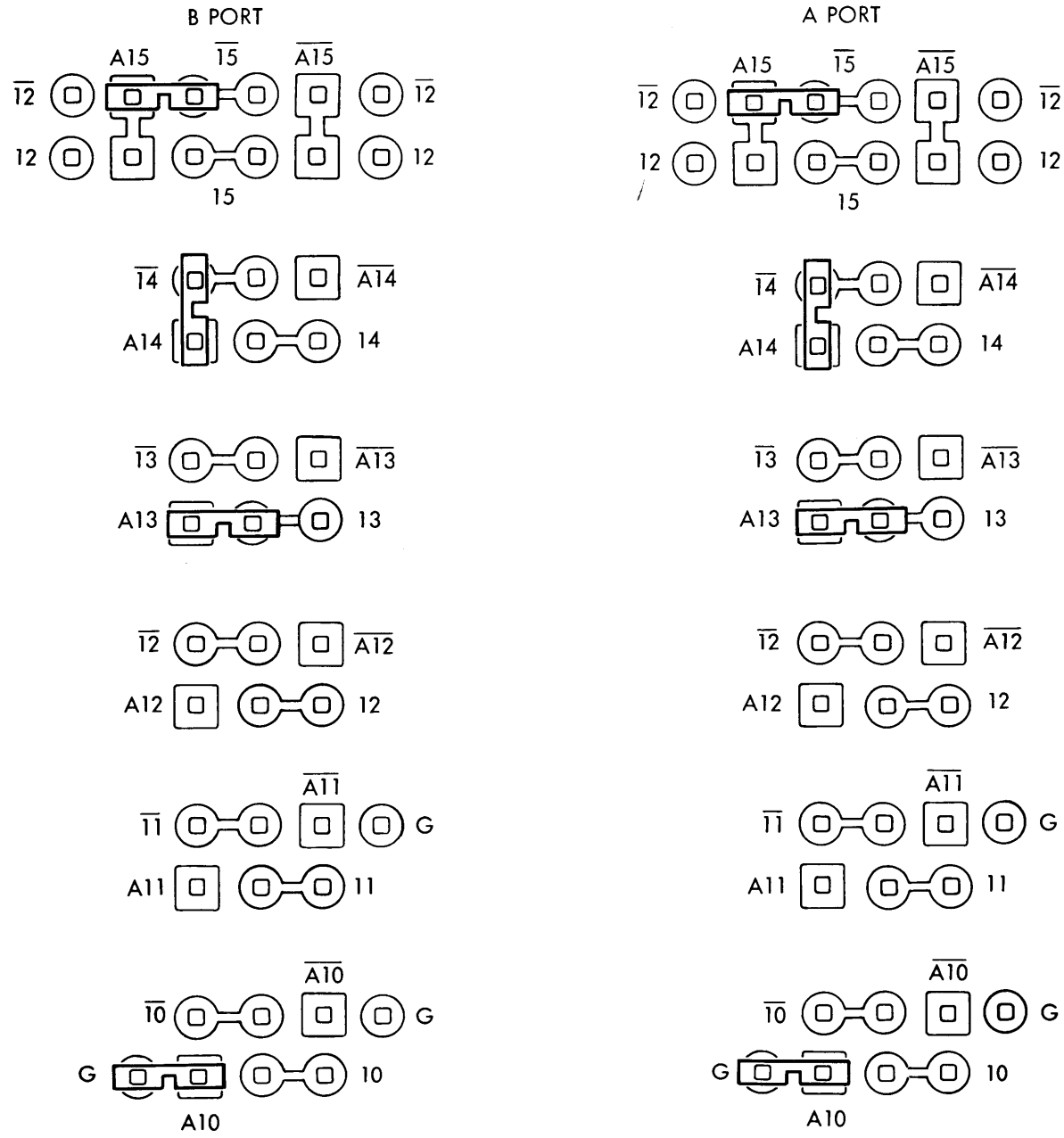


Figure 2-1. 8K Core Memory Module

INSTALLATION



NOTES:

a. THE JUMPER CONNECTIONS SHOWN ARE FOR THE SECOND 8K MEMORY MODULE. THE JUMPER ASSIGNMENTS ARE LISTED UNDER COLUMN HEADING 8-15K IN TABLE 2-1.

b. PINS DESIGNATED WITH CIRCLES ARE ADDRESS BITS FROM THE MEMORY ADDRESS BUS. PINS DESIGNATED WITH SQUARES ARE ADDRESS SEM SELECTION INPUTS (SEE SECTION 4.5.1.)

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Figure 2-2. Typical Address Jumper Configuration

are for the second 8K module. Jumper assignments for the various memory modules are listed in table 2-1. Each vertical column under the memory bank address headings lists the address bits to be connected for a particular memory module. Except in special applications, address jumper assignments for ports A and B are identical.

2.4 INTERFACE DATA

The memory interface circuits consist of transistor-transistor logic (TTL) drivers and receivers (7400 series ICs or equivalent). Figures 2-3, 2-4, and 2-5 are simplified schematics of typical data, address, and control line configurations. The address and control lines are unidirectional and the data lines are bidirectional. Memory-bus drivers sink large currents due to the large number of terminations and gate inputs. The bus structures show the maximum of eight 8K memory modules on-line at a time. For one memory module, the 16 address lines can be decoded for only one port at a time. However, since the ports are independent, two memory modules can run simultaneously on different ports. During the operation of a memory module, no spurious signals are generated on the inactive port.

2.5 MEMORY INTERLEAVING

Memory interleaving is an optional feature that increases the performance of the memory. With memory interleaving, even addresses are located in one 8K module and odd address in another 8K module. This permits instruction-execution cycles to overlap thus decreasing the time required to run a program. Memory interleaving is normally installed at the factory and consists of changing address jumpers on the memory PC card (section 4.5.1).

During interleaving, memory modules are active simultaneously and thus draw more current. To prevent power supply overloading, special power supply and chassis configurations may be required.

Table 2-1. Jumper Assignments for 8K Module

MEMORY MODULE / ADDR INPUT SELECTIONS / ADDR	0-15K EVEN*	0-15K ODD*	16-31K EVEN*	16-31K ODD*	32-47K EVEN*	32-47K ODD*	48-63K EVEN*	48-63K ODD*
	0-7K	8-15K	16-23K	24-31K	32-39K	40-47K	48-55K	56-63K
A10	G	←					→	G
A11					↓			
A12								
A13	$\overline{13}$	13	$\overline{13}$	13	$\overline{13}$	13	$\overline{13}$	13
A14	$\overline{14}$	$\overline{14}$	14	14	$\overline{14}$	$\overline{14}$	14	14
A15	$\overline{15}$	$\overline{15}$	$\overline{15}$	$\overline{15}$	15	15	15	15
$\overline{A10}$	H	←					→	H
$\overline{A11}$								
$\overline{A12}$								
$\overline{A13}$								
$\overline{A14}$								
$\overline{A15}$								

NOTE: H = NO CONNECTION, G = GROUND CONNECTION, BLANK IS IRRELEVANT
* = INTERLEAVING ADDRESSES

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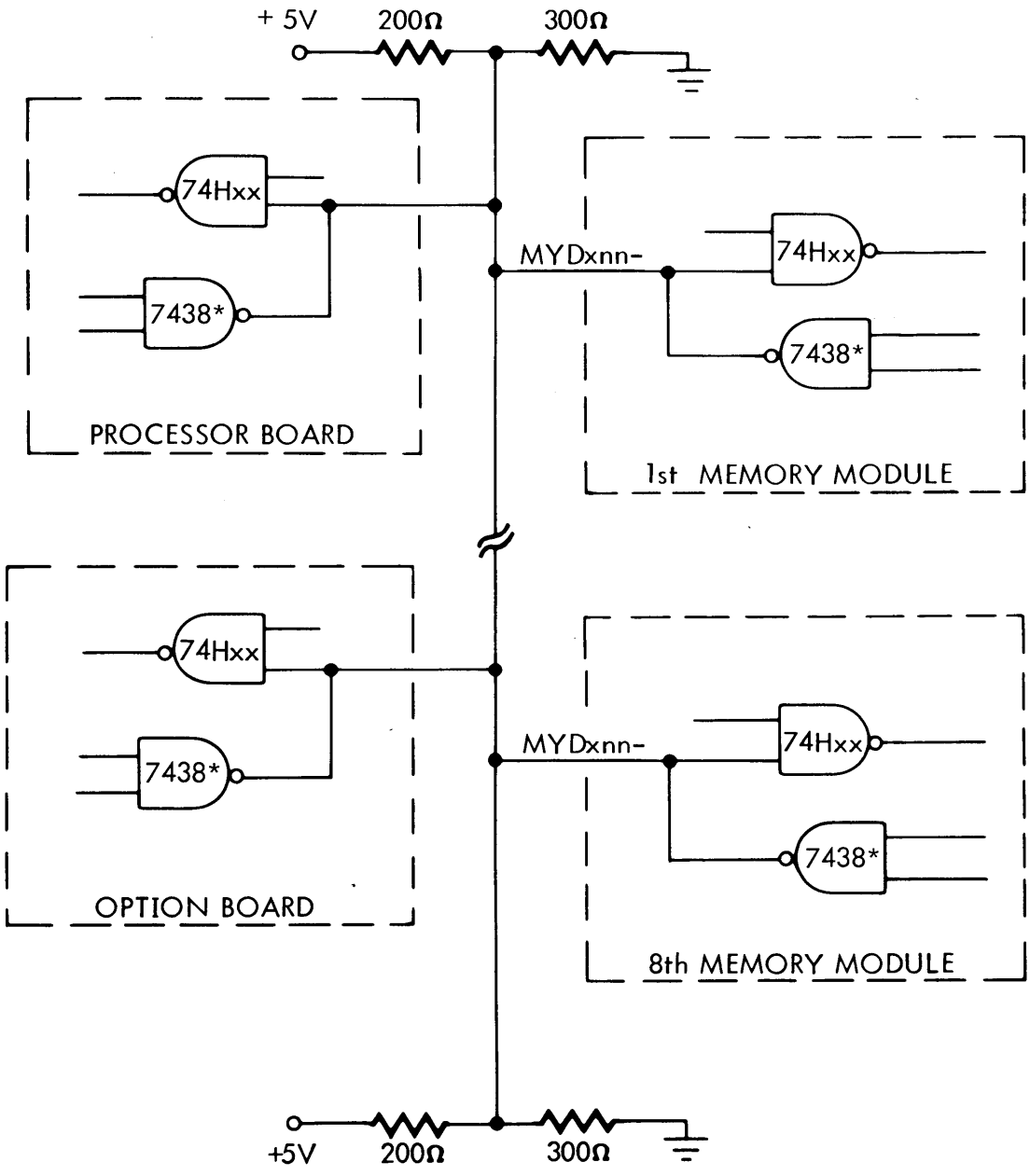
INSTALLATION



*THE 7438s ARE SELECTED

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Figure 2-3. Typical Data Bus Configuration

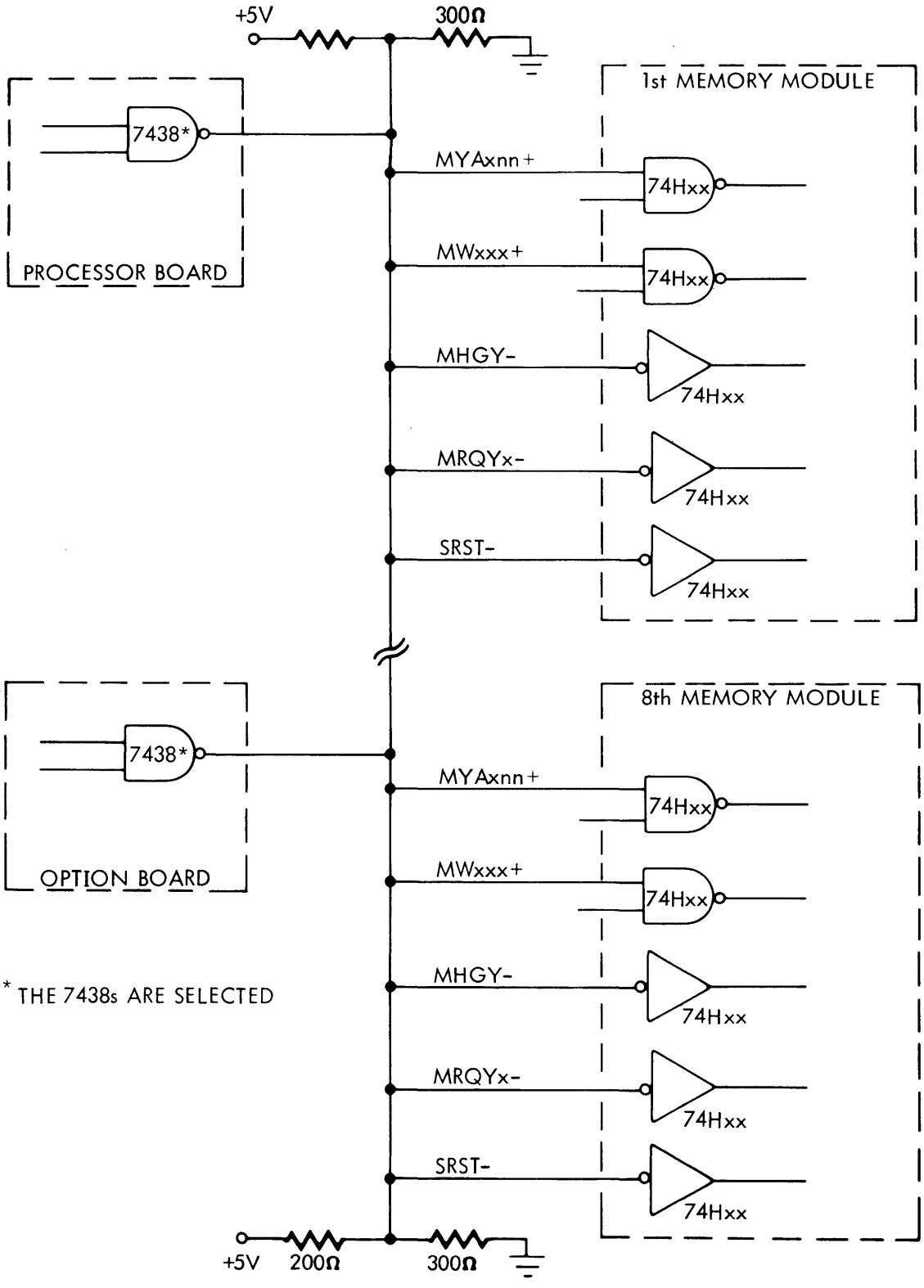

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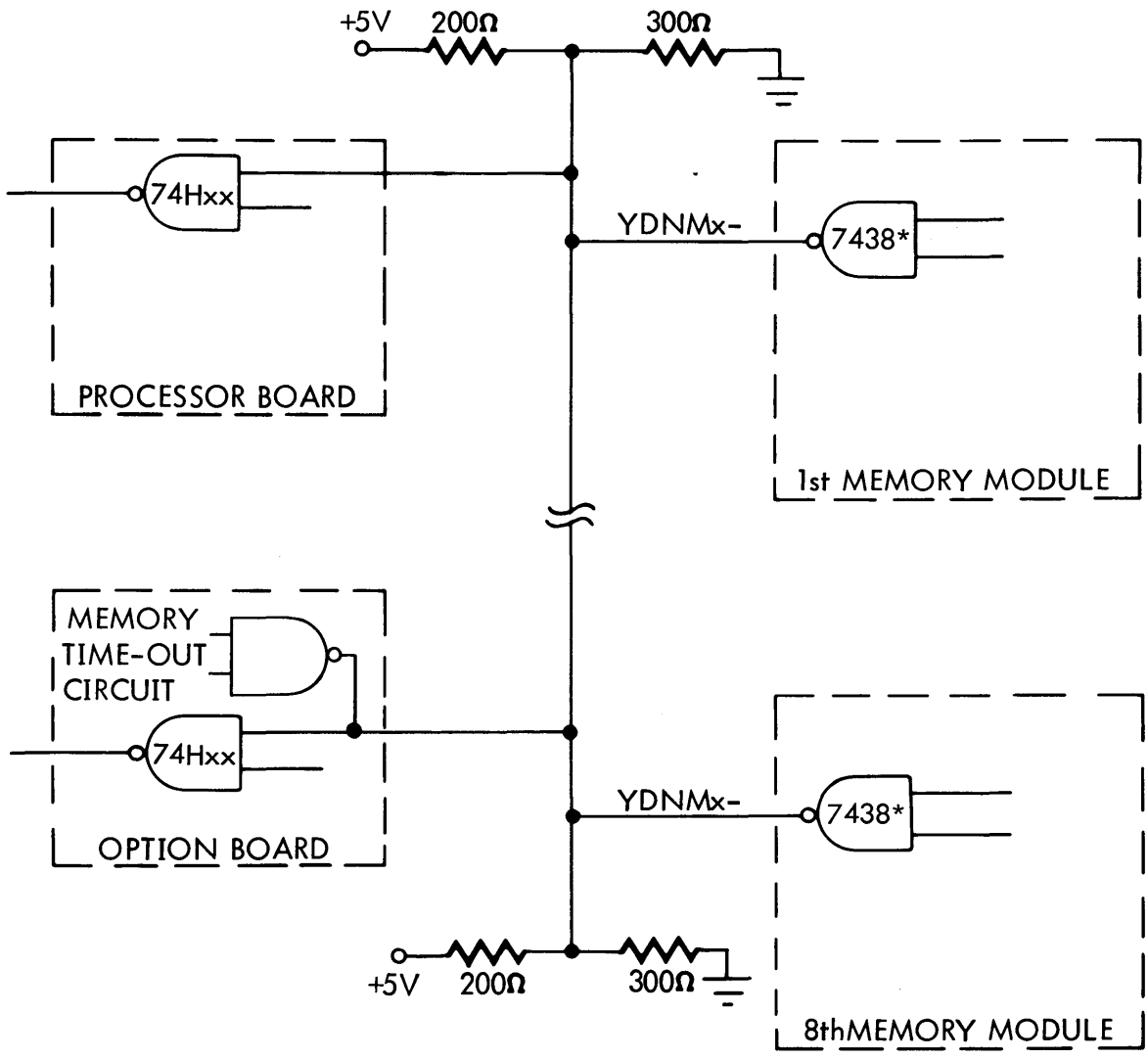
Figure 2-4. Typical Address and Control Bus Configuration

INSTALLATION



* THE 7438s ARE SELECTED

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Figure 2-5. Typical Memory-Acknowledgment Bus

2.6 INTERCONNECTION

All memory input and output signals are routed through connector P1 on the PC card. Refer to table 2-8 for pin assignments of connector P1. Memory stack signals are routed through connectors J1 and J2 on the PC card. Refer to tables 2-9 and 2-10 for pin assignments of connectors J1 and J2.

Table 2-2. P1-Connector Pin Assignments

Pin	Row A (Bottom)	Row B (Top)
1	+22.5V (N/U)	+20V (N/U)
2	+20.6V	+20.6V
3	-12V	-12V
4	-12V	-12V
5	LFRFC+ (N/U)	+5 VMEM (N/U)
6	+5V	+5V
7	+5V	+5V
8	+5V	+5V
9	Ground	Ground
10	SPFA - (N/U)	SRST -
11	MYAA00+	MYAB00+
12	MYAA01+	MYAB01+
13	MYAA02+	MYAB02+
14	MYAA03+	MYAB03+
15	MYAA04+	MYAB04+
16	MYAA05+	MYAB05+
17	MYAA06+	MYAB06+
18	MYAA07+	MYAB07+
19	MYAA08+	MYAB08+
20	MYAA09+	MYAB09+
21	MYMA09+ (N/U)	MYMB09+ (N/U)
22	MYAA10+	MYAB10+
23	MYMA10+ (N/U)	MYMB10+ (N/U)
24	MYAA11+	MYAB11+
25	MYMA11+ (N/U)	MYMB11+ (N/U)
26	MYAA12+	MYAB12+
27	MYMA12+ (N/U)	MYMB12+ (N/U)
28	MYAA13+	MYAB13+
29	MYMA13+ (N/U)	MYMB13+ (N/U)
30	MYAA14+	MYAB14+
31	MYMA14+ (N/U)	MYMB14+ (N/U)
32	MYAA15+	MYAB15+
33	MYMA15+ (N/U)	MYMB15+ (N/U)
34	MYKA16+ (N/U)	MYKB16+ (N/U)
35	MYKA17+ (N/U)	MYKB17+ (N/U)
36	MYKA18+ (N/U)	MYKB18+ (N/U)
37	MYKA19+ (N/U)	MYKB19+ (N/U)
38	Ground	Ground
39	MRQYA -	MRQYB -
40	MRMYA -	MRMYB -
41	Ground	Ground
42	YDNMA -	YDNMB -
43	MHMY -	MHGY -
44	Ground	Ground
45	MWRYA+	MWRYB+
46	MWLYA+	MWLYB+
47	Ground	Ground
48	MYDA00 -	MYDB00 -
49	MYDA01 -	MYDB01 -
50	MYDA02 -	MYDB02 -
51	MYDA03 -	MYDB03 -
52	MYDA04 -	MYDB04 -
53	MYDA05 -	MYDB05 -
54	MYDA06 -	MYDB06 -
55	MYDA07 -	MYDB07 -
56	MYDA08 -	MYDB08 -
57	MYDA09 -	MYDB09 -
58	MYDA10 -	MYDB10 -
59	MYDA11 -	MYDB11 -
60	MYDA12 -	MYDB12 -
61	MYDA13 -	MYDB13 -
62	MYDA14 -	MYDB14 -
63	MYDA15 -	MYDB15 -
64	MYDA16 -	MYDB16 -
65	MYDA17 -	MYDB17 -
66	Ground	Ground

Table 2-3. J1-Connectors

Pin	Row A (Component side of stack card)	Row B (Non-component side of stack card)
1	GRD	GRD
2	CA4A	CA4A
3	CC4A	CC4A
4	CA5A	CA5A
5	CC5A	CC5A
6	CA6A	CA6A
7	CC6A	CC6A
8	CA7A	CA7A
9	CC7A	CC7A
10	GRD	GRD
11	GRD	GRD
12	GRD	GRD
13	XS6A	XS7A
14	XS4A	XS5A
15	XS2A	XS3A
16	XS0A	XS1A
17	GRD	GRD
18	GRD	GRD
19	GRD	GRD
20	S15A -	S15A
21	I15A	S14A
22	S14A -	I14A
23	S13A -	S13A
24	I13A	S12A
25	S12A -	I12A
26	S11A -	S11A
27	I11A	S10A
28	S10A -	I10A
29	S09A -	S09A
30	I09A	S08A
31	S08A -	I08A
32	S17A -	S17A
33	I17A	S16A
34	S16A -	I16A
35	S07A -	S07A
36	I07A	S06A
37	S06A -	I06A

INSTALLATION

Table 2-3. J1-Connectors *(continued)*

Pin	Row A (Component side of stack card)	Row B (Non-component side of stack card)
38	S05A –	S05A
39	I05A	S04A
40	S04A –	I04A
41	S03A –	S03A
42	I03A	S02A
43	S02A –	I02A
44	S01A –	S01A
45	I01A	S00A
46	S00A –	I00A
47	GRD	GRD
48	GRD	GRD
49	GRD	GRD
50	YS1A	YS0A
51	YS3A	YS2A
52	YS5A	YS4A
53	YS7A	YS6A
54	GRD	GRD
55	GRD	GRD
56	GRD	GRD
57	CA3A	CA3A
58	CC3A	CC3A
59	CA2A	CA2A
60	CC2A	CC2A
61	CA1A	CA1A
62	CC1A	CC1A
63	CA0A	CA0A
64	CC0A	CC0A
65	GRD	GRD

Table 2-4. J2-Connector Pin Assignments

Pin	Row A (Component side of stack card)	Row B (Non-component side of stack card)
1		
2	CA4B	CA4B
3	CC4B	CC4B
4	CA5B	CA5B
5	CC5B	CC5B
6	CA6B	CA6B
7	CC6B	CC6B
8	CA7B	CA7B
9	CC7B	CC7B
10	GRD	GRD
11	GRD	GRD
12	GRD	GRD
13	XS6B	XS7B
14	XS4B	XS5B
15	XS2B	XS3B
16	XS0B	XS1B
17	GRD	GRD
18	GRD	GRD
19	GRD	GRD
20	S00B	S00B –
21	I00B	S01B –
22	S01B	I01B
23	S02B	S02B –
24	I02B	S03B –
25	S03B	I03B
26	S04B	S04B –
27	I04B	S05B –
28	S05B	I05B
29	S06B	S06B –
30	I06B	S07B –
31	S07B	I07B
32	S16B	S16B –
33	I16B	S17B –
34	S17B	I17B
35	S08B	S08B –
36	I08B	S09B –
37	S09B	I09B
38	S10B	S10B –
39	I10B	S11B –
40	S11B	I11B
41	S12B	S12B –
42	I12B	S13B –
43	S13B	I13B
44	S14B	S14B –
45	I14B	S15B –
46	S15B	I15B
47	GRD	GRD
48	GRD	GRD
49	GRD	GRD
50	YS1B	YS0B
51	YS3B	YS2B
52	YS5B	YS4B
53	YS7B	YS6B
54	GRD	GRD
55	GRD	GRD
56	GRD	GRD
57	CA3B	CA3B
58	CC3B	CC3B
59	CA2B	CA2B
60	CC2B	CC2B
61	CA1B	CA1B
62	CC1B	CC1B
63	CA0B	CA0B
64	CC0B	CC0B
65	GRD	GRD

SECTION 3
OPERATION

The memory system contains no operating controls or indicators.

SECTION 4
THEORY OF OPERATION

This section describes the operation of the core memory circuits, referencing sheet numbers of the memory logic diagram (91C0377 in volume 2) and memory mnemonics (section 6). For ease of reading, some mnemonics are written with the variables n and x in place of the actual numbers and letters. For example, memory data mnemonics MYDA00- through MYDA15- are written MYDxnn-. Figure 4-1 is a memory-interface block diagram, and figure 4-2 shows the configuration of a typical expanded memory.

4.1 MEMORY CYCLE

During any memory cycle, the memory always performs a reading sequence followed by a writing sequence. When a word is transferred from the processor to memory, the memory cycle is a **clear/write** operation. When a word is transferred from memory to the processor, the memory cycle is a **read/restore** operation.

4.1.1 Clear/Write

A clear/write operation loads the memory. The clearing sequence resets the addressed cores to zero. The writing sequence then loads data into the addressed cores.

During the clearing sequence, the X and Y wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed.

During the writing sequence, the X and Y wires of an address word are activated (write current) to magnetize the cores to one. If a core is to be zero, the associated inhibiting wire generates a current that cancels the X current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into memory.

4.1.2 Read/Restore

A read/restore operation reads information from memory. The reading sequence unloads the addressed word from memory. The restoring sequence immediately reloads (writes) the word into the same core location.

During the reading sequence, the X and Y wires of an addressed word are activated (read current) to magnetize the cores to zero. Addressed cores already at zero are not changed. If an addressed core is one, a voltage is induced in the associated sense wire when the core switches to zero. The sense voltage is then interrogated and amplified to provide a memory read bit.

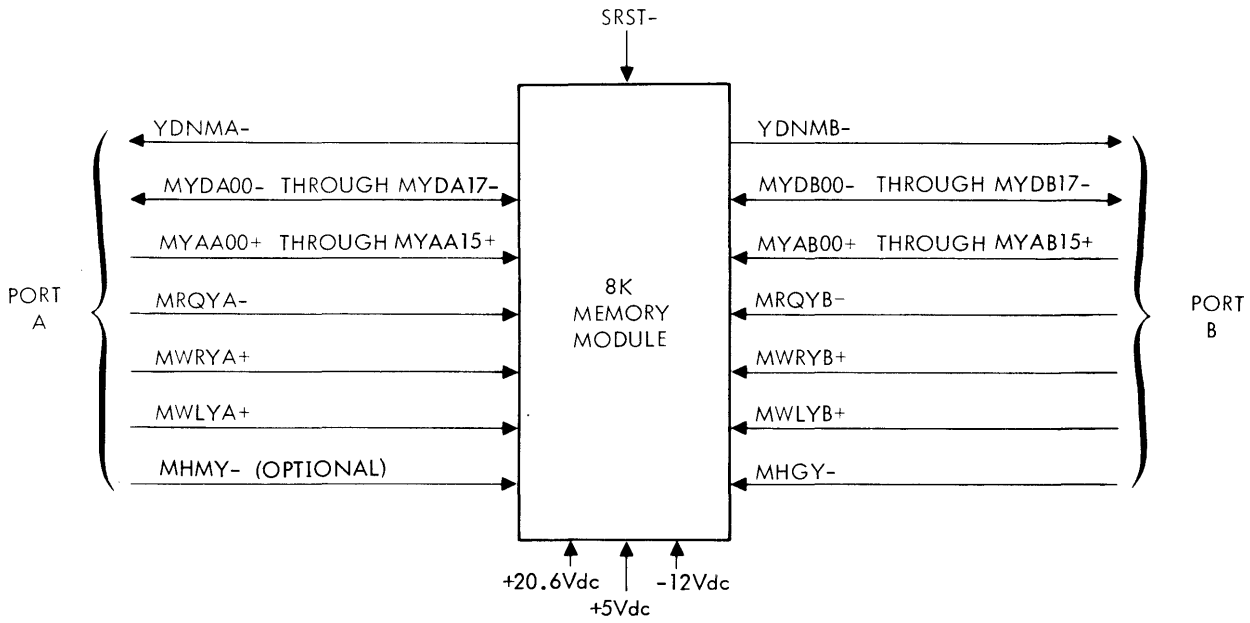

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Figure 4-1. Memory Interface Block Diagram

During restoring sequence, the X and Y wires of an addressed word are activated (write current) to magnetize the cores to one. If a core is to be zero, the associated inhibiting wire generates a current that cancels the X current, preventing the core from switching. The word, with correct bit configuration, is thus loaded into the same core location.

4.2 MAGNETIC CORE OPERATION

The basic information storage element of the memory is the magnetic core. The core is a toroid of ferrite that can be magnetized in two discrete directions representing the presence or absence of a binary bit. The magnetization is a result of current passing through the core. Total current must reach a threshold strength before the core becomes magnetized. The direction of current flow through the core determines the direction of magnetization; the two possible directions of current flow are called **read** and **write**.

The memory uses the coincident-current technique to magnetize cores. Two perpendicular wires, X and Y, pass through each core. During memory operations, the current on any X or Y wire is approximately one-half of the current necessary to magnetize a core. Because of the orientation of the cores and wires in a plane, only the core at the intersection of two activated wires becomes magnetized. A three-core-by-three-core matrix is shown in figure 4-3. The figure indicates the total driving current received by each core when wires X2 and Y2 are activated. Only the center core is magnetized, since it is the only one that receives the full driving current, I.

4.3 MEMORY INTERFACE OPERATION

Typical memory interface waveforms are illustrated in figure 4-4. The memory cycle is initiated when the negative transition of the memory start request (MRQYx −) is received by port A or B (the module addresses must have been stable for at least 12 nanoseconds). The memory first resolves priority in case of conflicting requests on the two ports, and then begins its memory timing sequences.

A memory acknowledgment signal (YDNMx −) is generated 170 nanoseconds (typical) before read data is stable on the memory data bus. The pulse width of YDNMx − is 185 nanoseconds (typical), and its trailing edge (positive-going transition) is used to clock the memory read data into a data register in the processor.

For a clear/write operation, the read/write control signal (MWRYx + or MWLYx +) must be received by the memory no later than 140 nanoseconds after the leading edge of the memory start request signal. The memory writes full or half words (bytes) as commanded. Bytes not written into retain previously written data.

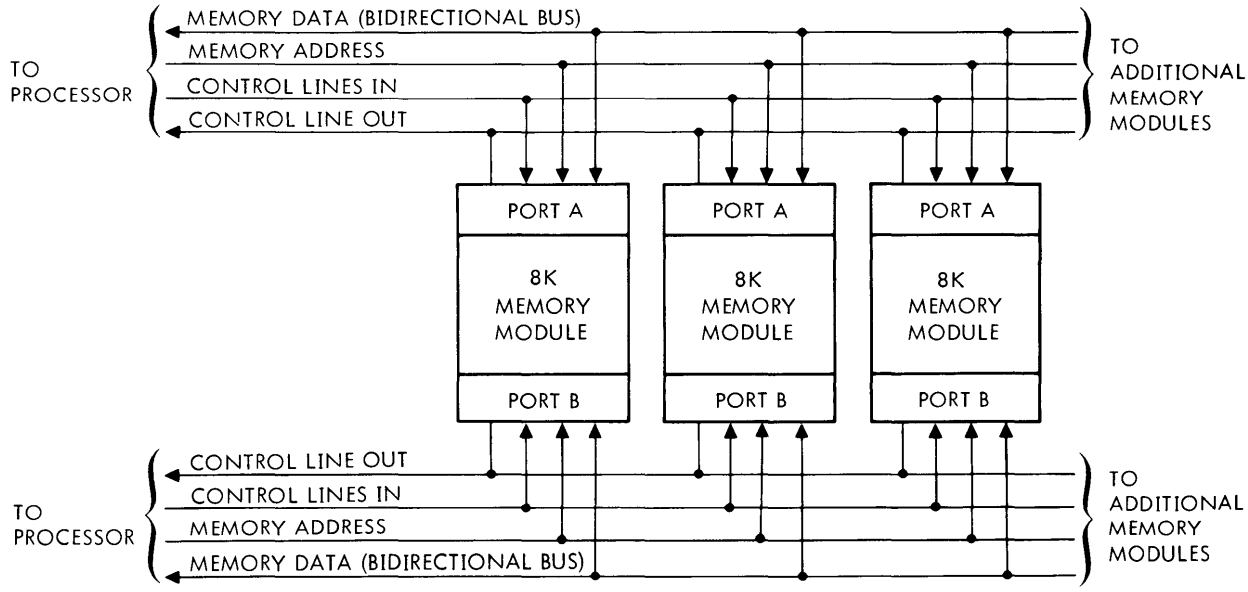

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Figure 4-2. Memory Expansion Block Diagram

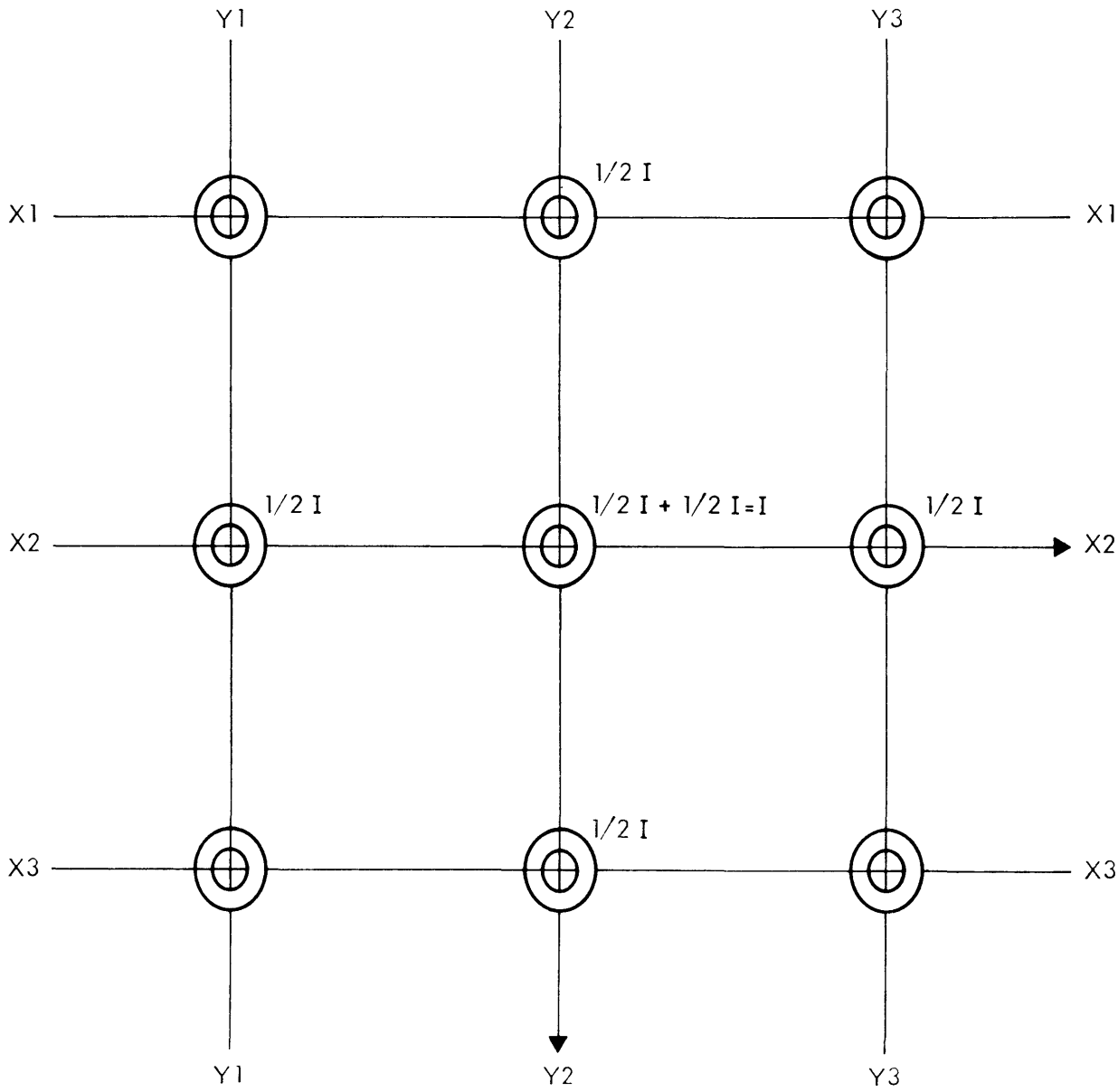

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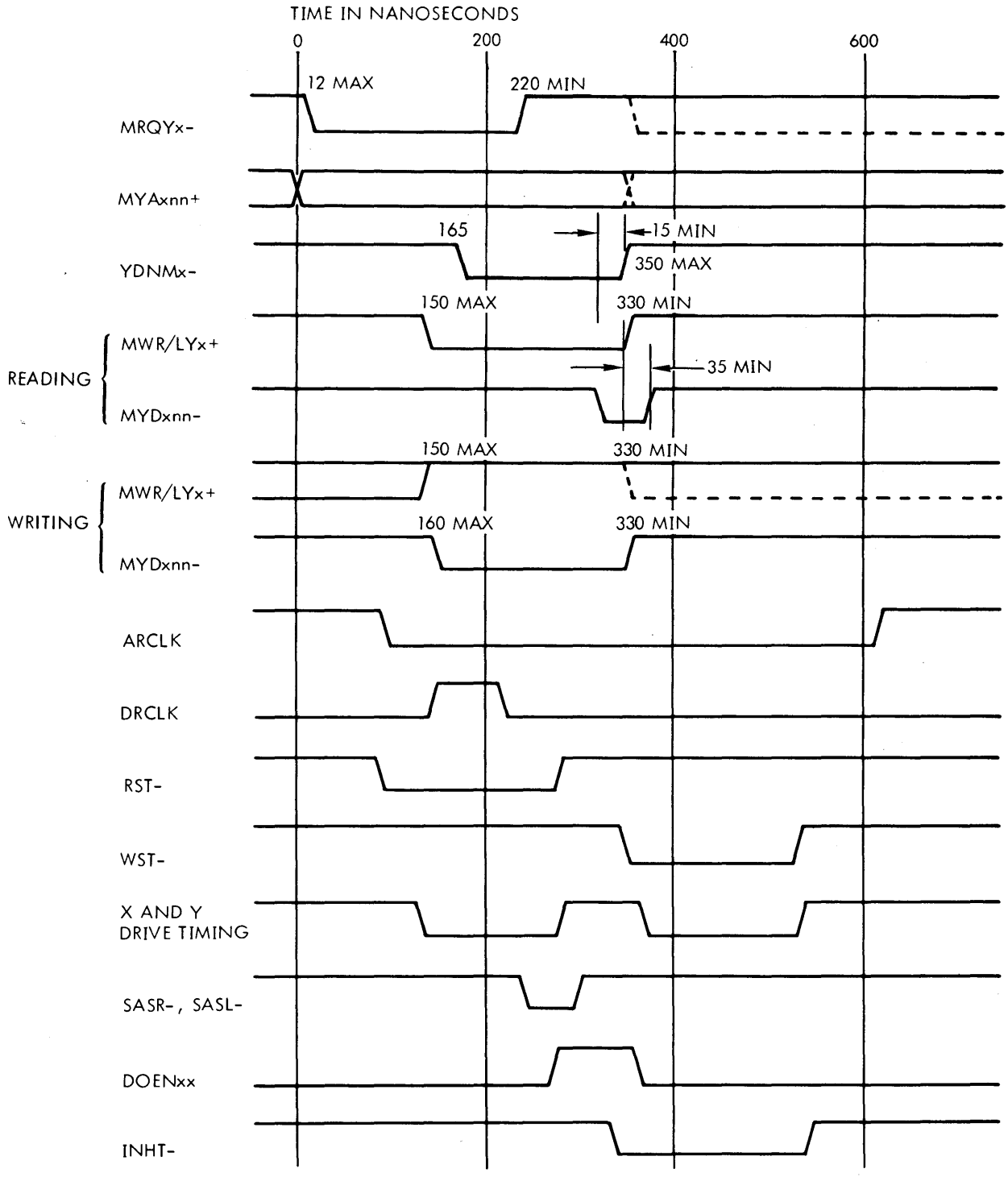
Figure 4-3. Three-Core-by-Three-Core Matrix

THEORY OF OPERATION



NOTE: ALL TIMES ARE IN NANOSECONDS AND ARE RELATIVE TO A STABLE ADDRESS AT MEMORY CONNECTOR (T=0).

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Figure 4-4. Typical Memory Interface Waveforms

4.4 MEMORY STACK CARD

The memory stack card contains a diode decoding matrix and a planar magnetic-core array composed of sixteen 4K mats (eighteen 4K mats for the 18-bit memory). Each mat, which is one bit of the 16-bit word, contains 64 rows (X lines) and 64 columns (Y lines) of magnetic cores (figure 4-5). Selection of one of the 64 X or 64 Y lines is implemented with two diodes per line and an 8-by-8 driver/sink switching matrix where, the diode end of the matrix is the drive end and the nondiode end, the sink end (figure 4-6). These are driven by the driver/sink switching circuits. There are 256 diodes for each 4K stack. Two memory stack cards are installed on each memory PC card to form the 8K memory increment.

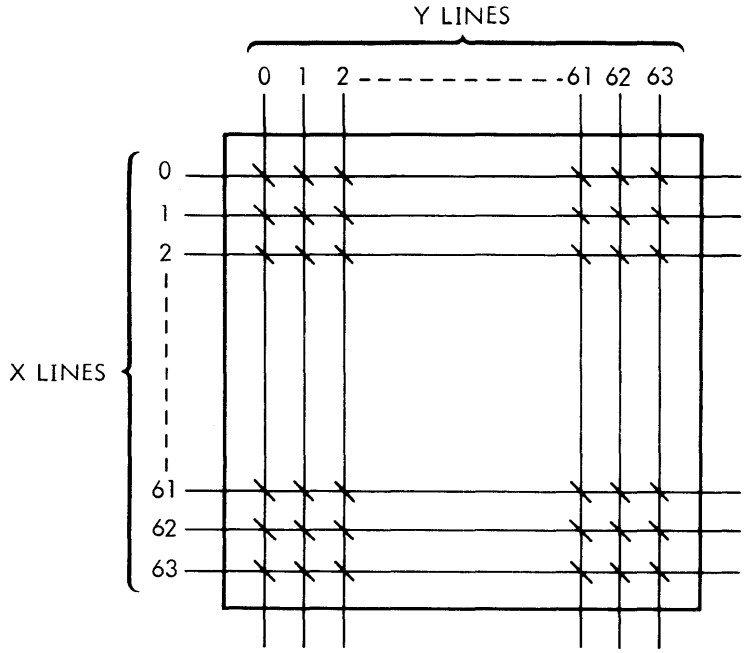
Three control lines (X, Y, and sense/inhibit) pass through each magnetic core:

a. *X Lines.* Each X line passes through the same row of cores in all 4K mats. The current in the selected X line will be one-half the current required to switch the state of a core. The direction of the current depends on whether memory is being written into or read from.

b. *Y Lines.* Each Y line passes through the same column of cores in all 4K mats. The current in the selected Y line will be one-half the current required to switch the state of a core. The direction of the current depends on whether memory is being written into or read from.

c. *Sense/Inhibit Lines.* A sense/inhibit line passes through all cores of a single 4K mat, parallel to the X lines and perpendicular to the Y lines. Each mat has an individual sense/inhibit line. This senses the state of the cores. If a core contains one, an induced voltage is applied to the associated sense amplifier; if a core contains zero, no voltage is induced. During reading, the sense amplifier outputs are strobed into the memory data register.

The sense/inhibit line also routes an inhibiting current through an addressed core into which a zero is to be written. During writing a half-current is applied to each of the selected (X and Y) lines to set the addressed cores to one. For zero cores, the inhibit current cancels the X line current to prevent the addressed core from switching to one. A one from the memory data bus (MYDxnn – low) sets the addressed core to zero by producing the inhibiting current. A zero from the memory data bus produces no such current.



NOTE: A SENSE/INHIBIT LINE, NOT SHOWN ABOVE, ALSO PASSES THROUGH ALL CORES OF A 4K MAT PARALLEL TO THE X LINES.

VTII-1202

Figure 4-5. 4K Core Mat

4.5 MEMORY PC CARD

The memory PC card (p/n 44P0613) contains the following functional circuits:

a. Module address selector

b. Priority selection

c. Timing control

d. Address register

e. Address multiplexors and decoders

f. Predrivers

g. Driver/sink switches

h. Current sources

i. Data register

j. Sense/inhibit timing

k. Sense/inhibit circuits

l. Voltage regulators

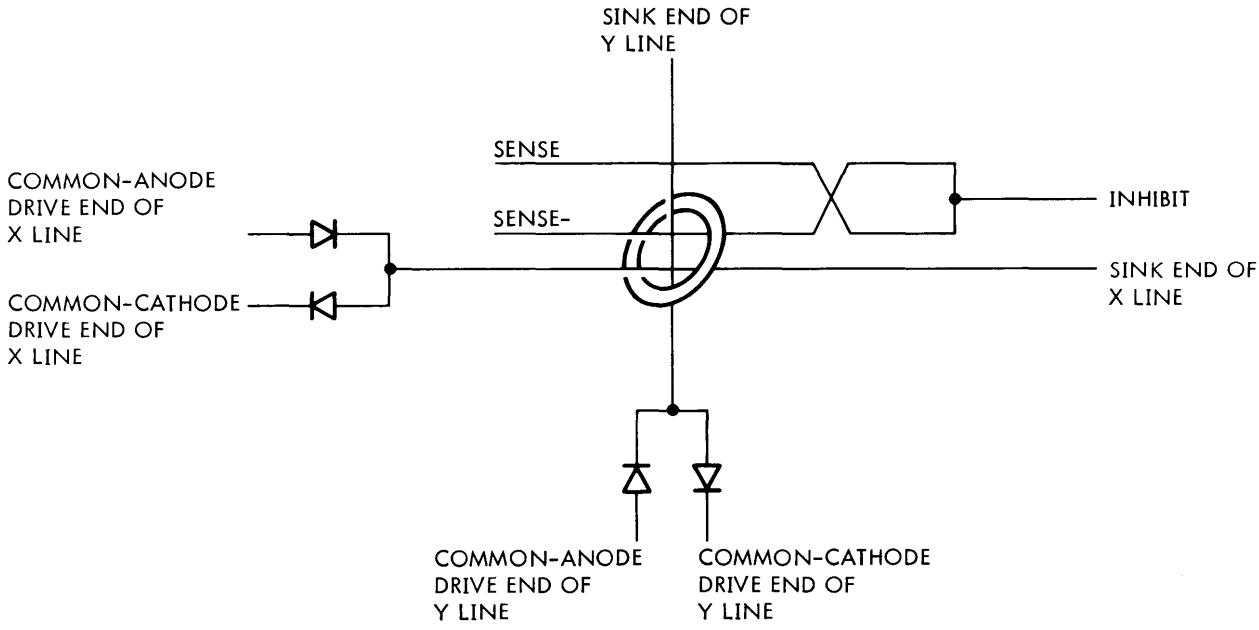
The functional memory circuits are illustrated in the block diagram (figure 4-7) and described in the following sections.

4.5.1 Module Address Selectors

The module address selectors (sheets 5 and 6) monitors address bits 10 through 15 and enables the priority-selection circuit when the assigned address of the memory module is detected. Module address assignments for each memory module are determined by jumper connections on the memory circuit card.

Figure 4-8 is a schematic of the module address selector for port A showing jumper connections for the first 8K memory module. When the assigned address is detected, the port-decoding signal APDEC- goes low.

For normal memory operation, address bits 0 and 13 are jumpered as shown in figure 4-8. However, to provide odd even address interleaving between memory modules, the jumpers for bit 0 and 13 are switched so that bit 0 is routed to the bit 13 line and bit 13 to the bit 0 line (dotted line connections).



VTII-1203

Figure 4-6. Memory Control Lines

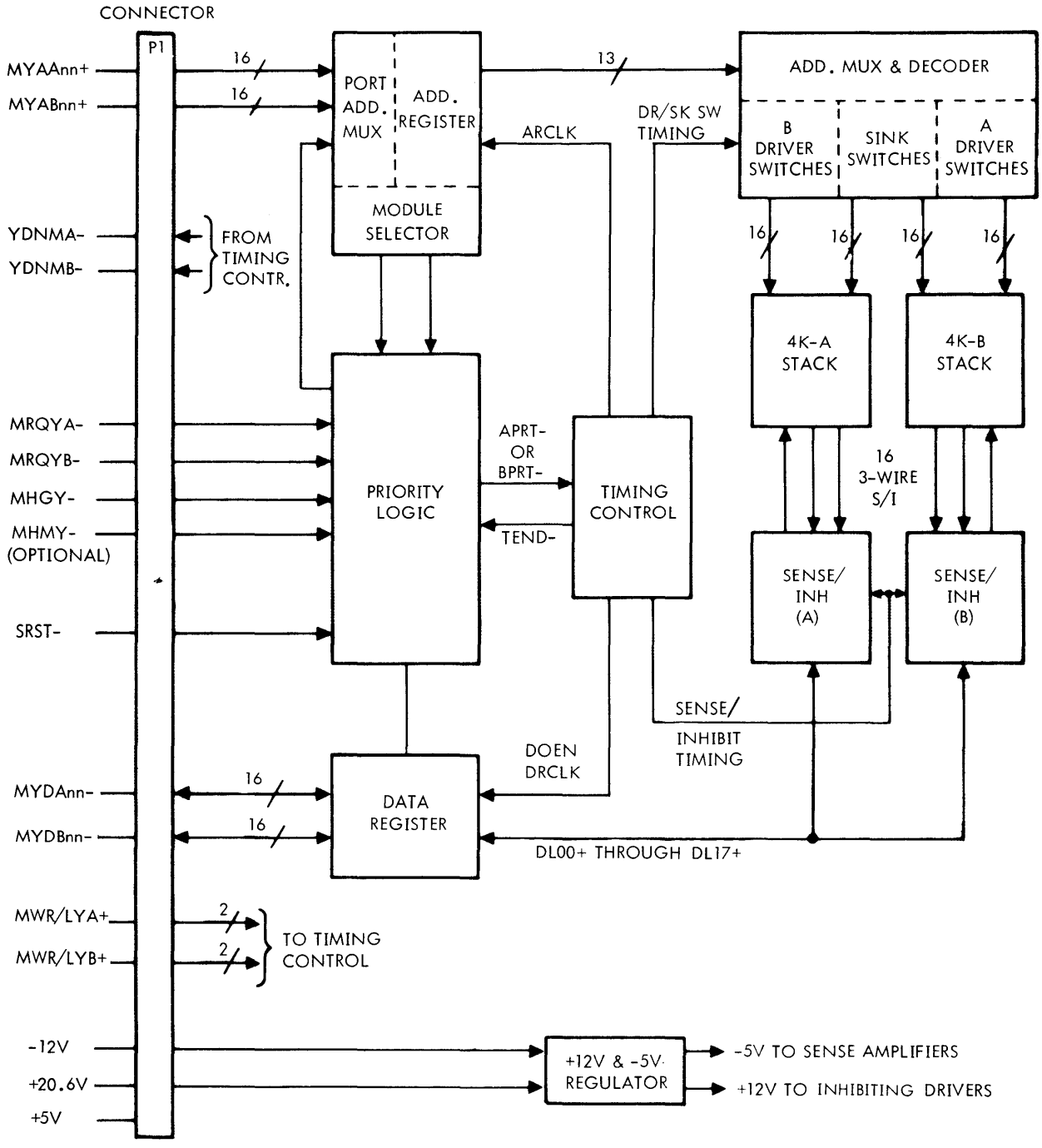
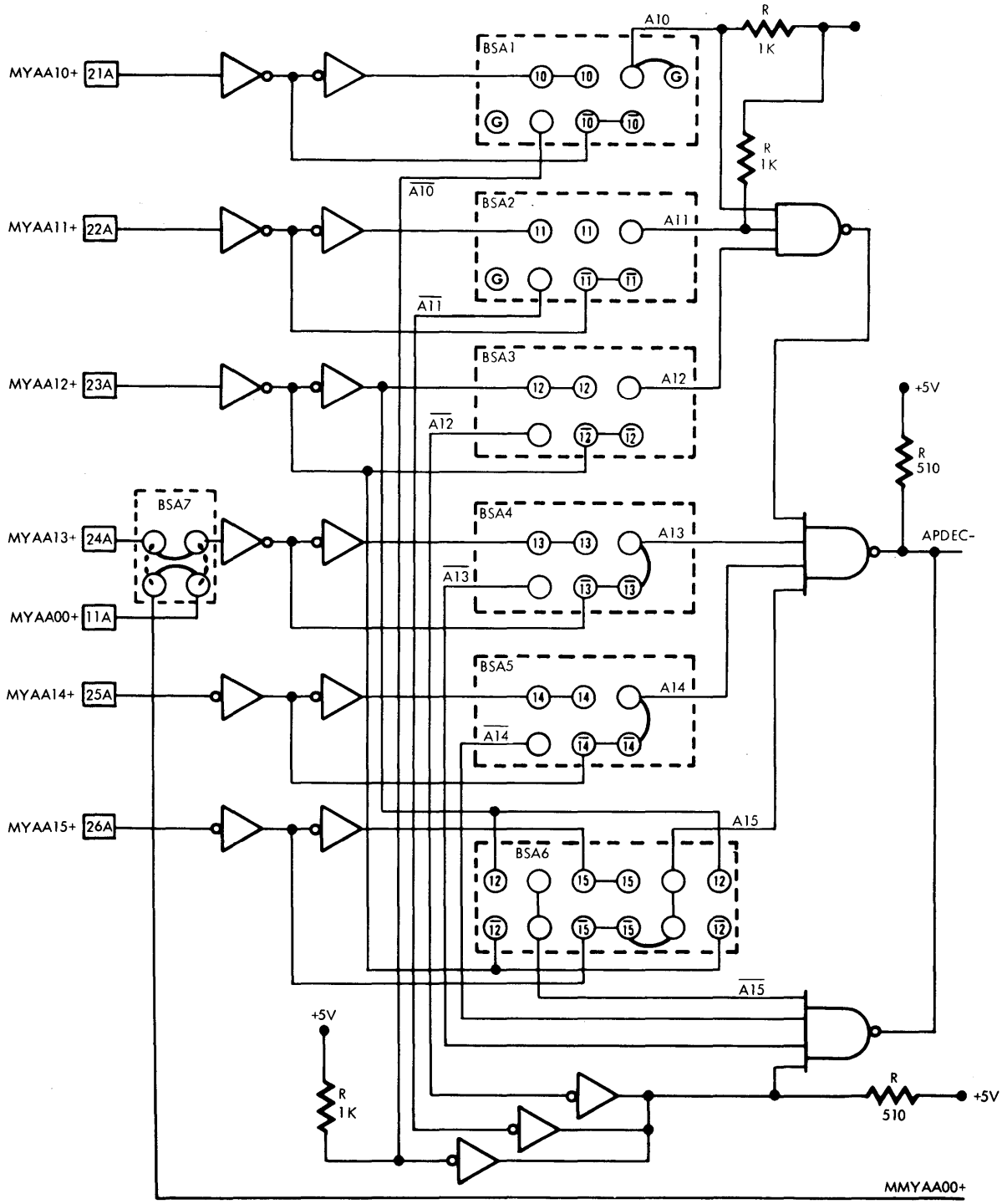


Figure 4-7. Core Memory Functional Block Diagram

THEORY OF OPERATION



NOTES:

1. THE ABOVE JUMPER ASSIGNMENTS ARE LISTED IN THE FIRST COLUMN OF TABLE 2-1.
2. FOR INTERLEAVING, BSA7 IS WIRED AS SHOWN BY THE DOTTED LINES INSTEAD OF THE SOLID LINE.

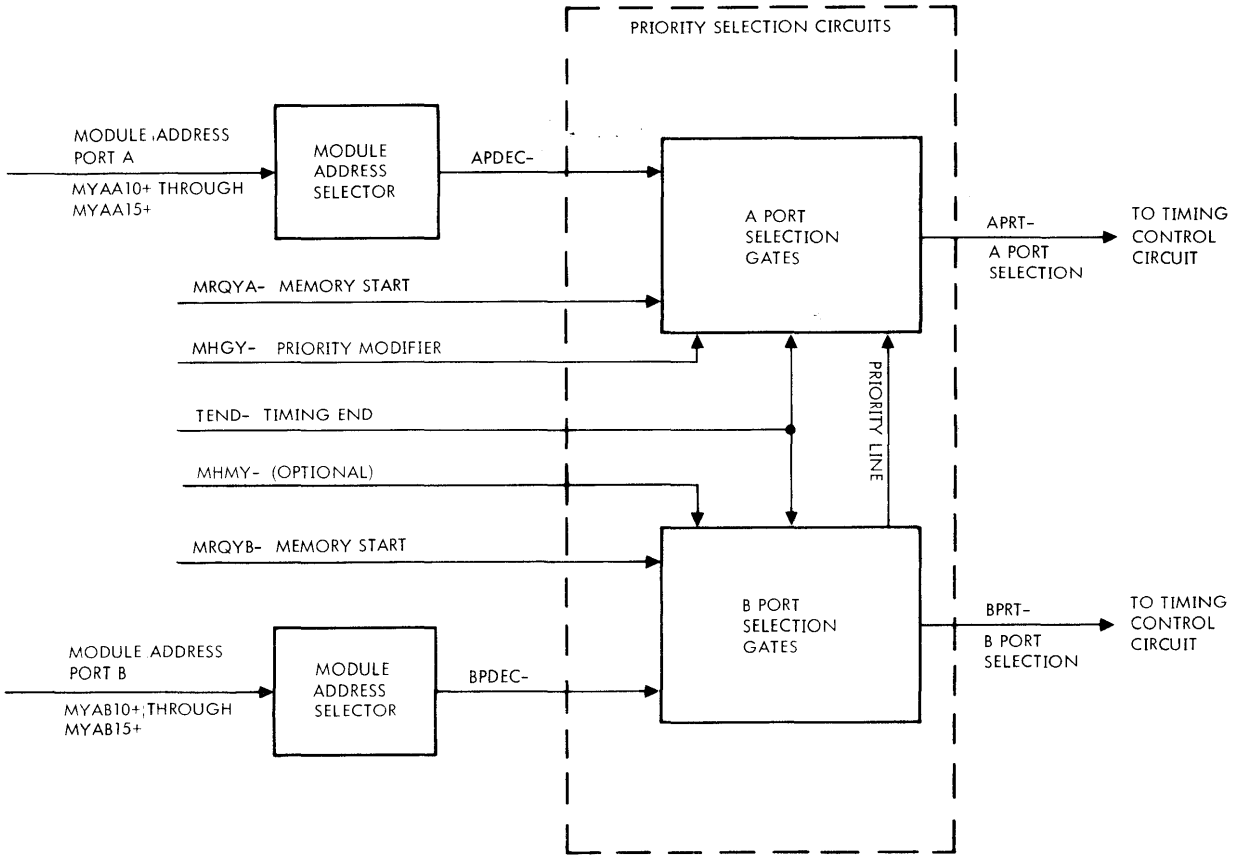
VTII-1532A

Figure 4-8. Address Jumpers for First 8K Memory Module (Not Interleaved)

4.5.2 Priority Selection

The priority selection circuit (sheet 7) determines which port has priority when the memory is not busy. If there are continuous requests on port B (which has the higher priority), port A requests are not acknowledged. However, ports A and B can be used simultaneously for different memory modules.

As illustrated in figure 4-9, the priority-selection circuit consists of A- and B-port selection gates (refer to figure 4-10 for B port waveforms). The selection gates receive a decoding signal (APDEC- or BPDEC-) from the module address selector, and memory start signal (MRQYA- or MRQYB-) from either the processor, PMA, or memory map. These signals generate a port-selection signal (APRT- or BPRT-) if the memory is not busy (TEND- is high) and priority permits. Priority is determined by two signals: a priority-line signal from the B-port selection gates, and a priority modifier (MHGY-) from either the writable control store, PMA, or memory map depending on the system configuration. A low MHGY- inhibits the A-port selection gates in all memory modules. In this condition, all access to memory through port A is inhibited, regardless of the module address or status of port B. The priority-line signal from the B-port selection gates is high when that port is busy, thus inhibiting the A-port selection gates. An optional priority-modifier (MHMY-) can be used to disable port B. This is implemented with a jumper connection on the PC card.



VTII-1517

Figure 4-9. Priority Selection Block Diagram

THEORY OF OPERATION

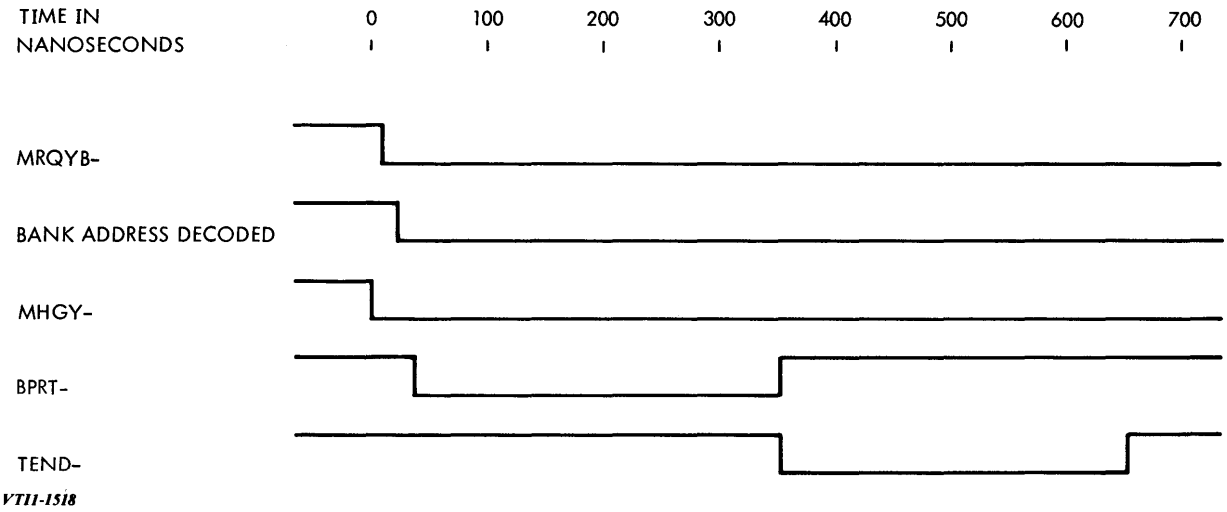


Figure 4-10. Priority Selection Waveforms (B Port)

4.5.3 Timing Control

The timing control circuit (sheets 8, 9, and 10) provides the timing and control signals required for memory operation. Refer to figure 4-11 for timing control waveforms.

A memory cycle is initiated when a port-selection signal (APRT − or BPRT −) causes a pulse (E1) to be sent into tapped delay line DL1. At precise intervals along the delay line, signals are tapped and combined with control signals to generate internal memory timing, as well as a memory acknowledgment signal (YDNMA − or YDNMB −). The space between adjacent output taps (E2 through E25) provides approximately 7 nanoseconds delay.

The logic level of the read/write control signal determines the type of memory operation. A high produces a clear/write, and a low produces a read/restore. During a clear/write operation the timing-control circuit sends a data-input enabling signal (DIENxx+) to the memory data register. During a read/restore operation, the timing-control circuit generates strobe signals SASR − and SASL − for the sense amplifiers.

4.5.4 Address Register

At the beginning of each memory cycle, the 13-bit address register accepts one address from either port A or port B. The first twelve output bits (L00+ through L11+) go to the address multiplexors and decoders. The remaining bit (L12+) goes to the driver/sink switch timing circuit for stack selection. When address bit 12 (MYAA12+ or MYAB12+) goes low, L12+ goes low and selects the 4K-A stack. The 4K-B stack is selected by a high address bit 12. The address register is illustrated on sheets 11 and 12 of the logic diagram.

Each address-register flip-flop has a gate circuit connected to its input to multiplex the port address. The port address is gated through to the address-register flip-flops by A- or B-port enabling signals (APEN, BPEN). The selected address is then clocked into the flip-flops on the negative transition of the address-register clock (ARCLK).

4.5.5 Address Multiplexors and Decoders

The address multiplexors and decoders (sheets 17 and 18) provide decoded signals that select the appropriate driver and sink switches to direct X and Y driving currents through the addressed cores. The multiplexor consists of the gate circuits IC91, 92, and 93. The decoders are designated IC94, 95, 96, and 97.

Address bits L00+ through L05+ are multiplexed with the read/write control signals R+ and RB −, and then used to select the proper driver switches for the 4K-A or 4K-B cores. During reading sequence, R+ is high and the multiplexor applies the complement of L00+ through L02+ to decoder IC96 as well as the complement of L03+ through L05+ to decoder IC94. During writing sequence RB − is high and the multiplexor applies the complement of L00+ through L02+ to decoder IC94 and the complement of L03+ through L05+ to decoder IC96. Figures 4-14 and 4-15 illustrate the multiplexing of address bits representing an octal 45 (100 101). The R gates are enabled during reading sequence and the W gates during writing sequence.

Address bits L06+ through L11+ select the proper sink switches, which are common to both 4K-A and 4K-B cores (sink-switch lines contain isolation diodes).

Each decoder circuit is a BCD-to-decimal decoder (figure 4-14). One of the four inputs (pin 12) is connected to ground. Two of the ten outputs (pins 10 and 11) are not used.

Because the multiplexed codes are in complement form, the outputs of decoders IC94 and IC96 are wired in the reverse order from the outputs of IC97 and IC95. Only one of the eight outputs of each decoder is activated (low level) for a particular 3-bit input code. Figures 4-15 and 4-16 illustrate read/write decoding for an octal address of 2345. Mnemonics for the active output of each decoder are indicated.

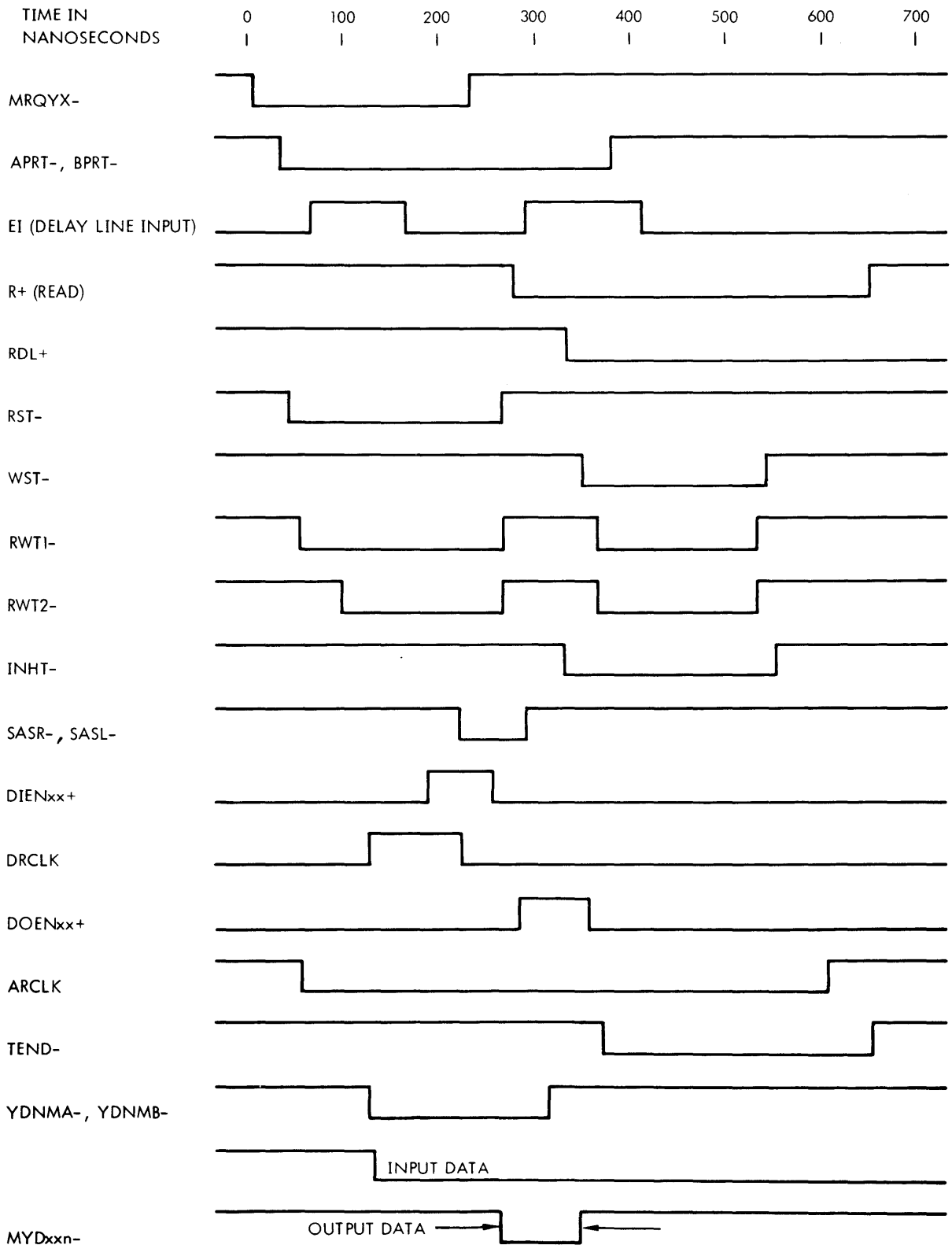
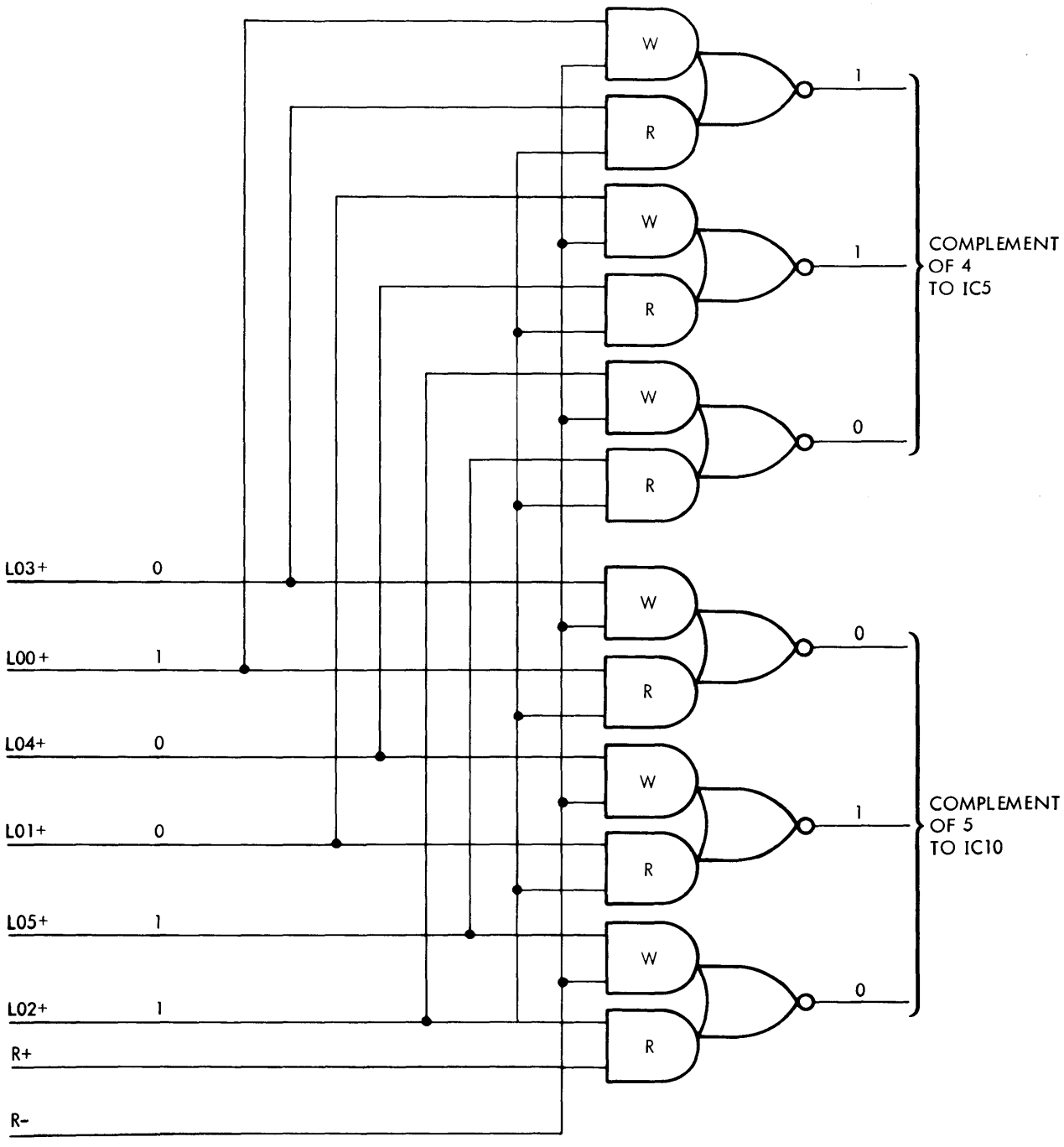


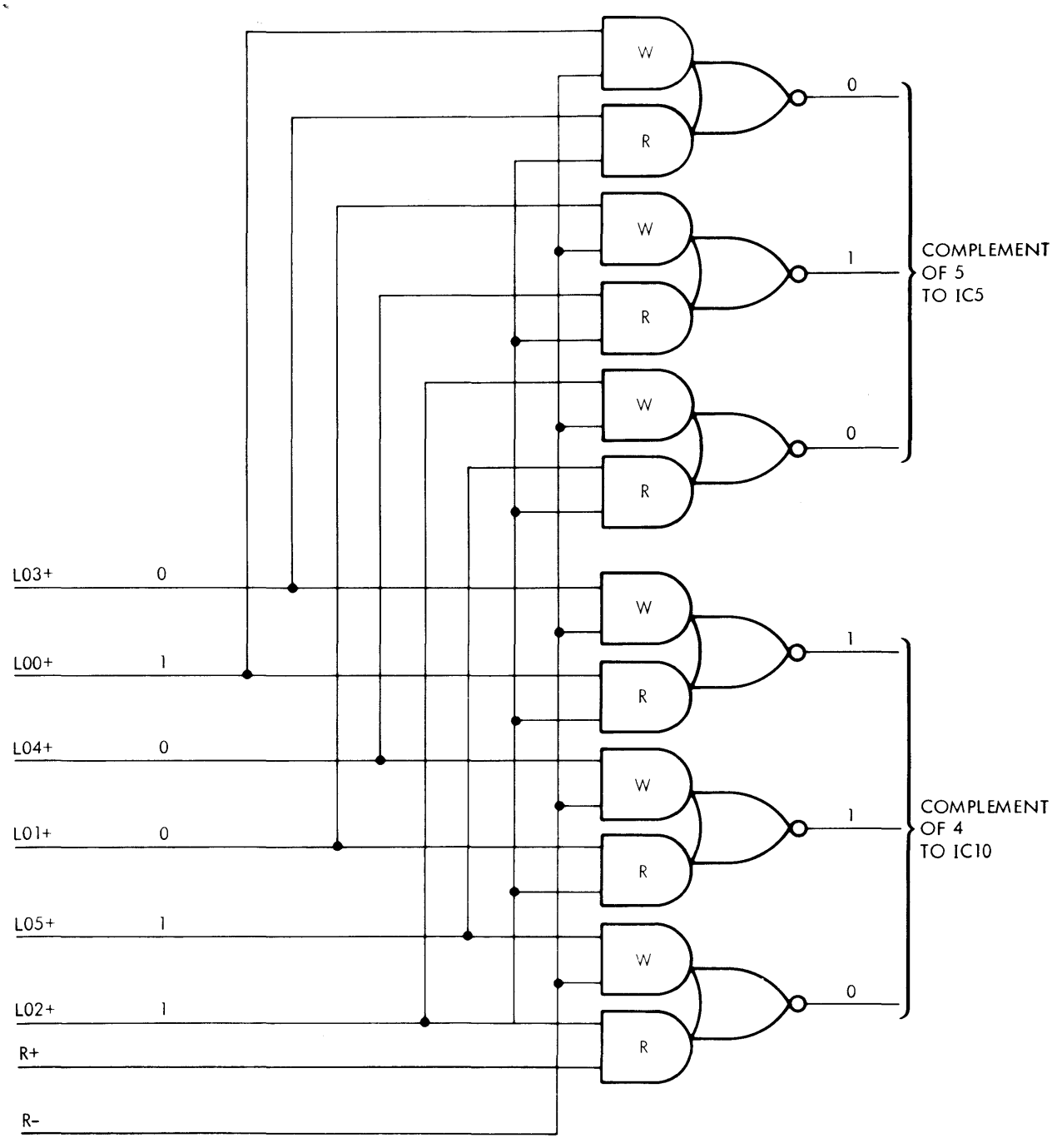
Figure 4-11. Timing Control Waveforms

THEORY OF OPERATION



VTII-1520

Figure 4-12. Read Multiplexing for Octal 45



VTII-1521

Figure 4-13. Write Multiplexing for Octal 45

THEORY OF OPERATION

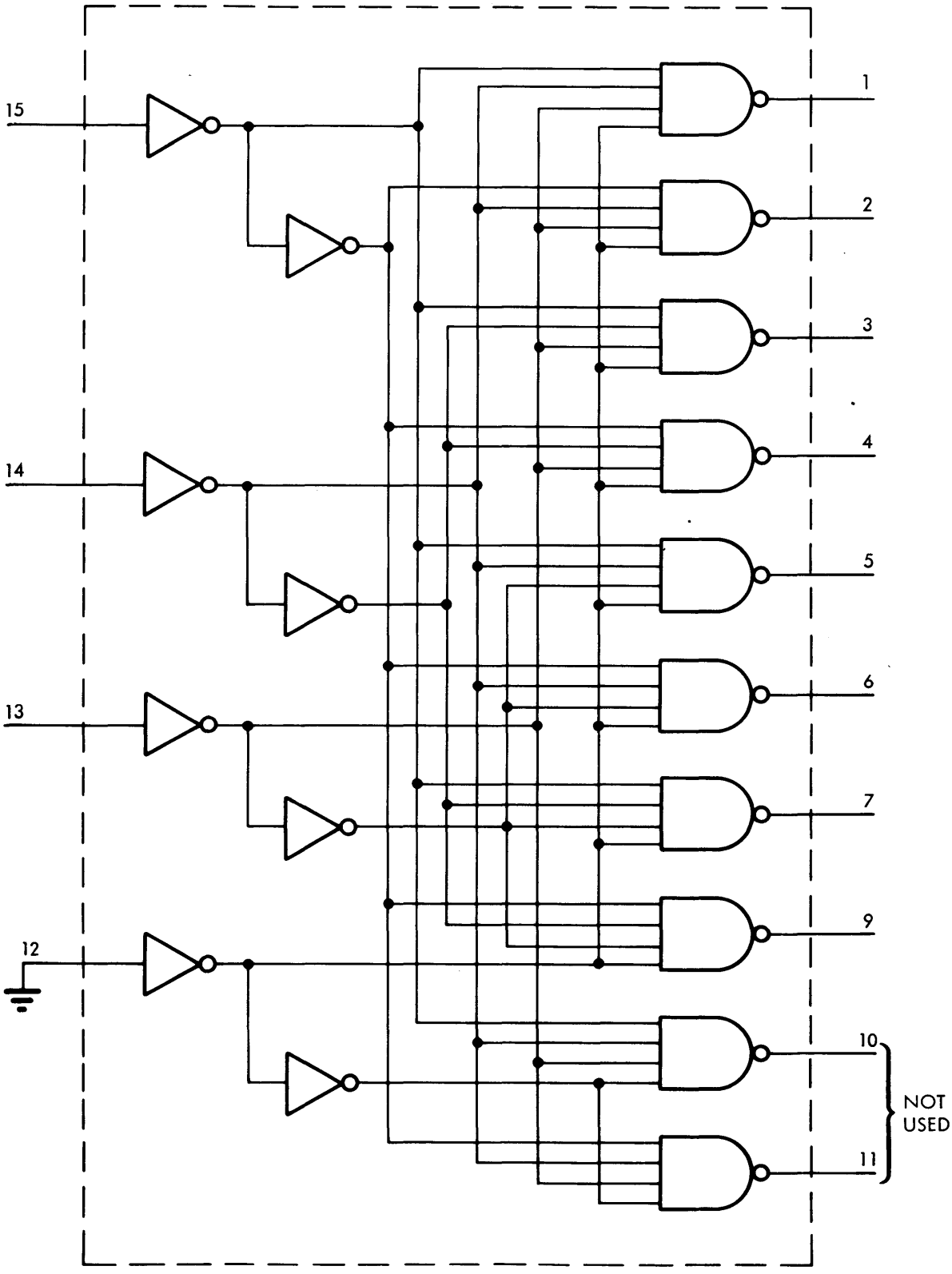
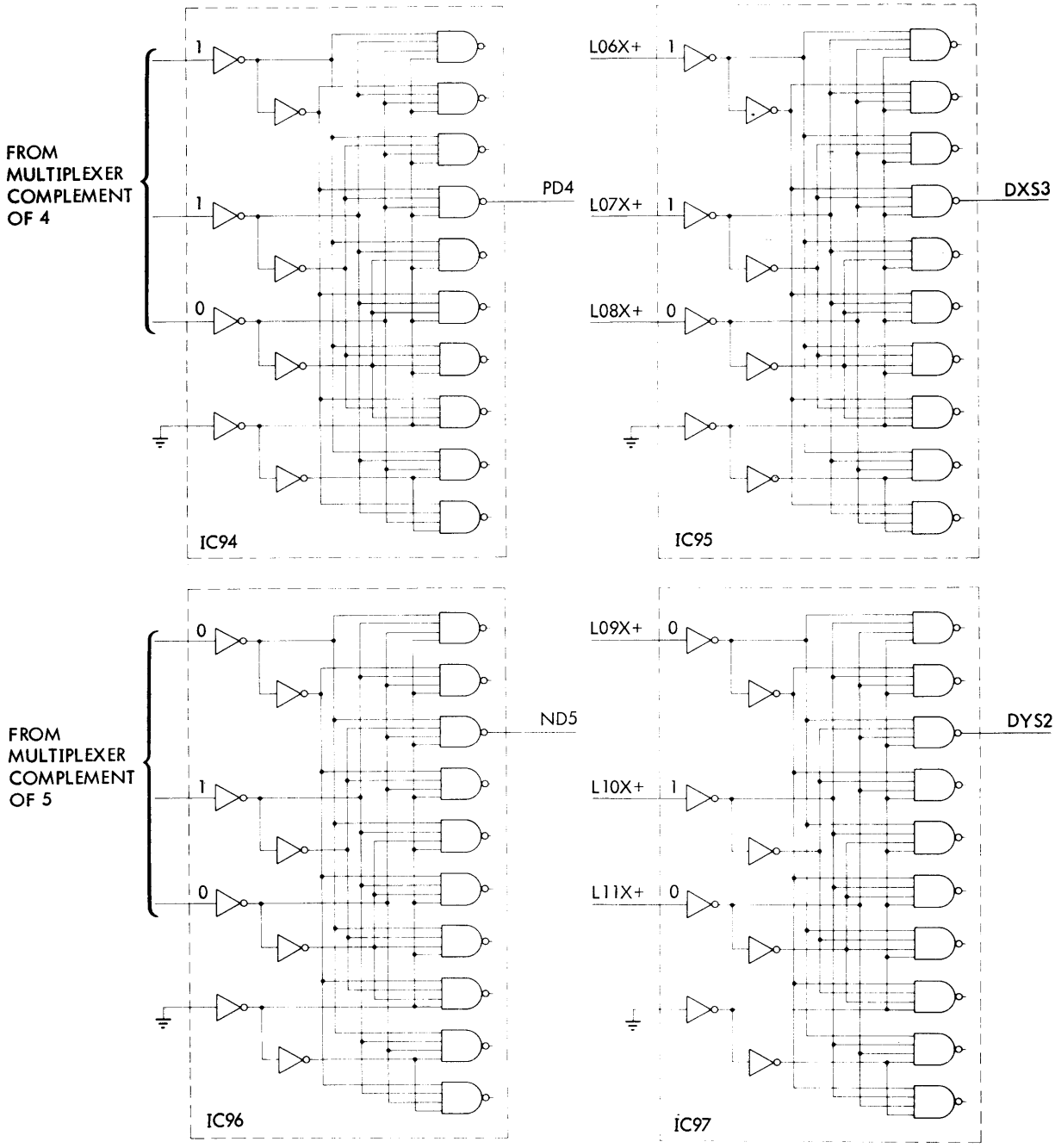


Figure 4-14. Decoder Logic Diagram and Pin Assignment

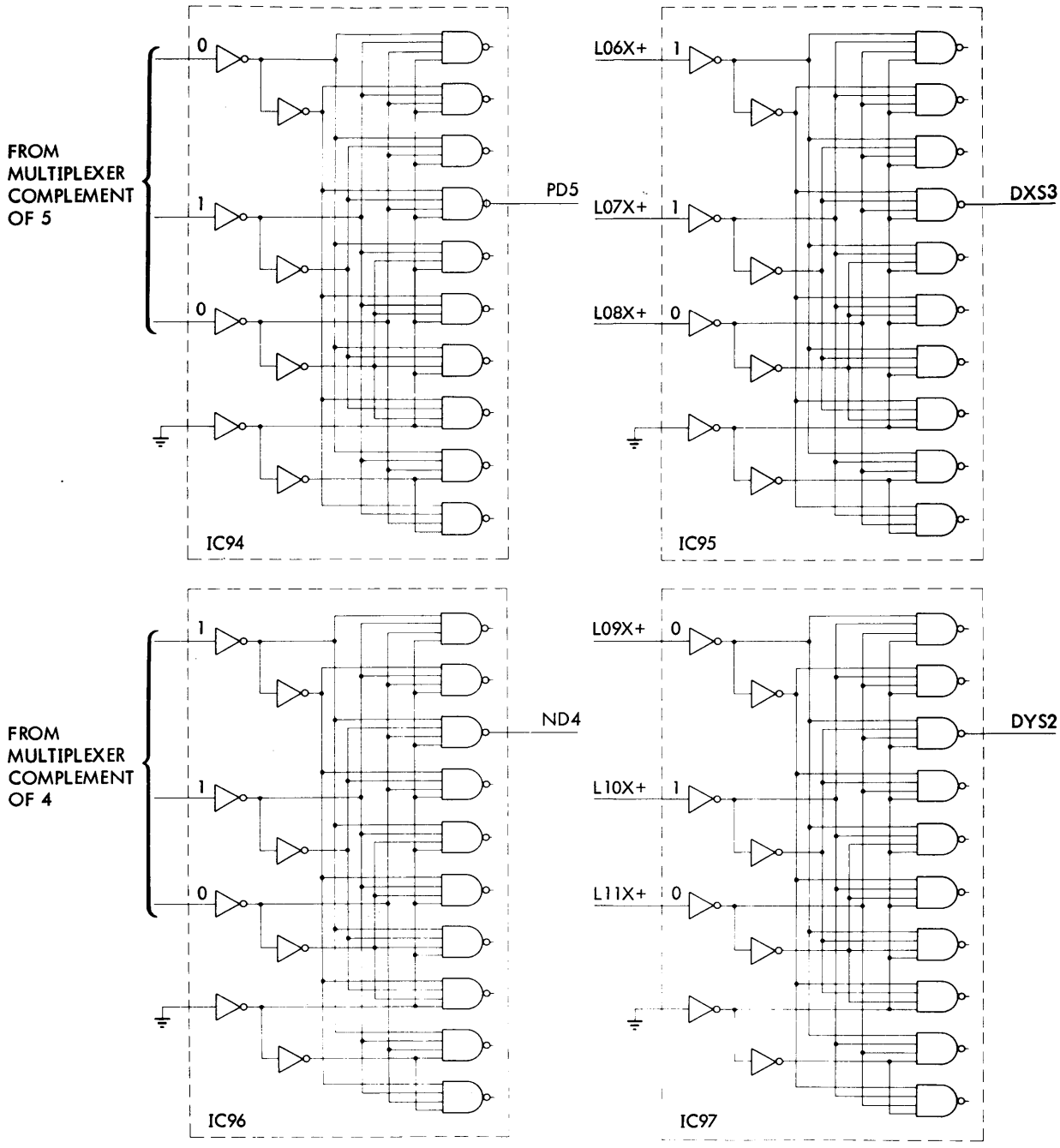


NOTE: THE DESIGNATIONS IC94, IC95, IC96, AND IC97 REFER TO LOGIC DIAGRAM 91C0377

VTII-1535

Figure 4-15. Read Decoding of Octal Address 2345

THEORY OF OPERATION



NOTE: THE DESIGNATIONS IC94, IC95, IC96, AND IC97 REFER TO LOGIC DIAGRAM 91C0377

VTII-1536

Figure 4-16. Write Decoding of Octal Address 2345

4.5.6 Predriver Circuits

The predriver circuits (sheet 19) receive read/write timing and stack-selection signals to produce appropriate currents for the driver and sink switches. The predriver circuits consist of gates IC88, IC89, and IC90, as well as the circuits associated with transistors Q17 through Q24. The circuit consisting of transistors Q11 through Q16 is a memory-data protection circuit that disables the predriver circuits during power-up and power-down.

The predriver input signals are:

a. *L12+ and L12–* Address bit 12 selects the first or second 4K stack of an 8K memory increment. L12– high selects the first 4K stack (4K-A). L12+ high selects the second 4K stack (4K-B).

b. *RWT1–and RWT2–* Timing signals for the X/Y read/write driver-switch circuits.

c. *RST–* Timing signal for the X and Y read sink circuits.

d. *WST–* Timing signal for the X and Y write sink circuits.

The eight predriver outputs (A, B, C, D, E, F, H, and K) provide currents for transformers in the driver- and sink-switch circuits (sheets 17 and 18) as follows:

a. *Output A* is activated (Q17 conducts) when RWT1- is low and L12– is high. The A output goes to a group of eight positive-drive driver switches that are connected to the X and Y lines of a 4K-A stack. During the reading sequence, one of these switches routes current through an X line. During the writing sequence, the same driver switch routes current through a Y line.

b. *Output B* is activated (Q21 conducts) when RWT2- is low and L12– is high. The B output goes to a group of eight negative-drive driver switches that are connected to the X and Y lines of a 4K-A stack. During the reading sequence, one of these switches routes current through a Y line. During the writing sequence, same driver switch routes current through an X line.

c. *Output C* is activated (Q22 conducts) when RWT1- is low and L12+ is high. The C output goes to a group of eight positive-drive driver switches that are connected to the X and Y lines of a 4K-B stack. During the reading sequence, one of these switches routes current through an X line. During the writing sequence, the same driver switch routes current through a Y line.

d. *Output D* is activated (Q18 conducts) when RWT2- is low and L12+ is high. The D output goes to a group of eight negative-drive driver switches that are connected to the X and Y lines of a 4K-B stack. During the reading sequence, one of these switches routes current through a Y line. During the write portion, the same driver switch routes current through an X line.

e. *Outputs E and F* are activated (Q20 and Q24 conduct) when WST – is low.

The E output goes to a group of eight sink switches that are connected to the X lines of the 4K-A and 4K-B stacks. During the writing sequence, one of these switches routes current through an X line of the selected stack.

The F output goes to a group of eight sink switches that are connected to the Y lines of the 4K-A and 4K-B stacks. During the writing sequence, one of these switches routes current through a Y line of the selected stack.

f. *Outputs H and K* are activated (Q19 and Q23 conduct) when RST – is low.

The H output goes to a group of eight sink switches that are connected to the X lines of the 4K-A and 4K-B stacks. During the reading sequence, one of these switches routes current through an X line of the selected stack.

The K output goes to a group of eight sink switches that are connected to the Y lines of the 4K-A and 4K-B stacks. During the reading sequence, one of these switches routes current through a Y line of the selected stack.

4.5.7 Driver/Sink Switches

The 16 driver/sink switch pairs provide X and Y currents for two 4K memory stacks. This is done by timesharing read/write driver switch pairs for the X and Y lines, and making the X and Y sink-switch pairs common to both 4K memory stacks. On sheets 17 and 18 of the logic diagram, the driver switches are designated circuits 1 through 4 and the sink switches 5 through 8.

The driver switches comprise:

a. *Circuit 1,* eight positive-drive, common-anode driver switches for the 4K-A stack. Positive-drive means that the collectors of the switches are connected to the positive current source. Common-anode means that the emitter of each switch is connected to the anodes of two groups of diodes in the 4K-A stack. One group consists of eight X-line diodes, the other of eight Y-line diodes. Circuit 1 is enabled when RWT1- is low and L12– is high. During the reading sequence, one of these switches routes current through an X line. During the writing sequence, the same switch routes current through a Y line.

b. *Circuit 2,* eight positive-drive, common-anode driver switches for the 4K-B stack. The collectors of these switches are connected to the same positive current source used by circuit 1. Each emitter is connected to the anodes of the two groups of diodes in the 4K-B stack. Circuit 2 is enabled when RWT1 – is low and L12+ is high. During both reading and writing sequences, the selected circuit 2 driver switch routes current through the X and Y lines in the same manner as that of circuit 1.

c. *Circuit 3,* eight negative-drive, common-cathode driver switches for the 4K-A stack. Negative-drive means that the emitters of the switches are connected to the negative current source. Common-cathode means that the collector of each switch is connected to the cathodes of two groups of diodes in the 4K-A stack. One group consists of eight X-line diodes, the other of eight Y-line diodes. Circuit 3 is enabled when RWT2- is low and L12– is high. During the reading sequence, one of these switches routes current through a Y line. During the writing sequence, the same switch routes current through an X line.

d. *Circuit 4,* eight negative-drive, common-cathode driver switches for the 4K-B stack. The emitters of these switches are connected to the same negative current source used by circuit 3. Each collector is connected to the cathodes of the two groups of diodes in the 4K-B stack. Circuit 4 is enabled when RWT2 – is low and L12+ is high. During both reading and writing sequences, the selected circuit 4 driver switch routes current through the X and Y lines in the same manner as that of circuit 3.

The sink switches comprise:

a. *Circuit 5,* eight Y write/sink switches for the 4K-A or 4K-B stacks. The emitters of these switches are connected to –12 volts. Circuit 5 is enabled when WST- is low to allow the selected sink switch to route writing current through a Y line of the 4K-A or 4K-B stack.

b. *Circuit 6,* eight X read/sink switches for the 4K-A or 4K-B stacks. The emitters of these switches are connected to –12 volts. Circuit 6 is enabled when RST- is low to allow the selected sink switch to route reading current through an X line of the 4K-A or 4K-B stack.

c. *Circuit 7,* eight Y read/sink switches for the 4K-A or 4K-B stacks. The collectors of these switches are connected to +12 volts. Circuit 7 is enabled when RST- is low to allow the selected sink switch to route reading current through a Y line of the 4K-A or 4K-B stack.

d. *Circuit 8,* eight X write/sink switches for the 4K-A or 4K-B stacks. The collectors of these switches are connected to +12 volts. Circuit 8 is enabled when WST- is low to allow the selected sink switch to route writing current through an X line of the 4K-A or 4K-B stack.

Address bits 0 through 11 are decoded in four groups of three bits each. L00X+ through L05X are multiplexed to select one of eight X-read/X-write driver-switch pairs and one of eight Y-read/Y-write driver-switch pairs. L06X+ through L08X+ select one of eight X-read/X-write sink switch pairs, and L09X+ through L11X+ select one of eight Y-read/Y-write sink switch pairs. Through the diode-decoding matrix on the memory stack card, the eight pairs of XY driver switches and eight pairs of X sink switches select one of 64 X lines. The same eight pairs of XY driver switches and 8 pairs of Y sink switches select one of 64 Y lines. The addressed word is at the intersection of the X and Y lines.

DRIVER SWITCHES. Schematics of the driver-switch circuits are on sheets 13 and 14 of the logic diagram. Circuits 1 and 2 have input signals consisting of:

a. Transformer drive current from the driver/sink-switch timing circuits (outputs A or C) that is applied to one end of the transformer primaries via pin 17.

b. Decoded signals PD0 through PD7 that are applied to the other ends of the transformer primaries via pins 1 through 8.

One of the eight driver switches is activated when the transformer drive current is present at pin 17, and one of the decoded signals goes low. This allows current to flow in the transformer, turning on the associated transistor. With the transistor on, the positive current source (pin 18) goes through the Y line during a writing sequence, and through the X line during reading sequence. Circuit 1 is used for the 4K-A stack and circuit 2 for the 4K-B stack.

Circuits 3 and 4 have input signals consisting of:

a. Transformer driver current from the driver/sink-switch timing circuits (outputs B or D) that is applied to one end of the transformer primaries via pin 17.

b. Decoded signals ND0 through ND7 that are applied to the other ends of the transformer primaries via pins 1 through 8.

One of the eight driver switches is activated in the same manner as for circuits 1 and 2. When a transistor in circuit 3 or 4 turns on, the negative current source (pin 18) goes through the X line during a writing sequence and through the Y line during a reading sequence. Circuit 3 is used for the 4K-A stack and circuit 4 for the 4K-B stack.

SINK SWITCHES. Like the driver switches, the input signals of the sink switches (sheets 15 and 16) consists of transformer drive currents (at pin 17) and decoded signals (at pins 1 through 8). A particular sink switch is activated in the same manner as a driver switch. When a transistor in circuit 5 turns on, a path is provided to sink the writing current of a Y line in the 4K-A or 4K-B stack, a transistor in circuit 6 provides a path to sink the reading current of an X line in the 4K-A or 4K-B stack, one in circuit 7 provides a path to sink the reading current of a Y line in the 4K-A or 4K-B stack, and a transistor in circuit 8 sinks the writing current of an X line in the 4K-A or 4K-B stack.

4.5.8 Current Sources

The current-source circuits are illustrated on sheet 20 of the logic diagram. The positive current source is shown on the upper half of the sheet and the negative current source on the lower.

The positive current-source circuit is passive in that power transistors Q3 and Q5 conduct only when driver/sink switches are active. With Q3 and Q5 conducting, drive current flows from the +20.6V supply, through Q3, Q5, and L1 to point L. The current at point L, nominally 400 milliamperes, goes to the positive-drive driver switches (circuits 1 and 2, on sheet 17). Transistors Q4 and Q6, zener diodes CR13 and CR15 and thermistor RT1 form a temperature-compensating network that causes the drive current to vary inversely with temperature. This compensates for the varying current required to change the state of the core with changes in temperature (more current is required as the temperature decreases, and less as temperature increases). As temperature increases, the resistance of the thermistor decreases. This causes more current to flow through the temperature-compensating network, resulting in lower drive current.

Except for the direction of current flow, the negative current-source circuit operates in the same manner. The drive current produced at point M, a nominal negative 400 milliamperes, goes to the negative-drive driver switches (circuits 3 and 4 on sheet 17.

The positive and negative drive currents are adjusted for optimum memory operation at the factory using potentiometers R47 and R49.

4.5.9 Data Register

The 16-bit (or optional 18 bit) data register (sheets 23 through 27) accepts incoming (write) data from the requesting port, and outgoing (read) data from the sense amplifiers. The memory data word consists of two 8-bit bytes: bits 0 through 7 are the right byte, and bits 8 through 15 are the left byte. (Optional bits 16 and 17 are parity bits for the left and right bytes, respectively).

During a clear/write operation, write data (MYDXnn -) are routed through multiplexing gates by the appropriate data-input enabling signal DIENxx. On the negative clock transition (DRCLK +), the register flip-flops apply the data to input gates of the inhibiting drivers.

During a read/restore operation, read data from the sense amplifiers are collector-ORed into the data-register flip-flops. The data are then transferred through line drivers by a data-output enabling signal DOENxx and placed on the bidirectional memory data bus as MYDxnn -.

4.5.10 Sense/Inhibit Timing

The sense/inhibit timing circuit (sheet 7) provides timing signals SASxx+ and INHTxx+ for the sense amplifiers and inhibiting drivers of the 4K-A or 4K-B stacks.

During a read/restore operation, sense-amplifier strobe signals are generated independently for left and right bytes. During read/restore and clear/write operations, inhibiting timing signals are generated simultaneously for left and right bytes. A low L12+ applied to the sense/inhibit timing circuit selects the 4K-A stack, and a low L12 - selects the 4K-B stack.

4.5.11 Sense/Inhibit Circuits

The sense/inhibit circuits (sheets 21 through 27, circuits 9 through 17) consist of 32 sense amplifiers and 32 inhibiting drivers, referred to as 32 pairs. Each pair is associated with a sense/inhibit line on the two 4K stacks to form a sense/inhibit loop for a single bit (figure 4-17).

The sense amplifier senses the state of the core by comparing the sense-line voltage with a predetermined threshold voltage. During a read/restore operation, the output of the sense amplifier is strobed by a sense-amplifier strobe and collector-ORed into the data register. During a clear/write operation, no such strobe is generated and data from the requesting port is clocked into the data register.

The inhibiting drivers, controlled by sense/inhibit timing, (section 4.5.10) receive data from the data register during the writing sequence to provide inhibiting current for a data bit of one (MYDxnn - low). For a data bit of zero, there is no such inhibiting current (MYDxnn - high).

In this memory system, the logical zero and one designations for the cores are reversed from those used for the memory data bus. For example, when a core in the one state is read from memory, the resulting data bit on the memory bus is a logical zero (MYDxnn - high). Conversely, a logical one data bit (MYDxnn - low) written into memory produces a core in the zero state.

READ/RESTORE DATA-LOOP OPERATION. During a read/restore operation, the sense amplifier of circuit 16 (sheet 26) senses the state of the bit-15 core by comparing the voltage on sense lines S15A - and S15A (pins 19 and 20) with a predetermined threshold voltage. The sense-amplifier threshold voltage (approximately 20 millivolts) is the result of applying a reference voltage SASTHA (pin 11) to the sense-amplifier resistor network. The output of the sense amplifier is strobed by the sense-amplifier strobe signal SASAL +, and collector-ORed into the data register.

When the bit-15 core is in the one state, the sense amplifier produces a high signal that is strobed with a high SASAL + (figure 4-17). The resulting low bit-15 signal is collector-ORed into the data register and inverted by a line driver to become a logical-zero bit 15 on the memory data bus (MYDA15- high). The low bit-15 signal also prevents the bit 15 inhibiting driver from turning on. Thus, during restoring, the write currents on the X and Y lines restore the core to the original state (one).

When the bit-15 core is in the zero state, the sense amplifier produces a low signal. This causes the bit-15 signal to remain high. During restoring, the high bit-15 signal is gated with INHTAL + to produce a low signal that turns on the bit-15 inhibiting driver. The resulting inhibiting current prevents the current on the X and Y lines from switching the bit-15 core to a one state.

CLEAR/WRITE DATA-LOOP OPERATION. During a clear/write operation, a high read/write control signal (MWxxx +) is sent to the timing-control circuit, preventing

SASR – and SASL – from being generated, thus disabling the sense amplifier so that the data register output is not altered. The high read/write control also produces a high DIENxx + that enables input data to be clocked into the data register. Furthermore, during the clear/write operation, a high DOENx + enables input data to be gated through line drivers back to the memory bus.

During the writing sequence, the state of the bit-15 signal is determined by the bit-15 flip-flop in the memory data register. If bit 15 (MYDA15 –) is a one, a high bit-15 signal is gated with INHTAL + to turn on the bit-15 inhibiting driver. Inhibiting current is thus generated, allowing the bit-15 core to remain in the zero state (a zero-state core represents a one-state data bit). If bit 15 (MYDA15 –) is a zero, a low bit-15 signal prevents the bit-15 inhibiting driver from generating the inhibiting current. The write currents on the X and Y lines set the bit-15 core to a one state (a one-state core represents a zero-state data bit).

4.5.12 Voltage Regulators

The memory PC card contains two voltage regulators (sheet 7) that provide -5 and + 12V dc. The regulator containing a 5.1-volt zener diode converts the -12V dc power source to -5V dc that is used by the sense amplifiers. The other regulator, which contains a 12-volt zener diode and an emitter follower, converts the + 20.6V dc power source to + 12V dc that is used by the inhibiting predrivers and the XY predriver circuits.

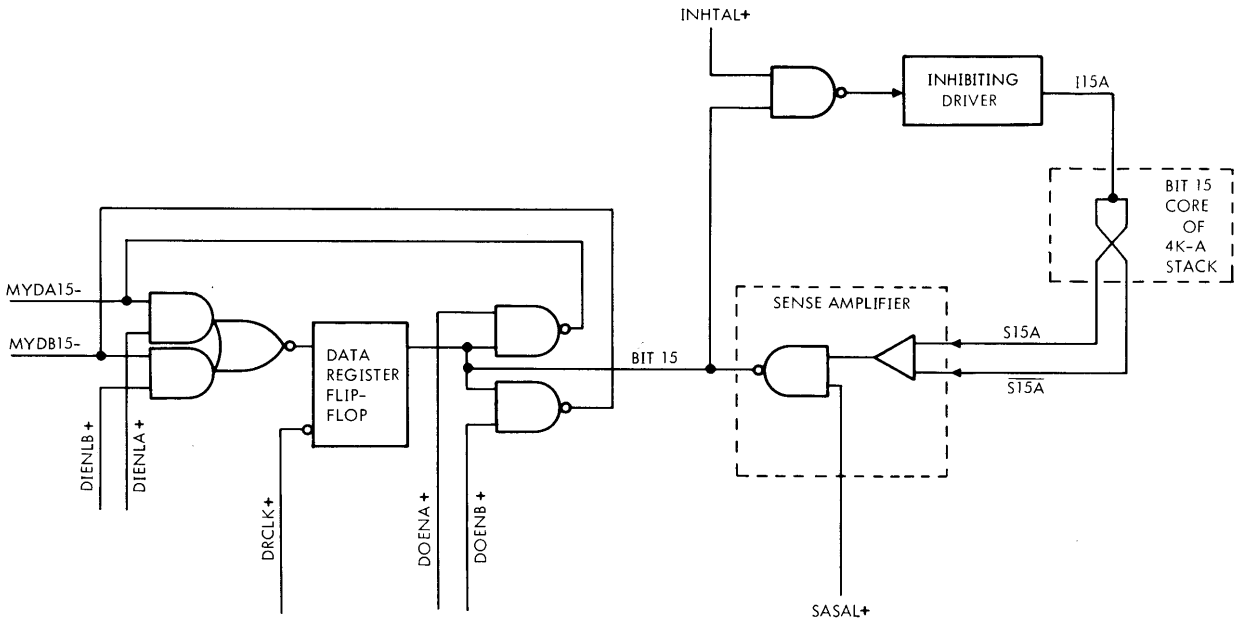


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Figure 4-17. Sense/Inhibit Data Loop for Bit 15

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting memory troubleshooting. The Varian MAINTAIN II test program system (Test Programs Manual, 98 A 9952 06x) contains a memory test program used to isolate a malfunction to a particular 8K memory module. Determine which memory board is at fault and move it to the top slot for troubleshooting. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for core-memory maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit and current probe (P6022), or equivalent.

b. Multimeter, Triplett type 630 or equivalent.

c. Soldering iron, 15-watt pencil type.

5.2 CIRCUIT BOARD REPAIR

The memory module is contained on a three-layer PC board. The two outer layers provide signal interconnections for the circuit components. The inner layer provides low-impedance ground and power-voltage distribution.

If it has been determined that circuit-board repair is required, it is recommended that the Varian Data Machines customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, extreme caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits.

5.3 DC VOLTAGES

Ensure that the dc voltages applied to the memory module are within 5 percent of their nominal values by measuring them at the following pins of connector P1 on the memory PC card:

+20.6 volts at pin 2
-12 volts at pin 3
+5 volts at pin 6

5.4 MEMORY ADJUSTMENTS

Each memory module contains three potentiometers that are adjusted at the factory for optimum memory operation. Readjustment is not normally required and should not be attempted except by factory-trained personnel. Potentiometer R22 adjusts the pulse width of a one-shot circuit that determines the memory cycle time. Potentiometers R47 and R49, which are in the current source circuits, adjust the positive and negative drive currents.

5.5 SIGNAL WAVEFORMS

As a troubleshooting convenience, the memory PC card contains test points at critical points throughout the memory circuits. The test point locations are shown on the PC card assembly drawing (44E0613) and logic diagram (volume 2). Typical waveforms at various test points are illustrated in figure 5-1. The sense-amplifier strobe signals (SASxx+) are generated only during a read/restore operation (MWRxYx+ low). Figure 5-2 shows current pulses produced by the positive and negative current source circuits. The pulses are monitored on the PC card at the current loops connected to L1 and L2.

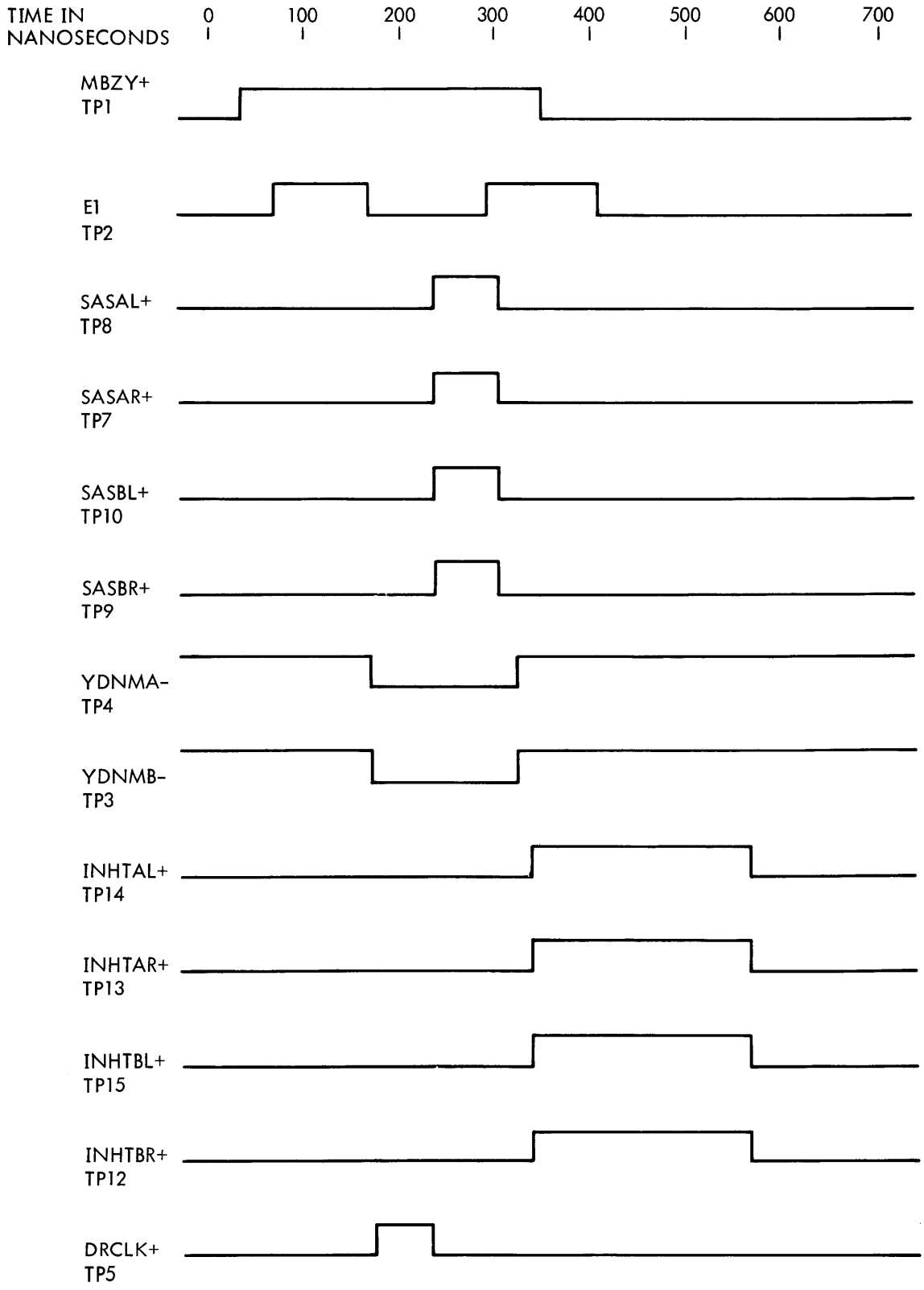

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Figure 5-1. Test Point Waveforms

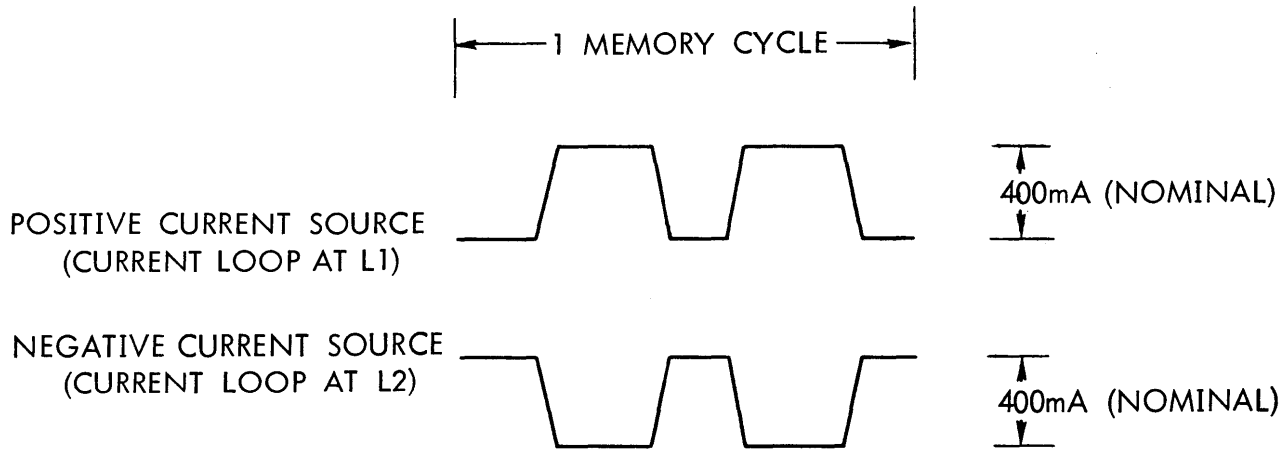

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Figure 5-2. Current-Source Waveforms

SECTION 6
MNEMONICS

This section presents alphabetized lists of memory mnemonics and their definitions. Table 6-1 contains external mnemonics, and table 6-2 internal mnemonics.

Table 6-1. External Memory Mnemonics

Mnemonic	Description
MHGY -	Port-B priority modifier (Inhibits port A).
MHMY -	An optional priority modifier that inhibits port B.
MRQYA -	Memory start request for port A.
MRQYB -	Memory start request for port B.
MWLYA +	Read/write control for left byte of port A. A high level produces a clear/write operation.
MWLYB +	Read/write control for left byte of port B. A high level produces a clear/write operation.
MWRYA +	Read/write control for right byte of port A. A high level produces a clear/write operation.
MWRYB +	Read/write control for right byte of port B. A high level produces a clear/write operation.
MYAA00 + through MYAA15 +	Memory address bits for port A.
MYAB00 + through MYAB15 +	Memory address bits for port B.
MYDA00 - through MYDA17 -	Memory input or output data for port A (bits 16 and 17 are optional parity bits).
MYDB00 - through MYDB17 -	Memory input or output data for port B (bits 16 and 17 are optional parity bits).
SRST -	System reset (disables memory during power-up and power-down).
YDNMA -	Memory acknowledgment from port A (memory cycle in progress on port A).
YDNMB -	Memory acknowledgment from port B (memory cycle in progress port B).

Table 6-2 Internal Memory Mnemonics

Mnemonic	Description
APEN +	A port enabled
APDEC –	A port decoded
APRT –	A-port selection signal
ARCLK +	Address-register clock
BPDEC –	B port decoded
BPEN +	B port enabled
BPRT –	B-port selection signal
CA0A to CA7A	Common-anode drive A (from X write or Y read driver switches for 4K-A cores)
CA0B to CA7B	Common-anode drive B (from X write or Y read driver switches for 4K-B cores)
CC0A to CC7A	Common-cathode drive A (from X read or Y write driver switches for 4K-A cores)
CC0B to CC7B	Common-cathode drive B (from X read or Y write driver switches for 4K-B cores)
DIENLA	Enable data input for left byte of port A.
DIENLB	Enable data input for left byte of port B.
DIENRA	Enable data input for right byte of port A.
DIENRB	Enable data input for right byte of port B.
DOENLA	Enable data output for left byte of port A.
DOENLB	Enable data output for left byte of port B.
DOENRA	Enable data output for right byte of port A.
DOENRB	Enable data output for right byte of port B.
DRCLK	Data-register clock.
DXS0 through DXS7	Decoded X sink (decoded signals from address bits 6, 7, and 8).
DYS0 through DYS7	Decoded Y sink (decoded signals from address bits 9, 10, and 11).
E1	Input pulse to the memory delay line.
E2 through E26	Output taps of the memory delay line.

Table 6-2 Internal Memory Mnemonics continued

Mnemonic	Description
INHT –	Inhibiting timing.
INHTAL +	Inhibiting timing for 4K-A stack, left byte.
INHTAR +	Inhibiting timing for 4K-A stack, right byte.
INHTBL +	Inhibiting timing for 4K-B stack, left byte.
INHTBR +	Inhibiting timing for 4K-B stack, right byte.
I00A through I15A	Output bits 0 through 15 of inhibiting drivers for 4K-A stack.
I00B through I15B	Output bits 0 through 15 of inhibiting drivers for 4K-B stack.
L00 + through L12 +	Output bits 0 through 12 of memory-address register.
MA10A + through MA12A +	Buffered memory-address bits from the port-A module-address decoder.
MA10B + through MA12B +	Buffered memory-address bits from the port-B module-address decoder.
ND0 to ND7	Negative-drive decoded (decoded signals from multiplexed address bits 0 through 5 sent to the negative-drive driver switches).
PD0 to PD7	Positive-drive decoded (decoded signals from multiplexed address bits 0 through 5 sent to the positive-drive driver switches).
MMYAB00 +	Modified memory-address bit 0.
R –	Read pulse
RST –	Read sink timing
RWT1 –	Read/write timing
RWT2 –	Read/write timing 2
SASAL +	Sense amplifier strobe for 4K-A stack, left byte.

Table 6-2 Internal Memory Mnemonics continued

Mnemonic	Description
SASAR +	Sense amplifier strobe for 4K-A stack, right byte.
SASBL +	Sense amplifier strobe for 4K-B stack, left byte.
SASBR +	Sense amplifier strobe for 4K-B stack, right byte.
SASL –	Sense amplifier strobe for timing for left byte.
SASR –	Sense amplifier strobe timing for right byte.
SASTHA	Reference voltage that produces the threshold voltage for sense amplifiers of the 4K-A stack.
SASTHB	Reference voltage that produces the threshold voltage for sense amplifiers of the 4K-B stack.
S00A through S15A	Input bits 0 through 15 of sense amplifiers for 4K-A stack.
S00B through S15B	Input bits 0 through 15 of sense amplifiers for 4K-B stack.
TEND –	End timing for A and B port entry.
WST –	Write sink timing
XS0A through XS7A	X sink A (from X read or X write sink-switches to a 4K-A stack)
XS0B through XS7B	X sink B (from X read or X write sink-switches to a 4K-B stack)
YS0A through YS7A	Y sink A (from Y read or Y write sink-switches to a 4K-A stack)
YS0B through YS7B	Y sink B (from Y read or Y write sink-switches to a 4K-B stack)