VARIAN 70 SERIES
SEMICONDUCTOR MEMORY

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varian data machines/a varian subsidiary

98 A 9906 041

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SECTION 1
GENERAL DESCRIPTION

The **Varian 70 Series Semiconductor Memory Manual** describes the memory and its interface with a Varian 70 series computer.

The manual is divided into six sections:

- Introduction to the memory and its relation to the system
- Installation and interface information
- Operation
- Theory of operation
- Maintenance
- Mnemonics list

There is also a Volume 2 to this manual. Volume 2 is assembled when the hardware is shipped, and reflects the configuration of a specific system. It contains engineering documents, such as logic and installation drawings.

This expandable, random-access, metal oxide semiconductor (MOS) memory has an internal cycle time of 330 nanoseconds.

The basic memory module has 8,192 (8K) words of 16 or 18 bits each. The semiconductor memory is expandable to 65,536 (64K) words by use of eight 8K word modules.

The standard 16-bit word contains two 8-bit bytes that can, in some systems, be manipulated independently. The optional 18-bit word provides a parity bit for each byte. Unless otherwise specified, further references in this manual are to 16-bit words.

The dual-port memory has two independent sets of I/O terminals for simultaneous access to different memory modules from different sources, e.g., main and peripheral processors. Port B has a higher access priority than port A. Furthermore, port B can obtain continuous access by locking out port A with a priority-modification signal (MHGY −, section 4), or port A can obtain such access with MHMY −. The latter signal is an optional feature.

The semiconductor memory is volatile and loses data if power is removed. During short-term power loss an optional, battery-powered data saver (Power Supply Manual, 98 A 9906 06x) activates and provides the appropriate voltages to power the memory refresh logic on each memory module.

In systems containing both a core memory (Core Memory Manual, 98 A 9906 03x) and a semiconductor memory, the latter is normally assigned the lower address area. However, in special applications semiconductor memory can be located above or between core-memory areas. Jumpers adjust the boundaries of the memory areas (module address).

Table 1-1 lists the specifications of the semiconductor memory.

Table 1-1. Semiconductor-Memory Specifications

Parameter	Specification
Speed (address lines must be stable 12 nanoseconds before leading edge of the start pulse)	Cycle time: 330 nanoseconds maximum Access time: 260 nanoseconds maximum
Logic levels (CPU bus)	True: -0.4 to +0.8V dc False: +2.4 to +5.0V dc
Address and control lines	Unidirectional
Data lines	Bidirectional
Word length	16-bit words containing two 8-bit bytes (optional 18-bit words have a parity bit for each byte)

(continued)

GENERAL DESCRIPTION

Parameter	Specification
Capacity	8,192 (8K) to 65,536 (64K) words in increments of 8K words
Dimensions	Each 8K increment on a PC board 15.6 by 19 by 0.587 inches (39.6 by 48.3 by 1.49 cm)
Interconnection	Over very short signal paths to the processor via one 132-pin connector
Priority	Port B has priority over port A to the dual-port memory (a priority-modifier permits complete disabling of port A, or port B, the latter being an optional signal)

Power

Full-rate Cycling

	8K	16K	32K
	(Values in amperes)		
+23.0V dc (Memory)	0.15	0.30	0.60
+20.0V dc (Memory)	3.0	6.0	9.50
+5.0V dc (Logic)	0.7	1.4	2.8
+5.25V dc (Memory)	1.0	2.0	4.0

The normal current requirements shown are for memory systems in which two modules at a time are operating, one module per port.

Data Saver (Optional)

	8K	16K	32K
	(Values in amperes)		
+22.5V dc (Memory)	0.01	0.02	0.05
+19.5V dc (Memory)	0.06	0.12	0.24
+5.2V dc (Memory)	0.10	0.20	0.40

Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation
Forced-air cooling	For each 3W dc power, one cubic foot of air per minute applied crosswise above and below each memory module

The following manuals are additional aids in understanding the Varian 70 series computers.

Title	Manual Number
System Handbook	98 A 9906 01x
Processor Manual	98 A 9906 02x
Core Memory Manual	98 A 9906 03x
Option Board Manual	98 A 9906 05x
Power Supply Manual	98 A 9906 06x

SECTION 2
INSTALLATION

2.1 INSPECTION

The semiconductor memory has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. Ascertain that wires and cables are neither loose nor broken, and that hardware is secure. If damage exists:

a. Notify the transportation company.

b. Notify Varian Data Machines.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

Each 8K increment of the semiconductor memory is on a standard mainframe multilayer printed circuit (PC) board approximately 15.6 by 19 by 0.587 inches (39.6 by 48.3 by 1.49 cm). The maximum component height is 0.4 inch (1.02 cm). Figure 2-1 is a block diagram of a single memory module, and figure 2-2 is a block diagram of an expanded memory system.

The memory storage arrays are packaged in 22-pin dual-in-line chips with ceramic or plastic cases. On each 8K memory board there are 128 such chips.

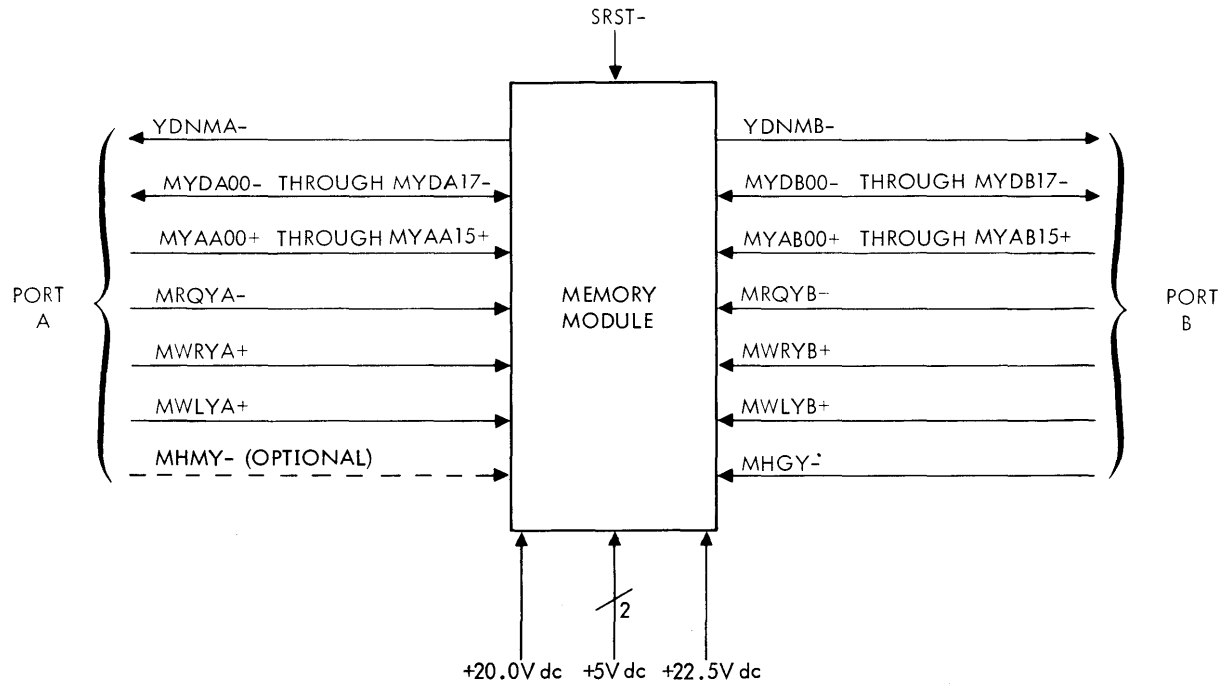

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Figure 2-1. Memory Module Block Diagram

INSTALLATION

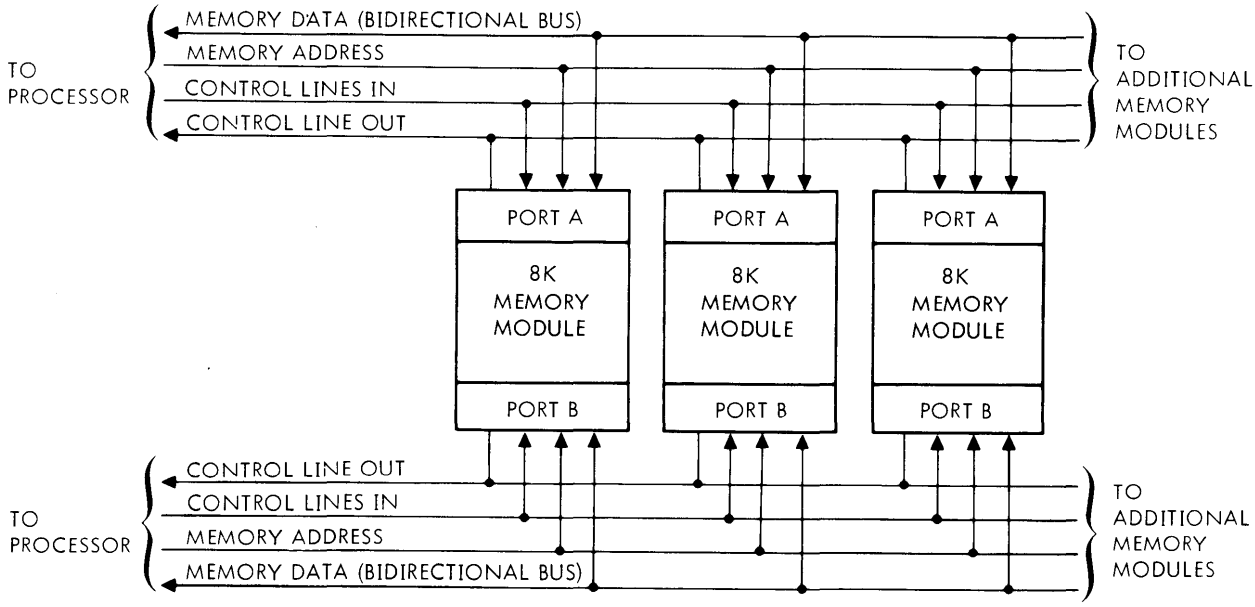

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Figure 2-2. Expanded-Memory Block Diagram

2.3 ADDRESS-JUMPER CONNECTIONS

Each memory module is assigned a module address determined by jumper connections on the PC board. These connections are normally made at the factory.

Jumper assignments are given in table 2-1 for modules in various 8K sections of memory. The vertical column under a module address lists the address bits to be connected for that module. Except in special applications, address jumper assignments for ports A and B are identical.

ADDR INPUT SELECTIONS \ MEMORY MODULE ADDR	0-7K	8-15K	16-23K	24-31K	32-39K	40-47K	48-55K	56-63K
A10	H	H	H	H	H	H	H	H
A11	H	H	H	H	H	H	H	H
A12	H	H	H	H	H	H	H	H
A13	$\overline{13}$	13	$\overline{13}$	13	$\overline{13}$	13	$\overline{13}$	13
A14	$\overline{14}$	$\overline{14}$	14	14	$\overline{14}$	$\overline{14}$	14	14
A15	$\overline{15}$	$\overline{15}$	$\overline{15}$	$\overline{15}$	15	15	15	15

NOTE: H = NO CONNECTION (HIGH)

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Table 2-1. Addressing Jumper Configuration

2.4 INTERCONNECTION

The data, address, and control signals pass between memory and the processor over a multilayer PC backplane through rear PC connectors (P01). Power is supplied to the boards via these connectors. The bus structure has up to eight 8K memory modules on line at a given time.

The memory interface is transistor transistor logic (TTL) compatible (figure 2-3). Address and control lines are unidirectional, and data lines are bidirectional. Each memory decodes 16 address lines, 3 of which select the memory module (8K capacity) and 13 of which contain the address of the word within that module. Only one module is active on a given port at one time. However, since the ports are independent, two modules can be active simultaneously, one on each port. No spurious signals are generated by the nonactive memory modules.

The pin assignments for the connector on the semiconductor memory board are provided in logic diagram 91C0397 (Volume 2).

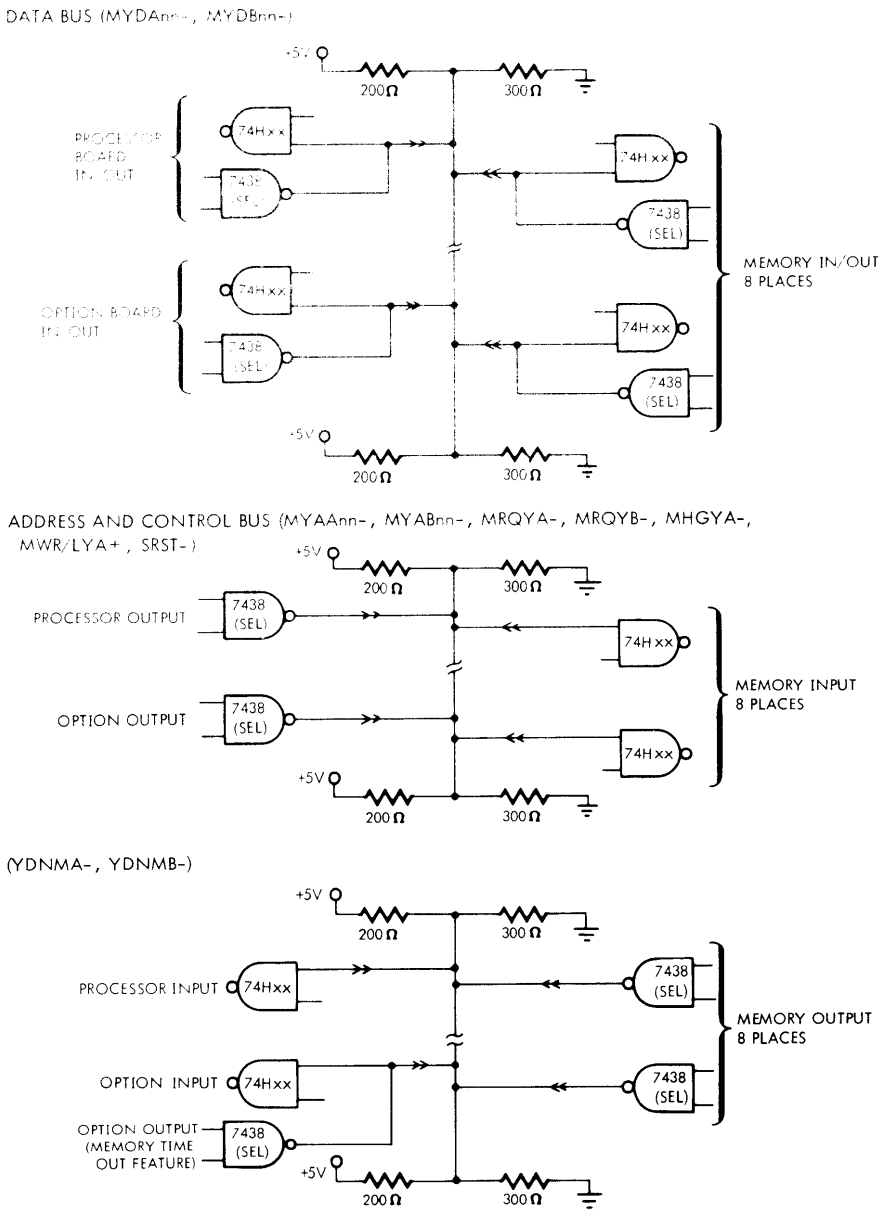

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Figure 2-3. Memory Interface Schematic

SECTION 3
OPERATION

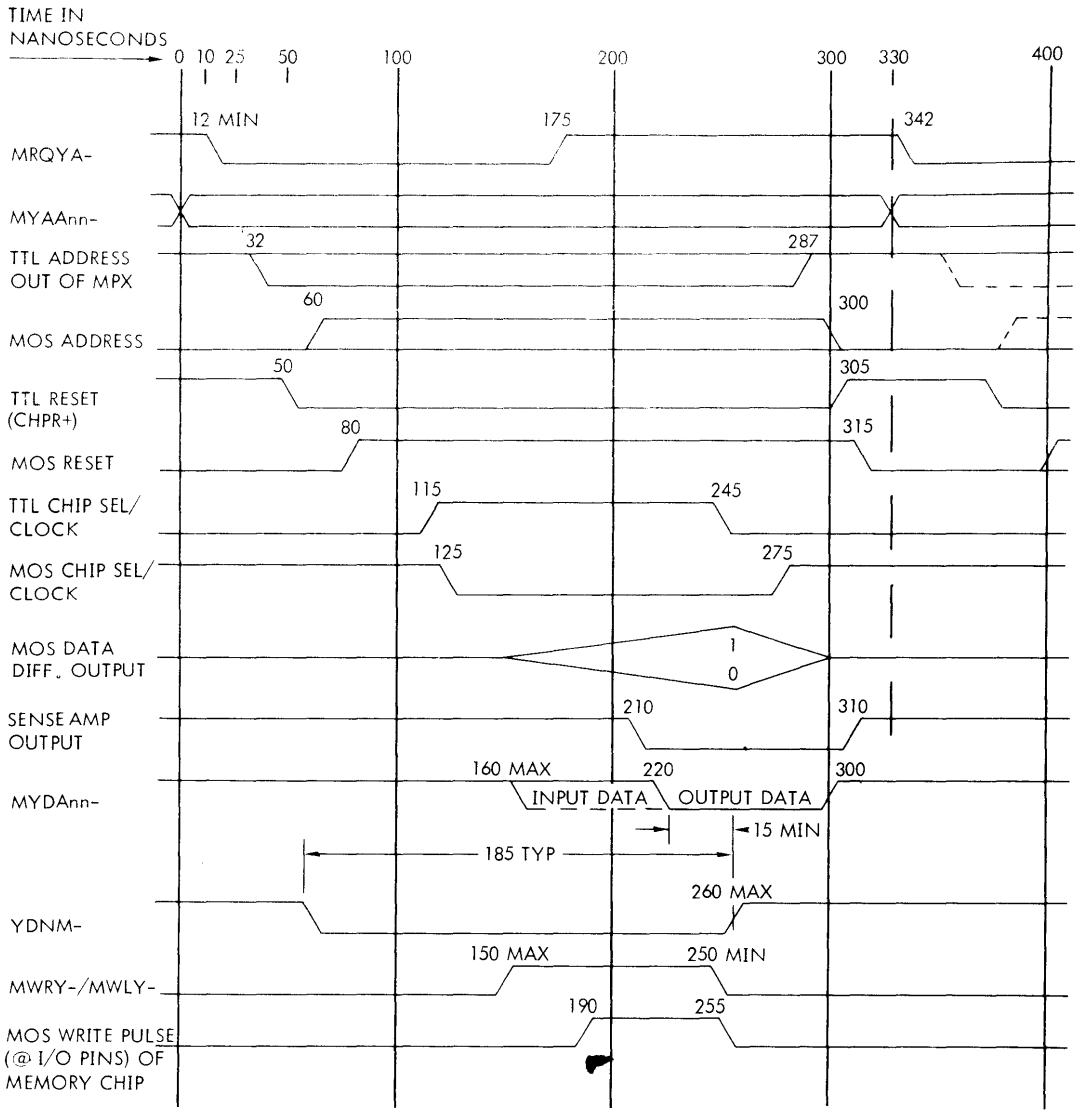
There are no operating controls or indicators on the semiconductor memory board.

SECTION 4
THEORY OF OPERATION

Section 4.1 explains a typical timing sequence and section 4.2 is a detailed block-diagram description. Refer to the timing diagram (figure 4-1) and the logics (Volume 2) as aids to following the theory of operations. TTL signals have high levels near +5V dc, whereas metal-oxide semiconductor (MOS) signals have highs near +19V dc.

4.1 TYPICAL TIMING SEQUENCE

The memory cycle is started by the falling edge of request line MRQYA – or MRQYB –. This means that the addresses have been stable for at least 12 nanoseconds, the refresher cycle (periodic recharging of the MOS memory cells) priority is not active (DSD+ low), and port A is not inhibited (MHGY – low). Once priority is resolved, the first falling edge of either (MRQYA – or MRQYB – begins the timing sequence with a pusle on the delay line. If, for example, port A is selected (APRI – low), the other priority signals (BPRI – and RFFPRI –) are inhibited until the completion of the port-A memory sequence.



NOTE: TIMES ARE RELATIVE TO STABLE ADDRESS AT MEMORY CONNECTOR, MEASURED @ 50% POINT

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Figure 4-1. Typical Timing Sequence

THEORY OF OPERATION

This first event terminates reset by forcing CHPR + low (TTL signal) and MOS RESET high. About fifty nanoseconds later the clock and chip-selection lines go low (MOS signal). After a 90-nanosecond delay from the falling edge of the MOS chip SEL/CLOCK the data appear at the memory IC output. This output is amplified and gated to the data bus (MYDxnn–) of the enabled port by a signal generated only in a reading sequence.

The memory announces that data are coming by lowering YDNM – 170 nanoseconds before data become stable at the output. YDNM – is 185 nanoseconds wide (typical). The rising (trailing) edge is used as a strobe to latch data into the processor data register.

In a writing sequence, the signal MWRY + or MWLY + is received by memory not later than 138 nanoseconds after the leading edge of MRQYA –. The memory writes full or half words, as commanded. Bytes not written into retain their previous data.

4.2 BLOCK DIAGRAM DESCRIPTION

The functional blocks (figure 4-2) of the semiconductor memory are discussed in detail in the following subsections.

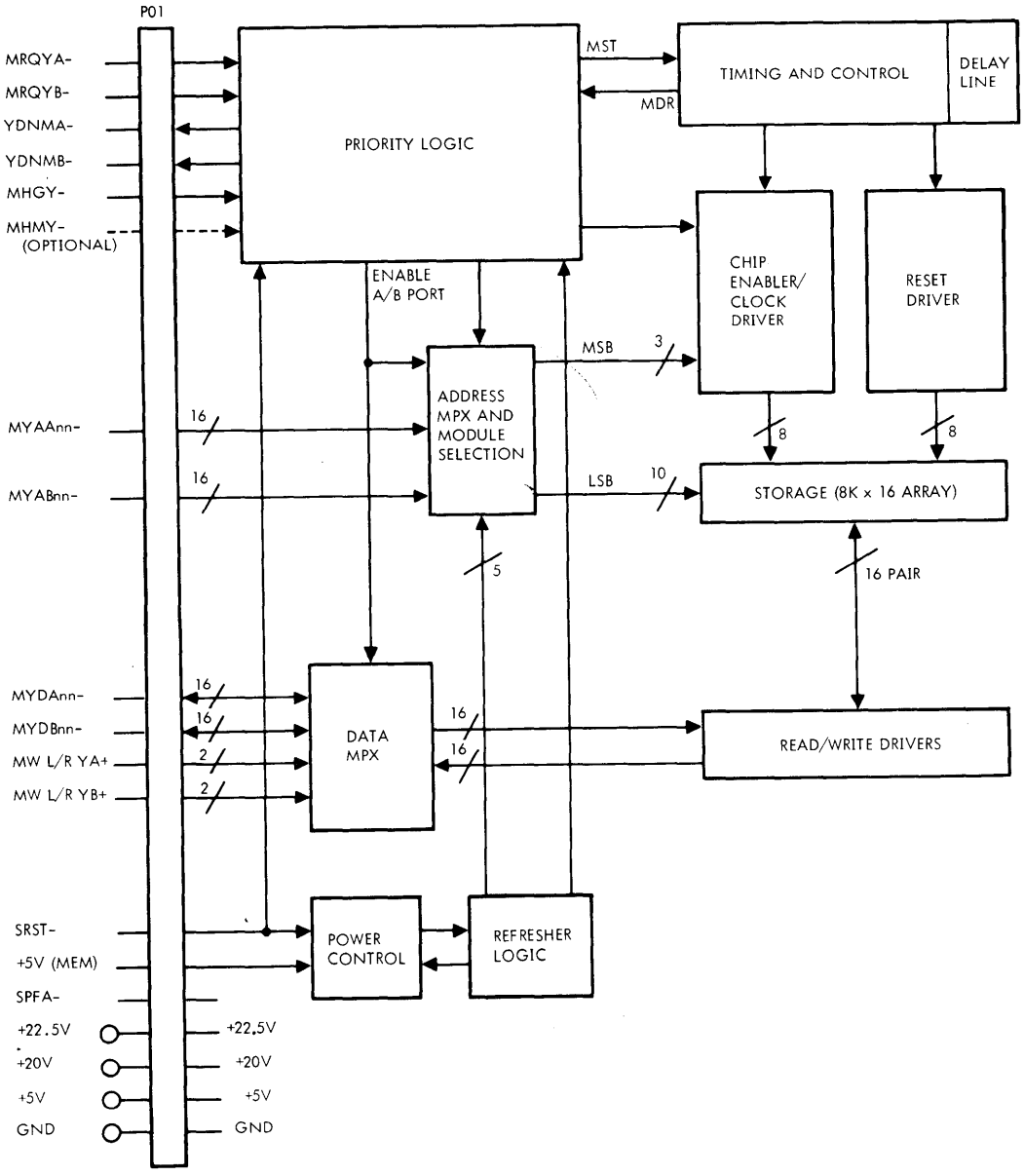

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Figure 4-2. MOS Memory Block Diagram

4.2.1 Priority Logic

The priority logic processes the memory start request signals MRQYA – and MRQYB –, examines the module signals MYAx10 – through MYAx15 –, monitors the A-port inhibitor (MHGY –), and initiates a memory cycle if appropriate. Both ports A and B can be serviced simultaneously provided they address different memory modules. Otherwise, continuous requests on port B (the priority port) inhibit port A from being serviced. If the port-A inhibitor (MHGY –) is active, port A is denied access to memory in all cases. Refresher requests are generated approximately every 60 microseconds and override both normal port access and the port-A inhibitor. If the optional port-B inhibitior (MHMY –) is present, there is an analogous sequence on that port.

4.2.2 Timing and Control

The memory timing sequence (figure 4-1) is initiated by a delay line. After this initial delay to establish priority and the address range, a pulse is initiated on the delay line. The memory-event sequencing is controlled by outputs from various taps along the line. Precise timing intervals are obtained by using combinations of taps, decoder logic, and flip flops. The refresher interval is timed by an independent loop using a one-shot as the timing element.

4.2.3 Address Multiplexor and Module Selection

The address multiplexor routes the address information to the memory elements from the three address sources (port A, port B, and refresher control). Ports A and B each supply a 16-bit address (MYAx00– through MYAx15–) and the refresher control logic supplies a five-bit module address RA00 through RA04).

The address muliplexor gates are a combination of AND/OR logic elements that are enabled when APEN+ or BPEN+ go high. The selected address is then ANDed and the driver signals A00 through A09 sent to the particular memory elements. The timing diagram of figure 4-1 shows a multiplexor address-out activity of approximately 330 nanoseconds.

The memory-module selection logic use bits MYAx13 through MYAx15 to select one of eight 8K modules, and bits MYAx10 through MYAx12 to select 1K within the selected module.

4.2.4 Data Multiplexor

The data multiplexor routes incoming (write) data signals MYDx00– through MYDx15–, from either port A or port B to the storage section via the write drivers and I/O bus (section 4.2.7). The data-multiplexor gates are a combination of AND/OR logic elements like the address multiplexor (section 4.2.3) and are enabled by APEN or BPEN signals. The output data go into the write driver.

The outgoing (read) data coming from the storage section via the I/O bus and read amplifiers (section 4.2.10) are enabled to the requesting port by the DOEN signals.

4.2.5 Refresher Logic

This logic provides signals RA00 through RA04 that refresh the memory approximately once every millisecond. Refreshing is done on a cycle-stealing basis in which one address group out of 32 is refreshed approximately every 3 microseconds. Burst refreshing (32 cycles every millisecond without breaks between cycles) is not done under normal operation because the latency time (11 microseconds) is too long for real-time I/O operation, e.g., with a disc or drum. However, burst refreshing is used when the control panel power switch is in the HOLD position, or during a power failure (data saver, WPR– and WPL– high) because of its efficient use of power due to reduced frequency of power switching. The refresher logic includes a counter that generates the 32 required addresses. It also generates on/off signals to the power control logic (section 2.4.6).

The refresh logic is started, when power is first turned on, by the circuit C12, R23, IC58, and C16 triggering one shot IC51. After voltage +5M has come up, capacitor C12 has charged up to the threshold level of IC58. This causes the output (pin 8) to go low (0 volts) causing a high to low transition on pin 1 of IC71. Pins 3, 4, and 5 are high at this time, allowing the one shot to be triggered.

NOTE: When the power switch on the control panel is turned to OFF, 30 seconds must elapse before turning the switch to hold or on to allow the memory refresh to start again.

4.2.6 Power Control

The internal power control switches the power inputs on and off. This allows the memory to remain in the low-power data-saver mode. DSRF– (data saver Refresher–) from the refresher logic activates the power outputs during the 11-microseconds of data-saver mode in 1-millisecond intervals. Upon restoration of power, the 1-millisecond burst sequence goes to completion before normal refreshing resumes.

4.2.7 Storage Section

The storage section is an array of 8 by 16 MOS integrated-circuit memory elements containing 1024 bits each. The storage is dynamic and needs periodic refreshing (sections 4.2.5, 4.2.6, and Appendix A). The storage is read nondestructively, i.e., no restoration cycle is required after reading, thus making cycle and access times almost equal. The storage elements are driven by MOS signals and have differential output signals at about 100 microamperes. These output signals are compared by the sense amplifier, which provides the read data. At the input to the sense amplifier the one and zero outputs are of opposite polarity, making the signal-to-noise ratio very high.

4.2.8 Reset Driver

The eight reset-driver signals RESET0 through RESET7 are active (low) between memory cycles to supply power to the entire memory array and provide the fastest possible access time. The reset drivers are enabled by CHPR + going high. Thus, the address decoder portion of the memory IC is always enabled when memory is not cycling. Decoding the address and transferring it into memory storage occurs within 40 nanoseconds of the reset rising edge (figure 4-1).

4.2.9 Chip Enabler/Clock Driver

The eight chip-enabler/clock-driver circuits power the portion (1K by 16 bits) of memory that transfers I/O data to the storage array and enables part of the address decoder with a chip-selection timing signal (CST +). To decode to 1K address, each of the eight drivers powers a 1K by 16 bit array and is accessed by receiving one of the input signals CHPSC0 through CHPSC7. During refreshing, all chips are refreshed simultaneously and all eight enabler/clock lines are pulsed for approximately 150 nanoseconds (between 125 and 275 nanoseconds of the MOS chip selection/clock, figure 4-1).

4.2.10 Read/Write Drivers

A typical two-bit input (write) driver and associated circuitry converts information from the bidirectional data bus of the requesting port to the MOS level required by the inputs to memory. The drivers are sectored to provide half-word or byte storage (8 bits). The two halves of the word (designated R or L) are stored according to the state of the two control lines (WPR + or WPL +) of the requesting port. These lines are gated with the active (low equals logical one) data signal (MYDAnn or B) and driven by the sense-amplifier bit drivers to the memory. The input data is enabled (low) for approximatley 80 nanoseconds (figure 4-1).

A typical output (read) driver and associated circuitry contains the 16 sense amplifiers that detect the one and zero signals from the storage element. Both time and amplitude discrimination are used. The sense signal has a differential output current that translates the ones and zeros into opposite polarities. The sense-amplifier output is the logical AND between a correct polarity input for a one and the DOEN timed strobe. The AND gates are enabled by DOENR/L. Since there is no data register in the semiconductor memory system, the output pulse from memory to the data line is determined by the width of the above signals. Note the relationship of MOS data out (figure 4-1) to sense amplifier out and output data.

4.2.11 System Reset

The system reset (SRST-) from the processor enables the power control one-shot and also activates the power down start (PDNS +) and certain gates in the refresher logic. The memory is then in burst-refresher mode with a period (2 milliseconds maximum) determined by the one-shot.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting troubleshooting. The Varian MAINTAIN II test program system (Test Programs Manual 98 A 9952 06x) contains a test program (p/n 92 A 0107 02x) used to isolate a malfunction to a particular 8K memory module. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following test equipment and tools are recommended for semiconductor-memory maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent

b. Multimeter, Triplett type 630 or equivalent

c. Soldering iron, 45-watt pencil type

5.2 MAINTENANCE PROCEDURES

Memory failures can be indicated by the repeated occurrence of the halt instruction or the completely random sequencing of instructions. Run the memory test until one of the above symptoms or other errors occurs. Determine which memory board is at fault and move it to the top slot for troubleshooting. On each memory board are a number of test points designated TP, followed by a number. There are also a set of delay-line taps, designated E, and arranged in the order (starting from the tap nearest TP15) E14, E1, E15, E2, E16, E3... Delay-line taps are jumpered at the factory and should be changed only by VDM customer-service engineers.

Use the theory of operation (section 4), and the logics (Volume 2) as aids in troubleshooting. Verify that the proper dc voltages are at the specified pins of connector P1 (sheet 4) and +20V dc is at TP (test point) 17. Verify that the collector of Q1 is at +8 volts.

5.2.1 General Memory Exercise Test

With the memory test program in a dynamic loop for reading and writing data and with the oscilloscope ground in TP1, 16 or 19, put the probe at TP15 or 18. This input to the delay line should show a pulse of approximately 330 nanoseconds per cycle. If there are no pulses, check APEN2+ (TP10), BPEN2+ (TP11), and CHPR+ (TP13). One of these three signals should be displayed. If not, examine the logic that generates these signals (sheets 9 and 6) and look for faulty gates or bad solder connections. If the above checks out, continue with the following checks.

Place the probe on CST+ (TP14) to verify that the chip-selection timing signal is present to enable one of the eight (1K by 16 bit) selection lines. If CST+ is not present, check the delay-line taps and for a possibly faulty AND gate (IC73). If CST+ is present, continue with the following checks.

During writing, make sure the program enables bit 0 for the active port (A or B, TP7 and 8, respectively). If neither MYDA00 – nor MYDB00 – is pulsing, check the write-data logic (sheet 19). If MYDA00 – or MYDB00 – is present, continue with the test.

During reading, place the probe on DOENRA+ (TP4) or DOENRB+ (TP5) to check for the data enable read signals. If not present, examine the logic (sheet 9); if present, check for data-out on the bidirectional I/O bus (MYDA00– or MYDB00– at TP7 and 8). If DOENR is enabled but no signal is present at MYDA00– or MYDB00–, verify that there is a current change at the differential amplifier input. If none is present, check the MOS array.

5.2.2 Refresher Test (Power Loss)

To check the refresher logic, turn the power switch, on the control panel, to the hold position. Place the scope probe on TP6 (DSD+) and observe that the signal goes high for bursts every millisecond. If the system has the data-save option, simulate a power failure (trip the CB on the power supply or pull the line cord) and observe that the DSD+ signal goes high every millisecond. If it does not, check for a high at IC71 pin 5 and IC77 pin 1. Also check to see the +5M power supply output is on continually.

5.2.3 Refresher Test (Power On)

To check the refresher logic, turn the power switch, on the control panel, to the on position. Place the scope probe on TP6 (DSD+) and observe that the signal goes high every 30 to 60 microseconds (without memory reguests to port A and B). If not, check for a high at TP9 (REN+) and also check the timing of one shot IC54 (TP12).

5.2.4 Troubleshooting Data Errors

The ICs comprising the memory array are arranged on the PC board so that data errors can be readily isolated to the faulty IC. Figure 5-1 shows the IC layout of a 16-bit 8K memory array. Each column of ICs is 1024 16-bit words of memory. From right to left, the IC columns comprise memory increments 1K through 8K, respectively. Each IC in a column contains 1024 1-bit memory cells. From top to bottom, the ICs comprise bit 0 through 15, respectively. Each IC designation indicates the 1K increment and bit

that the IC comprises. For example, IC215 indicates bit 15 of the second 1K increment. Thus, a data error consisting of bit 15 of a word in the second 1K increment can be corrected by replacing IC215.

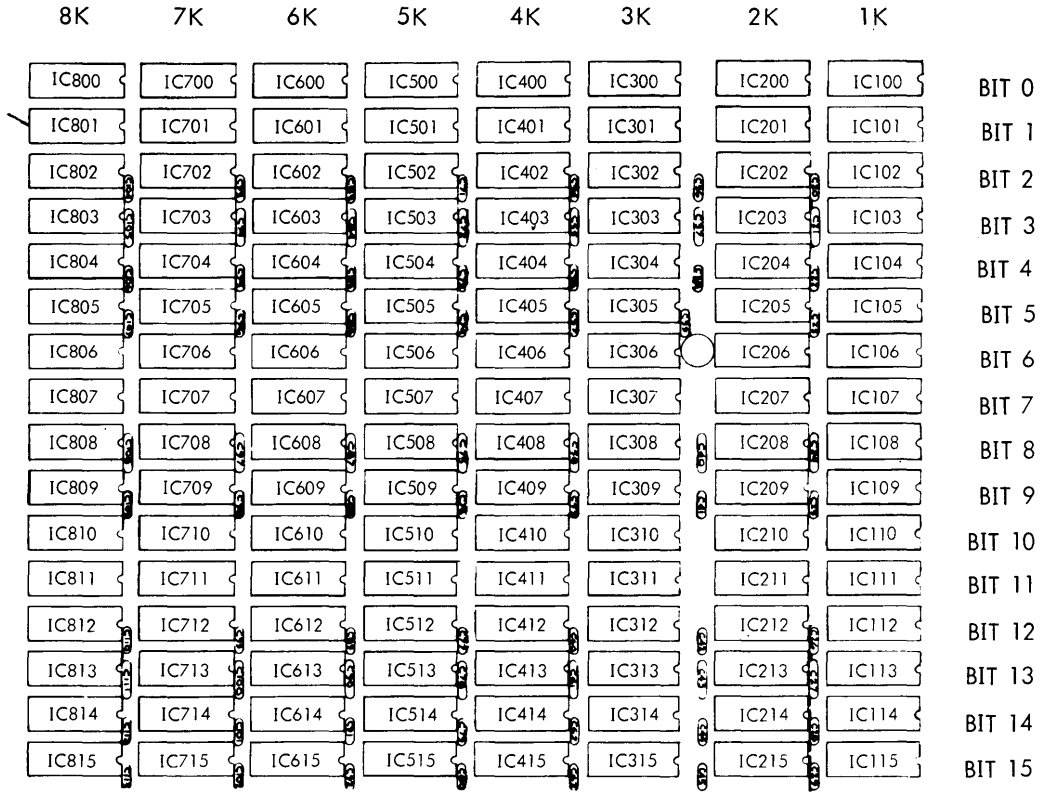

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Figure 5-1. IC Layout of 16-Bit 8K Array

SECTION 6
MNEMONICS

Mnemonic	Description
A00A A00B A01A A01B A02A A02B A03A A03B A04A A04B A05A A05B A06A A06B A07A A07B A08A A08B A09A A09B	Ten drivers from each of the A and B ports that route address information to the memory elements
A10 through A12	Module address selection
APEN1	Address enabler for port A
APEN2	Address and data enabler for port A
APRI-	Port A priority
BPEN1	Address enabler for port B
BPEN2	Address and data enabler for port B
BPRI-	Port B priority
CHPR+	Chip reset control for reset driver logic
CHPSC0 CHPSC1 CHPSC2 CHPSC3 CHPSC4 CHPSC5 CHPSC6 CHPSC7	Eight chip-selection lines (each handles 1K by 16-bit words)
CST	Chip-selection timing signal that enables CS0 through CS7
DOENLA	Data-out enabler left for port A
DOENLB	Data-out enabler left for port B

MNEMONICS

Mnemonic	Description
DOENRA	Data-out enabler right for port A
DOENRB	Data-out enabler right for port B
DS +	Data Saver power
DS −	
DSD +	Data Saver power delay
DSD −	
DSR −	Data Saver power reset
MHGY −	Port B priority modifier (inhibits port A)
MHMY −	Memory map priority
MRQYA −	Memory start request for port A
MRQYB −	Memory start request for port B
MWLYA +	Read/write control for left byte of port A
MWLYB +	Read/write control for left byte of port B
MWRYA +	Read/write control for right byte of port A
MWRYB +	Read/write control for right byte of port B
MYAA00 +	Memory address bits for port A and port B
MYAB00 +	
MYAA01 +	
MYAB01 +	
MYAA02 +	
MYAB02 +	
MYAA03 +	
MYAB03 +	
MYAA04 +	
MYAB04 +	
MYAA05 +	
MYAB05 +	
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MYAA09 +	
MYAB09 +	
MYAA10 +	
MYAB10 +	
MYAA11 +	
MYAB11 +	
MYAA12 +	
MYAB12 +	
MYAA13 +	
MYAB13 +	
MYAA14 +	
MYAB14 +	
MYAA15 +	
MYAB15 +	
MYDA00 −	Memory input or output data for port A and
MYDB00 −	port B (bits 16 and 17 are optional parity bits)
MYDA01 −	

Mnemonic	Description
MYDB01 –	
MYDA02 –	
MYDB02 –	
MYDA03 –	
MYDB03 –	
MYDA04 –	
MYDB04 –	
MYDA05 –	
MYDB05 –	
MYDA06 –	
MYDB06 –	
MYDA07 –	
MYDB07 –	
MYDA08 –	
MYDB08 –	
MYDA09 –	
MYDB09 –	
MYDA10 –	
MYDB10 –	
MYDA11 –	
MYDB11 –	
MYDA12 –	
MYDB12 –	
MYDA13 –	
MYDB13 –	
MYDA14 –	
MYDB14 –	
MYDA15 –	
MYDB15 –	
MYDA16 –	
MYDB16 –	
MYDA17 –	
MYDB17 –	
PDNS +	Power down start (from refresher logic)
RA00	Refresher address counter
RA01	
RA02	
RA03	
RA04	
READL	Read input left to sense amp strobe left
READR	Read input right to sense amp strobe right
REFPRI –	Refresher priority (enables refresher counter)
REN	Enable refresher
RESET0	Eight reset drivers (power the address decoder)
RESET1	
RESET2	
RESET3	
RESET4	
RESET5	
RESET6	
RESET7	
RESET +	Reset interval
RESET –	

MNEMONICS

Mnemonic	Description
SRST –	System reset (from CPU power supply)
WPL	Write pulse left
WPR	Write pulse right
YDNMA – YDNMB –	Memory acknowledgment from port A Memory acknowledgment from port B

APPENDIX A
MOS CELL OPERATION

The AMS 6002, used here for illustration, is one of several elements that can be used. The storage element in the AMS 6002 is the four-transistor cell shown in figure A-1. (The transistors connected at A and B are not part of the cell). The operation of the cell is straightforward. The cell is selected by taking the clock input to VDD and is a dc stable flip-flop at that time. When the clock is at VSS the cell does not conduct and information is stored on one of the parasitic capacitors.

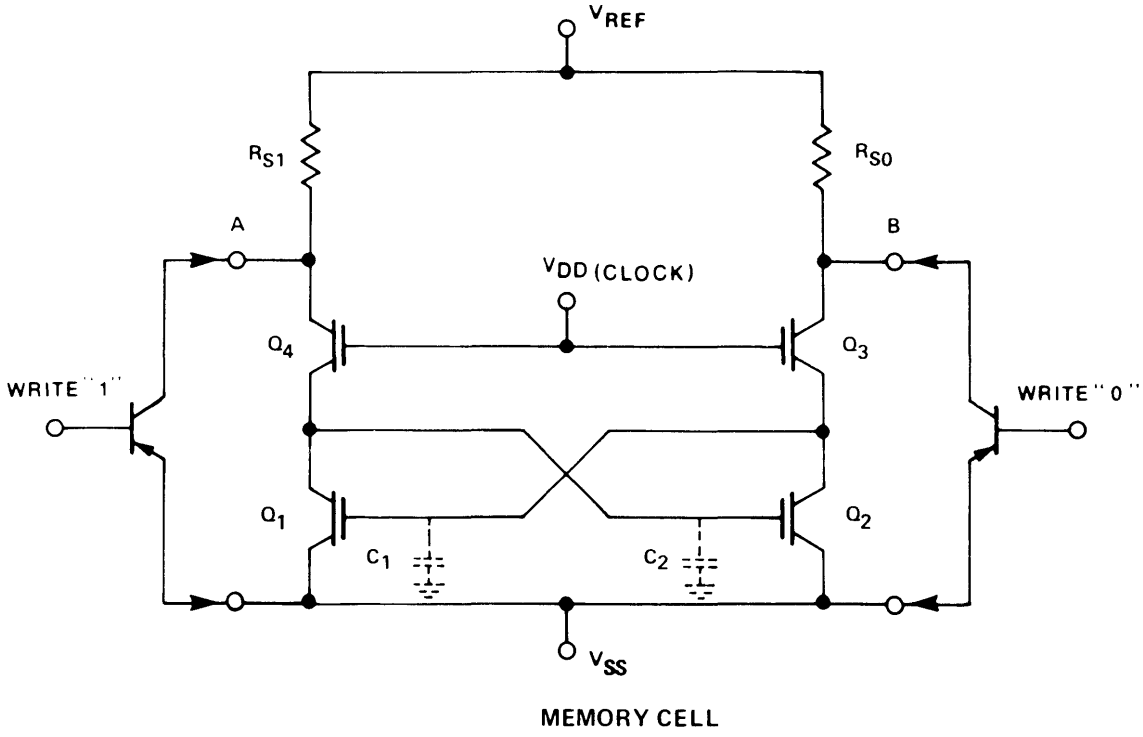

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Figure A-1. Memory Cell

Writing data into the cell is simply executed with a pair of switches such as the transistors attached at A and B. If the write " 1" transistor is turned on A closes to VSS. This shuts off any conduction that may have been occurring in Q_2 . At the same time the capacitor C_1 is charged and Q_1 begins to conduct current. When the cell is selected for a subsequent reading operation, current is available in the Q_1 , Q4, and RS_1 side of the cell, and a differential amplifier between A and B would sense the voltage difference and detect the presence of a " 1" .

To understand how the cell is integrated into a 1024 array, consider the block diagram in figure A-2 and the timing information in figures A-3 and A-4. The reset input in the low state: (1) precharges the device and (2) turns off all address inverters. On the 6002 the address inputs are the drain of the MOS device, and because they are off during the reset period very low input capacitances are seen.

Address inputs can be changed prior to reset going low, provided that the previous cycle is complete. However, the input capacitances are greater at that time.

MOS CELL OPERATION

After the reset input is taken high, there is a delay for the row and column decoders to function (TDD in the timing diagrams). The clock and chip-selection periods occur next, with the clock input gating the row decoder while the chip-selection input enables the column decoders. Information from the selected cell is then transferred to the I/O lines, which are also gated by the chip-selection input. After the output data has been sensed, the clock and chip-selector return to the positive state and the device is ready for the next cycle.

In the 6002, the row-decoder output is tied to the clock (VDD) input of the cell in figure A-1. Thus, whenever a row is selected all 32 cells are stable. This selection refreshes those 32 cells regardless of the state of the chip-selection input. In order to refresh the 1024 bits, all 32 rows must be selected by using all 32 combinations of the A_0 through A_4 addresses.

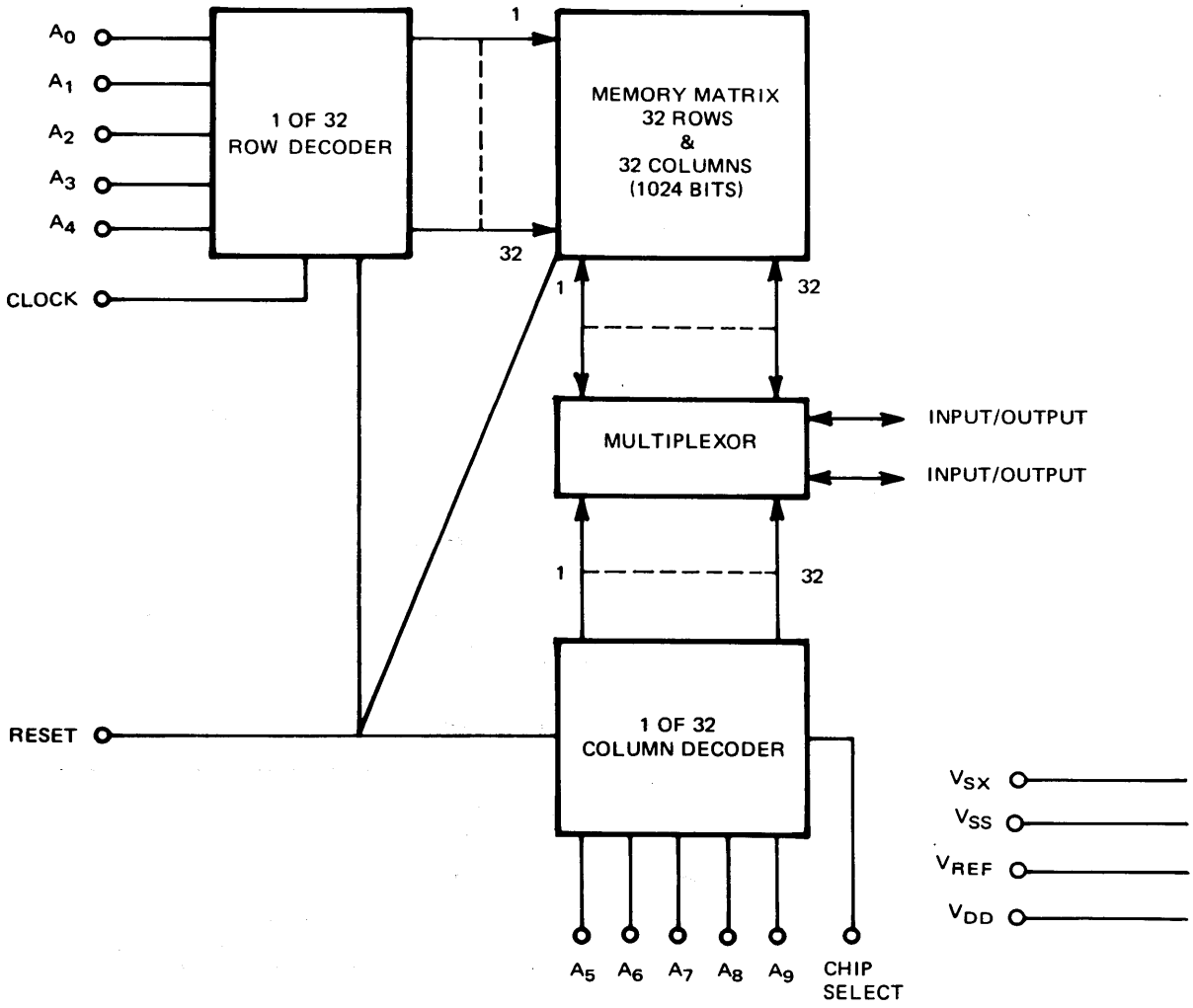

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Figure A-2. AMS 6002 Block Diagram

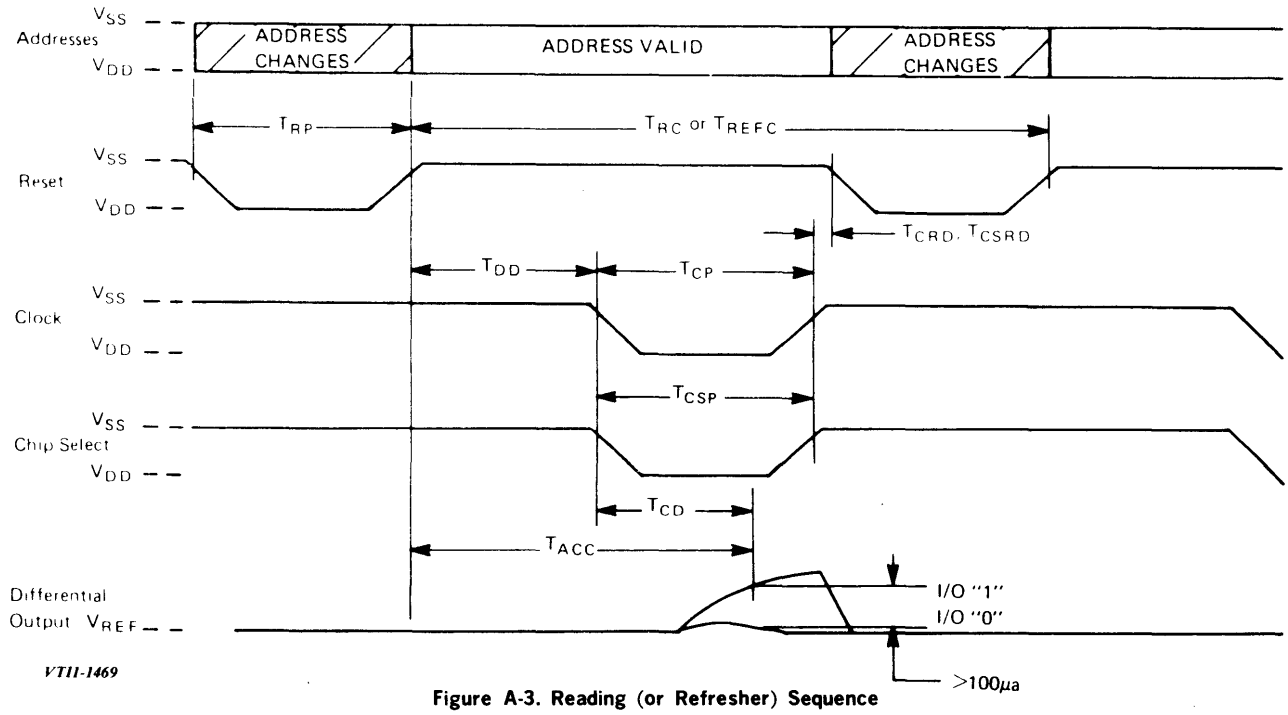

Figure A-3. Reading (or Refresher) Sequence

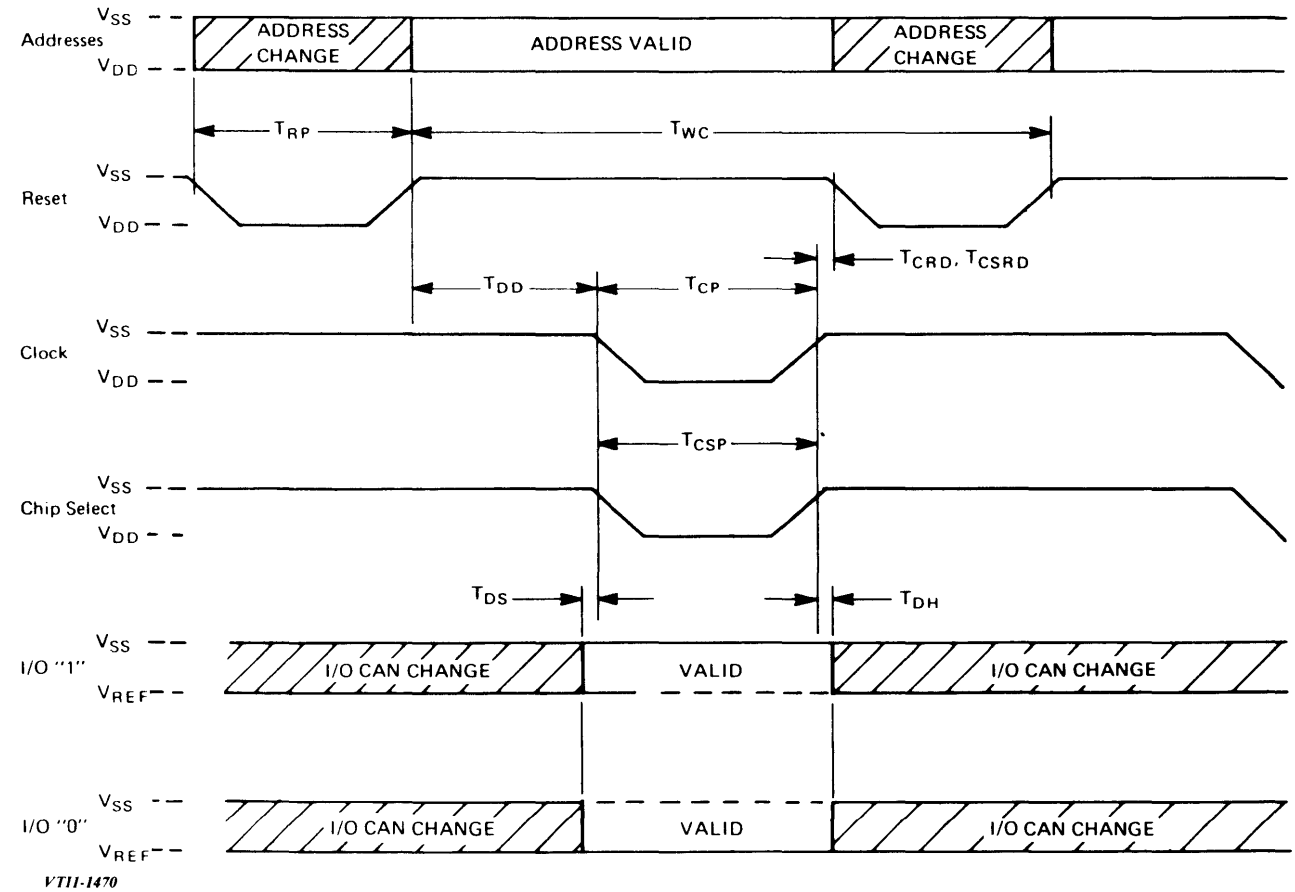

Figure A-4. Writing Sequence

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