



varian data machines / a varian subsidiary

VARIAN
73/620 TEST PROGRAMS
MANUAL



VARIAN 73/620 SYSTEMS TEST PROGRAMS

Specifications Subject to Change Without Notice



varian data machines / a varian subsidiary
2722 michelson drive / irvine, california 92664
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This manual describes the MAINTAIN II test-program system for verifying the correct operation and detecting and isolating malfunctions in Varian computer systems.

The reader should be familiar with the instruction set of the system for which he uses these programs and some assembly-language programming. The person who runs these tests should also know the operating procedures for the control panel and peripheral devices on his system.

The organization of this manual is based on the organization of the test system. The first chapter presents an overview of the entire system. The following chapters present the components of the system. In a chapter for a specific component the reader finds an overview in more detail and a definition of the minimal hardware necessary for using the component, a description of its design and structure, followed by the information needed to use the test in the order needed: first the preliminary procedures such as loading and setting sense switches, then the execution procedures, followed by an explanation of any error indication that may occur during execution or cause termination, and finally examples of the program input and output.

RELATED DOCUMENTATION

The computer handbook provides data about capabilities and use as well as a brief guide to the other software for the system. The maintenance manuals are provided for every computer and each of the internal options and peripheral controllers. These manuals include information about the operation, installation, and maintenance.

VARIAN 73 SYSTEM

Throughout this manual references to the 620/f computer apply to the Varian 73 computer unless otherwise noted. Appendix A is a tabular comparison of console operation between the Varian 73 and 620/f systems. A separate test program for the 73 system writable control store (WCS) is discussed in the system maintenance manual.

GENERAL OPERATING DESCRIPTIONS

In this manual references to the instruction register designate the I register of the 620/f and the U register on other 620-series computers. Similarly, references to START on the 620/f are the same as RUN on other systems. RESET is SYSTEM RESET on 620 computers except the 620/f which is RESET. The applicable system handbook gives detailed descriptions of control-panel switches and indicators and general operating procedures.



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SECTION 1

SYSTEM OVERVIEW

The **Varian 620 MAINTAIN II Test Program System** is a system approach to testing and maintaining Varian 620-series computers, internal options, and peripherals. MAINTAIN II provides an effective and uniform interface between the computer and the user.

The test programs in this manual cover only the computers and internal options. Refer to the Bibliography for a list of Software Performance Specifications (SPS) covering peripheral test programs that operate in the MAINTAIN II Test Program System.

The test programs are to be used in conjunction with the maintenance manuals for the system, which include theory of operation installation, and maintenance information.

The MAINTAIN II system programs are designed to verify correct system operation, including internal instructions, memory, internal computer options, and peripherals and their controllers. Malfunctions can be isolated to a specific area of the system and corrected.

1.1 STRUCTURE

The MAINTAIN II system consists of the following elements (figure 1-1):

- a. Test executive program, which includes preliminary instruction and memory tests, binary loader, and test executive
- b. Instructions test program
- c. Memory test program
- d. Teletype (TTY) test program
- e. Internal computer option test programs
- f. Peripheral test programs

The test executive program:

- a. Loads test program tapes
- b. Accepts control directives and parameters from the user
- c. Executes test programs
- d. Contains a utility package, consisting of aids for debugging, program maintenance, and hardware troubleshooting
- e. Includes standard test program subroutines, i.e., TTY input/output, time delay, memory size determination, SENSE switch option, etc.

The preliminary instructions test portion of the executive test program validates basic CPU operation, the preliminary memory test checks basic functions of the first 4K memory module, and the binary loader reads binary data and stores it in memory.

The memory test program verifies correct operation of memory. It is applicable to both 16- and 18-bit systems with from 4,096- to 32,768-word memories.

The instructions test program tests and verifies execution of internal, I/O, and optional instructions.

The TTY test program verifies correct operation of the Varian-modified 33/35 ASR TTY unit.

The internal computer option test programs individually test each option to ensure correct operation.

The peripheral test programs verify correct operation of associated system peripherals (i.e., line printer, disc, paper tape system, etc.) and their controllers.

1.2 MAINTENANCE CONCEPTS

MAINTAIN II minimizes maintenance time for the 620-series computers. The programs can be executed when the computer is off-line and not transferring data or performing control functions.

MAINTAIN II test programs are normally on punched paper tape; other media, such as object card decks, are available. The programs exercise the computer, internal options, and peripherals and their controllers with sequences of instructions. If an instruction is improperly executed, the sequence is halted and error messages are output to indicate the failing instruction or operation. The user can then repeat, continue, or halt the program until the fault is isolated and corrected.

To correct hardware malfunctions:

- a. Isolate the fault to a functional area, such as memory, control, arithmetic/logic, operations register, input/output, or peripheral device or its controller. Eliminate the functional areas that are operating properly.
- b. Execute, repeat, or modify the applicable test program for the area of the suspected fault.
- c. Correct the fault by replacing the faulty component or circuit card and restore the system to normal operation.
- d. Verify system operation by rerunning the test program.

The maintenance manuals appropriate to the user's system describe the theory of operation of all major functional areas of the computer, internal options, and peripheral controllers. Also given are system checkout procedures using the control panel and specified electronic test equipment.

Specific operating procedures for MAINTAIN II basic computer test programs are given in the following chapters, which also include descriptions of error conditions and error messages.



1.3 BIBLIOGRAPHY

The following list covers MAINTAIN II Test Programs for current product-line peripherals.

SPS	Test Program
89A0180	Card Reader Test
89A0199	Card Punch Test
89A0247	Magnetic Tape Test

SPS	Test Program
89A0239	Moving Head Disc Test (620-35)
89A0207	Moving Head Disc Test (620-36/37)
89A0194	Drum/Fixed Head Disc Test
89A0189	Paper Tape Reader/Punch and BIC Test
89A0174	Line Printer Test
89A0228	Universal Asynchronous Serial Controller Test



SECTION 2

TEST EXECUTIVE PROGRAM

The **Test Executive Program** is the controlling factor in the MAINTAIN II test program system. In addition to loading, executing, and monitoring the other MAINTAIN II test programs, the test executive program:

- Provides utility aids for debugging, program maintenance, and hardware troubleshooting
- Includes standard subroutines for use by associated test programs, i.e., TTY I/O, time delay/time out, memory size determination, power failure/restart protection, SENSE switch options, etc.

The test executive program is designed for a minimum hardware configuration of a 620-series computer with 4K of memory (maximum, 32K) and a 33/35 ASR TTY. All system sizes can be tested, but the test programs operate in the first 4K memory module only. The test can, however, be performed in both TTY and control panel modes of operation (section 2).

The test executive object format is normally a punched paper tape that can be loaded from the TTY or high-speed paper tape reader. A punched card object deck is also available.

2.1 COMPONENTS OF THE SYSTEM

The test executive program consists of:

- Preliminary instructions test
- Preliminary memory test
- Binary loader
- Test executive

The preliminary instructions test validates central processing unit (CPU) operation by testing the machine instructions listed in table 2-1. Successful execution of this test indicates that MAINTAIN II test programs can be correctly loaded.

The preliminary memory test verifies correct operation of the first 4K of memory. Memory addresses 000000 through 007420 are tested in two passes. The first pass checks each address with a pattern of 052525; the second pass, 0125252. The original contents of memory are saved and restored by the program.

Table 2-1. Preliminary Instructions Test Summary

Mnemonic	Description
ADD	Add memory to A register
ADDI	Add immediate

Table 2-1. Preliminary Instructions Test Summary
(continued)

Mnemonic	Description
ANAI	AND immediate
DAR	Decrement A register
DBR	Decrement B register
DECR 02	Set B register to -1
DXR	Decrement X register
ERA	Exclusive-OR memory and A register
ERAI	Exclusive OR immediate
IAR	Increment A register
IBR	Increment B register
INCR 03	Set A and B registers to +1
IXR	Increment X register
JAN	Jump if A register negative
JAP	Jump if A register positive
JAZ	Jump if A register zero
JBZ	Jump if B register zero
JIF 011	Jump if A register = 0 and OVFL is set
JMP	Jump (unconditional)
JMPM	Jump and mark (unconditional)
JMP ^o	Jump indirect
JOF	Jump if overflow indicator set
JXZ	Jump if X register zero
LDA	Load A register
LDAI	Load A register immediate
LDB	Load B register
LDBI	Load B register immediate
LDX	Load X register
LDXI	Load X register immediate
LLRL	Load logical rotation left
LLSR	Long logical rotation right
LRLA	Logical rotation left A register
LSRA	Logical shift right A register
MERG 032	Transfer ORed A and B registers to B register
NOP	No operation
ORAI	Inclusive-OR immediate
ROF	Reset overflow indicator
STA	Store A register
STAI	Store A register immediate
STB	Store B register
STX	Store X register
SUB	Subtract memory from A register
TBA	Transfer B register to A register
TBX	Transfer B register to X register
TXA	Transfer X register to A register
TZA	Transfer zero to A register
TZB	Transfer zero to B register
TZX	Transfer zero to X register
XAZ	Execute if A register zero
XBZ	Execute if B register zero
XIF 022	Execute if B register = 0 and A register = ≥ 0



TEST EXECUTIVE PROGRAM

- h. Manually load the appropriate bootstrap routine in the A register:

NOTE: ABL cannot be used to load the Test Executive because the preliminary tests and loader do not load into standard ABL directed locations.

Address	Reader Code (DA = 037)
007756	102637
007757	004011*
007760	004041
007761	004446
007762	001020
007763	007772
007764	055000
007765	001010
007766	007600
007767	005144
007770	005101
007771	100537
007772	101537
007773	007756
007774	001000
007775	007772

Code (DA = 01)	
102601	CIB
004011*	ASLB
004041	LRLB
004446	LLRL
001020	JBZ
007772	Memory Address
055000	STA
001010	JAZ
007600	Memory Address
005144	IXR
005101	INCR
102601	CIB
101201	SEN
007756	Memory Address
001000	JMP
007772	Memory Address

* For the 18-bit 622/i, enter 004013.

- i. Load 007770 in the P register; 006500 in the X register; and zero in the A, B, and instruction registers.
- j. Reset REPEAT, press RESET, and, in run mode, press START or RUN.
- k. If using the TTY, set the reader lever to START/RUN.

After the preliminary tests and binary loader are read into memory, the bootstrap routine jumps to address 007600. The paper tape reader is turned off, and the preliminary instructions test automatically executed, starting at address 006500.

Following successful execution of the instructions test, the program automatically executes the preliminary memory test. The program then jumps to the binary loader, which

loads the test executive. Setting SENSE switch 3 during their execution causes the program to loop on the combined preliminary instructions and memory tests.

Preliminary test error conditions are described in section 2.2.3.

2.2.2 Operating the Test Executive

This program can be executed using the systems Teletype or directly from the computer control panel.

For Teletype operation when the test executive program is loaded and halts with 006177 in the P register, press START or RUN to begin execution. This procedure assumes that the TTY device address is 01; if it is not, load the device address in the A register and press START or RUN.

To start the test executive program manually:

- a. Clear the instruction register to zero.
- b. Load 007000 in the P register.
- c. Press RESET, and, in run mode, press START or RUN.
- d. Load the desired device address (if the TTY device address is other than 01) in the A register, and press START or RUN.

The program begins execution by outputting the message:

THIS IS THE 620 TEST EXECUTIVE

MEMORY SIZE IS nK

where n indicates memory size (for example 4 or 8, or multiples of 4). The program then waits for control statement input.

Control	Description
A	Print/change the contents of the pseudo-A register.
B	Print/change the contents of the pseudo-B register
Cx.	Print/change the contents of memory address x.
Dx.	Dump (list) memory on the Teletype printer beginning at memory address x.
Ex,y.	Generate a punched paper tape in binary format on the Teletype paper tape punch. x is the address of the first word; y, the address of the last word.

continued



TEST EXECUTIVE PROGRAM

Trap to memory address 000204, starting at address 000100; display the trap address and the contents of the A, B, and X registers:

T204,100.
(000204) 142340 002000 010405

Load and execute a test program tape:

L.
(TEST IDENTIFIER)

Transfer to and execute a test program located at address 000500:

G500.
(TEST IDENTIFIER)

Punch a paper tape in binary format beginning at address 000001 through 000006, after initializing the addresses to the desired values:

I0,7,0.
I1,6,1.
I2,5,2.
I3,4,3.
E1,6.

Punch a paper in object format:

I0,7,0.
I1,6,1.
I2,5,2.
I3,4,3.
P1,6,7.

In the two examples immediately above, the initialize memory control statement has been used to establish a specified pattern in memory for validation of the format of the resultant operation.

Terminate an erroneous control statement:

P1,6\

Cancel an octal digit and replace with the following digit:

I0,6- 7.

Detailed descriptions of loading and execution procedures of other MAINTAIN II test programs under test executive control are contained in the following chapters.

Briefly, to load a test program tape:

- Position the desired test program tape in the tape reader.
- Type L on the TTY keyboard.
- The program is loaded and a test identifier message output on the TTY printer.

Return to the beginning of a test program is normally controlled by a SENSE switch option, or after the execution of a specified number of cycles.

To return to the test executive from a test program, follow the restarting procedure described in section 2.2.1. Pressing the INT switch on the 620/f computer also returns control to the test executive; however, since some programs dynamically alter memory, refer to the applicable chapter of this manual regarding restrictions on interrupting a test in progress.

In general if a test is operating under interrupt control, the program should be terminated via sense switch 3, then use the INT switch. This precludes leaving an interrupt hanging that may cause subsequent problems.

To return to a just-executed test program from the test executive, type

Gx.

where x is the starting address of the test program (refer to the program listing supplied with the software and to the following chapters for starting addresses).

For systems that do not include a TTY or if the TTY is partially inoperative, load the test executive program using the available input device (e.g., high-speed paper tape reader or card reader). Starting the test executive with 006152 in the P register automatically sets the mode control flag for control panel mode, determines memory size, and halts the program.

To load MAINTAIN II object programs in this mode:

- Initialize the paper tape reader (TTY or high-speed).
- Position the tape at the reading station.
- Prepare the reader for on-line usage.
- Load a program-loading code in the A register, i.e., zero to load the program and halt (used if the program is to be executed without the TTY), less than zero to verify the program tape, and greater than zero to load and execute the program.
- Load 007600 in the P register.
- Press RESET.
- Press START or RUN.

Refer to the following chapters for detailed procedures for loading and executing MAINTAIN II test programs.

2.2.3 Error Indications

After the preliminary tests and binary loader are loaded, the preliminary instructions test is automatically executed beginning at address 006500. If an error is detected, the program halts with the error code in the instruction register (table 2-5).



TEST EXECUTIVE PROGRAM

the TTY or its controller is not operating properly, the program halts with 000077 in the instruction register, and the TTY output routine times out.

Refer to the applicable maintenance manual for troubleshooting and correction procedures, or continue test program execution in control panel mode.

If an illegal control statement is input, the test executive outputs the message:

INVALID

Correctly reinput the erroneous statement.

During TTY input activity or while the TTY is waiting for input, setting SENSE switch 3 terminates the input. This internal test executive routine also applies to test programs calling the test executive I/O routines.

If the system includes the power failure/restart (PF/R) option, the test executive PF/R routine permits automatic recovery of operating conditions after a prime power failure and recovery.

In the control panel mode of operation, the user has no direct interface with the test executive other than the start-up of the program.

2.2.4 Test Examples**Heading Message**

THIS IS THE 620 TEST EXECUTIVE
MEMORY SIZE IS 16K

Correct Control Statement A Input

A 000000 2.
A 000002 1,
A 000001 .
A 000001 ,

Cancelling Control Statement A Input

A 000001 \
A 000001 2\
A 000001 .

Invalid Control Statement A Input

A 000001 X INVALID
A 000001 2X INVALID
A 000001 .

Correct Control Statement B Input

B 000000 2.
B 000002 1,
B 000001 .
B 000001 ,

Cancelling Control Statement B Input

B 000001 \
B 000001 2\
B 000001 .

Invalid Control Statement B Input

B 000001 X INVALID
B 000001 2X INVALID
B 000001 .

Correct Control Statement C Input

C10.=000000 1.
C10.=000001 .
C10.=000001 2.
C10.=000002 .

C10.=000002 1,
(000011) =000000 2.
C10.=000001 ,
(000011) =000002 .
C10.=000001 ,
(000011) =000002 ,
(000012) =000000 3.
C10.=000001 ,
(000011) =000002 ,
(000012) =000003 .

C10.=000002 1,
(000011) =000000 2.
C10.=000001 ,
(000011) =000002 .
C10.=000001 ,
(000011) =000002 ,
(000012) =000000 3.
C10.=000001 ,
(000011) =000002 ,
(000012) =000003 .

Cancelling Control Statement C Input

C10.=000002 \
C10.=000002 3\
C10.=000002 \
C10.=000002 3\
C10.=000002 .

C10.=000001 ,
(000011) =000002 \
C10.=000001 ,
(000011) =000002 3\
C10.=000001 ,
(000011) =000002 ,
(000012) =000003 4\
C10.=000001 ,
(000011) =000002 \
C10.=000001 ,
(000011) =000002 3\
C10.=000001 ,
(000011) =000002 ,
(000012) =000003 4\
C12.=000003 .



S0,7,\
 S0,7,5\
 S0,7,5,\
 S0,7,5,7\
 S,\
 S,7\
 S,7,\
 S,7,5\
 S,7,5,\
 S,7,5,7\
 S,,\
 S,,5\
 S,,5,\
 S,,5,7\
 S,,,\
 S,,,7\

Correct Control Statement X Input

X 000000 2.
 X 000002 1,
 X 000001 .
 X 000001 ,

Cancelling Control Statement X Input

X 000001 \
 X 000001 2\

Invalid Control Statement X Input

X 000001 X INVALID
 X 000001 2X INVALID
 X 000001 .

Correct Control Statement D Input

D0.
 (000000) 000000 000001 000002 000003 000004 000005 000006 000007
 (000010) 000010 000011 000012 000013 000014 000015 000016 000017
 (000020)

D0,
 (000000) 000000 000001 000002 000003 000004 000005 000006 000007
 (000010) 000010 000011 000012 000013 000014 000015 000016 000017

D4.
 (000004) 000004 000005 000006 000007
 (000010) 000010 000011 000012 000013 000014 000015 000016 000017

D4,
 (000004) 000004 000005 000006 000007
 (000010) 000010 000011 000012 000013 000014 000015 000016 000017

Correct Control Statement I Input

I0,7,0.
 I1,6,1.
 I2,5,2.
 I3,4,3.
 D0.
 (000000) 000000 000001 000002 000003 000003 000002 000001 000000

Control Statement L Input With Forced Check-Sum Error

I0,7,0.
 L.CHECKSUM ERROR X = 000001
 D0.
 (000000) 000000 000001 000002 000003 000003 000006 000001 000000

Correct Control Statement P Input

I0,7,0.
 I1,6,1.
 I2,5,2.
 I3,4,3.
 P1,6,7. a a F a a A a a A a a B a a C a a C a a B a a A a a G a a a a a G a a G
 P1,6,777777. a a F a a A a a A a a B a a C a a C a a B a a A a a B a a A a a G



SECTION 3

INSTRUCTION TESTS

The **Instructions Test Program** of MAINTAIN II tests machine instructions, including optional instructions. It operates under the control of the test executive (section 2), which provides the user interface, utility aids, and standard subroutines.

The 620-series internal instructions are divided into functional groups to facilitate orderly testing. The test program is divided into three independent parts, two of which include, in addition to instruction subtests, an error printout routine, and a subtest-looping routine.

Part 1 of the instructions test program tests the following groups of instructions:

Basic control and switch (subtest 1)

Register change (subtest 2)

Overflow (subtest 3)

Shift/rotate (subtest 4)

Load/store (subtest 5)

Logical (subtest 6)

Jump/execute (subtest 7)

Arithmetic (subtest 8)

Indirect-addressing-limit test (subtest 13)

Part 2 tests the following groups of instructions:

Extended addressing (subtest 9)

Optional (subtest 10)

Input/output (subtest 11)

Part 3 is the instruction execution verification test (subtest 12). Part 3 is applicable only to the 620/f; it is not applicable to the V73.

The supervisor routine (IBGN) interfaces with the test executive to determine the mode of operation (Teletype or control panel). The test executive sets the mode flag (\$CON). If the Teletype mode is selected, the supervisor calls standard I/O routines for input/output via the Teletype printer and keyboard. The standard I/O routines are called indirectly through the test executive pointer table.

To test the 18-bit computer, the supervisor routine overlays data parameters and instructions since the program is assembled in 16-bit format.

From user inputs, the supervisor controls:

- a. Subtest sequencing
- b. Test cycles
- c. Output of the end-of-cycle message (e.g., END INST #2)

The error printout routine controls the output of error messages on the Teletype printer. This routine:

- a. Saves the contents of the A, B, and X registers at entry.
- b. Issues a carriage return and line feed.
- c. Outputs the address that called the routine (this is the error print address for troubleshooting reference).
- d. Outputs the saved contents of the A, B, and X registers.
- e. Restores the A, B, and X registers with original contents at entry and exits.

The instructions test program contains special manual entry points for looping and/or troubleshooting a subtest or sequence of subtests.

The basic control portion of this test (subtest 1, part 1) verifies that the computer performs basic operations required for execution of this and subsequent routines properly. The instructions tested are:

Mnemonic	Instruction
ERA	Exclusive-OR memory and A register
JAN	Jump if A register negative
JAZ	Jump if A register zero
JMP	Jump (unconditional)
JMP*	Jump indirect
JOF	Jump if overflow indicator set
LDA	Load A register
LDAI	Load A register immediate
LLRL	Long logical rotation left
NOP	No operation
ROF	Reset overflow indicator
SOF	Set overflow indicator
STA	Store A register

The switch instruction portion of this test (subtest 1, part 2) consists of two routines, each requiring user interven-



INSTRUCTION TESTS

The following two-word nonaddressing instructions are also tested:

Mnemonic	Instruction
LDAI	Load A register immediate
LDBI	Load B register immediate
LDXI	Load X register immediate
STAI	Store A register immediate
STBI	Store B register immediate
STXI	Store X register immediate

The logical instructions test (subtest 6) checks the following one-word addressing instructions using direct addressing:

Mnemonic	Instruction
ANA	AND memory and A register
ERA	Exclusive-OR memory and A register
ORA	Inclusive-OR memory and A register

The following two-word nonaddressing instructions are also tested:

Mnemonic	Instruction
ANAI	AND immediate
ERAI	Exclusive-OR immediate
ORAI	Inclusive-OR immediate

The jump/execute instructions test (subtest 7) comprises three routines. The first routine tests the following instructions using relative, direct, and indirect addressing. Both true and false conditions are checked.

Mnemonic	Instruction
JAN	Jump if A register negative
JANM	Jump and mark if A register negative
JAP	Jump if A register positive
JAPM	Jump and mark if A register positive
JAZ	Jump if A register zero
JAZM	Jump and mark if A register zero
JBZ	Jump if B register zero
JBZM	Jump and mark if B register zero
JMP	Jump (unconditional)
JMPM	Jump and mark (unconditional)
JO	Jump if overflow indicator set
JO	Jump and mark if overflow indicator set
JXZ	Jump if X register zero
JXZM	Jump and mark if X register zero
XAN	Execute if A register negative
XAZ	Execute if A register zero
XBZ	Execute if B register zero
XEC	Execute (unconditional)
XOF	Execute if overflow indicator set
XXZ	Execute if X register zero

The second routine of the jump/execute instructions test checks the following 620/f instructions:

Mnemonic	Instruction
JANZ	Jump if A register not zero
JANZM	Jump and mark if A register not zero
JBNZ	Jump if B register not zero
JBNZM	Jump and mark if B register not zero
JO	Jump if overflow indicator not set
JO	Jump and mark if overflow indicator not set
JXNZ	Jump if X register not zero
JXNZM	Jump and mark if X register not zero
XANZ	Execute if A register not zero
XBNZ	Execute if B register not zero
XO	Execute if overflow indicator not set
XXNZ	Execute if X register not zero

The third routine tests 620/f instructions IJMP (jump indexed) and JSR (jump and set return in X register). IJMP is tested in direct, indirect, relative, indexed relative to X, and indexed relative to B addressing modes. JSR is tested using both the B and X registers for return address storage.

The arithmetic instructions test (subtest 8) checks standard arithmetic instructions with both positive and negative operands and those causing overflow. The instructions tested are:

Mnemonic	Instruction
ADD	Add memory to A register
ADDI	Add immediate
SUB	Subtract memory from A register
SUBI	Subtract immediate
INR	Increment memory and replace
INRI	Increment memory and replace immediate

The extended-addressing test (part 2, subtest 9) comprises two routines. The first routine tests preindexing in which the selected register contents are added to the second word of the instruction after the effective address has been accessed. The second word of two-word extended addressing instructions contains an effective address. Addressing modes are: direct, indirect, relative, and indexed relative to the X or B register. The instructions tested are:

Mnemonic	Instruction
ADDE	Add extended
ANAE	AND extended
ERAE	Exclusive-OR extended
INRE	Increment memory and replace extended
LDAE	Load A register extended
LDBE	Load B register extended
LDXE	Load X register extended
ORAE	Inclusive-OR extended
STAE	Store A register extended
STBE	Store B register extended
STXE	Store X register extended
SUBE	Subtract extended



INSTRUCTION TESTS

If, before typing the period to complete computer-type input, the user wishes to change the specification to another computer type:

- a. Type a backarrow (←).
- b. Type the new computer-type code, followed by a period.

When a valid computer-type code and a period have been entered, the TTY printer outputs **cycles =**.

Type one of the following:

Input	Definition
(period)	Specifies continuous execution of the test and suppresses the END INST message after each test cycle
(comma)	Specifies continuous execution of the test and printing of the END INST message after each test cycle
Octal number followed by a period	Specifies automatic termination of the test after the designated number of cycles suppresses the END INST message after each test cycle
Octal number followed by a comma	Specifies automatic termination of the test after the designated number of cycles and printing of the END INST message after each test cycle

The test can be terminated at the completion of the current test cycle by setting SENSE switch 3, which returns control to the beginning of the test program.

Error conditions are described in control panel mode of operation.

If a TTY is not available or partially inoperative, load the program tape using the available input device:

- a. Load the test executive program using the high-speed paper tape reader or the card reader and associated loader program.
- b. Start the executive program with 006152 in the P register to establish control panel mode.
- c. Load the instructions test program (part 1, 2, or 3) using available input device.

To establish initial conditions in control panel mode:

- a. Set the P register to 000600.
- b. Press START or RUN.

The program halts with 000724 in the P register for selection of computer type and number of cycles:

- a. Set the A register to the computer type.
- b. Set the B register to the number of cycles; zero specifies continuous test execution until SENSE switch 3 is set.

In this mode of operation, set SENSE switch 1 for every subtest, excluding subtest 1.

The I/O instruction subtest (subtest 11) is not executed in the control panel mode.

- c. Press START or RUN.

The following SENSE switch options apply to all of the instructions test program except subtests 1 and 12.

Switch	Set	Reset
1	Halt on error	Print error data
2	Loop on subtest	Halt after subtest
3	terminate test	continue test

SENSE switch 2 can be used with special program entry points for troubleshooting.

To loop on a subtest for troubleshooting (parts 1 and 2):

- a. In the listing supplied with the program, locate the special troubleshooting routine labeled ITRS and load the address of ITRS in the P register.
- b. Load the appropriate computer number in the A register.
- c. Press START or RUN. The program halts with zero in the instruction register.
- d. Select the desired subtest for looping. Refer to the addresses in ITRS.
- e. Load the selected address in the P register, and set SENSE switch 2.
- f. Press START or RUN.

If the instructions test program is run on the 620/f computer, pressing the INT switch returns control to the test executive.

3.2 EXECUTING INSTRUCTION TESTS

Instruction tests can be operated from the Teletype or the control panel. Upon entry of valid CPU type and number of cycles, the basic control portion of the control and switch subtest is executed; the program then halts with 000600 in



INSTRUCTION TESTS

Part 3 of the instructions test program (applicable to the 620/f only) automatically executes the instruction execution verification test (subtest 12) the specified number of cycles or until SENSE switch 3 is set. The message:

END INST #3

is output at the end of each cycle if it is not suppressed.

When all subtest 12 cycles are complete:

- a. Control returns to the supervisor routine.
- b. The message:

CPU TYPE =

is output.

Error conditions are described in section 3.3.

After successful loading and initialization, part one of the instructions test program is automatically executed. SENSE switch 1 must be set during program execution in this mode (except for subtest 1).

At the completion of subtest 1, subtests 2 through 8 are executed by the program. Control is then returned to the part 1 supervisor.

To execute part 2 of the program:

- a. Load the part program tape.
- b. Load the applicable computer code in the A register.
- c. Load the number of test cycles in the B register; zero specifies continuous execution of the test.
- d. Press START or RUN.

I/O instruction subtest 11 is not executed in control panel mode.

After completion of part 2 testing, control is returned to its supervisor and the test can be rerun or control returned to the test executive.

The execution of part 3 is identical to that of part 2 described above.

To terminate the instructions test after a halt and return to the test executive when testing the 620/i, 620/L, or 622/i computer:

- a. Clear the instruction (U) register.
- b. Load 007000 in the P register.
- c. Press SYSTEM RESET.
- d. Press RUN two times.

When testing the 620/f and V73 computers, return control to the test executive by pressing the INT switch.

To return to the instructions test program from the test executive, type G600.

The value 600 represents the starting address of the instructions test program.

3.3 ERROR INDICATIONS

If an illegal entry is typed on the system's Teletype in response to:

CPU TYPE =
CYCLES =

the message:

INVALID

is output and the program waits for a correct entry. If the test is to be run on a 16-bit computer (620/i, 620/L, or 620/f) and a type 5 or 6 (622/i, 18-bit) is specified, or vice versa, the program again outputs the message:

CPU TYPE =

Correctly retype the entry.

During the basic control and switch portion of this subtest, programmed halts allow the setting of the SENSE switches. All other halts indicate the occurrence of errors. SENSE switch options are not applicable because the switches are being tested.

Refer to the program listing to correlate the instruction(s) under test with the contents of the P register. Error messages are not output.

During the switch portion of this subtest, the program halts upon detection of an error. The P register contains the error address, and the A, B, and X register, their values when the error is detected. Error messages are not output.

Press START or RUN to continue testing after an error halt.

Error reporting during subtests 2 through 8 is a function of SENSE switch 1.

If SENSE switch 1 is set, the program halts when an error is detected. The P register contains the error address. The significance of the A, B, and X register contents can be determined by referring to the program listing. Refer also to the listing to correlate the failing instruction(s) with the P register contents.

If SENSE switch 1 is reset and the error condition does not prohibit normal printout, an error message of the form:

(nnnnnn) aaaaaa bbbbbb xxxxxx

where

(nnnnnn) is the address of the instruction in error
aaaaaa is the A register contents
bbbbbb is the B register contents
xxxxxx is the X register contents

**EXAMPLE 2**

Execute part 1 on a type 2 computer with an 8K memory.
but specifying other computer types:

THIS IS THE 620 INSTRUCTION TEST, PART 1

```

CPU TYPE = 1.
CYCLES = 1,
END INST # 1
CPU TYPE = 3.
CYCLES = 1.
( 003572 )      000001      000000      000000
( 003675 )      000001      000000      000000
( 004004 )      177777      000000      000000
( 004061 )      177777      000000      000000
( 004105 )      177777      000000      000000 NO INDIRECT ADDRESS LIMITING
CPU = 4.
CYCLES = 1.
( 003572 )      000001      000000      000000
( 003675 )      000001      000000      000000
( 004004 )      177777      000000      000000
( 004061 )      177777      000000      000000
( 004105 )      177777      000000      000000 NO INDIRECT ADDRESS LIMITING
END INST #1
CPU TYPE =

```

Note the error printouts when computer types 3 and 4 are specified. The program tested the 620/f-only jump-if-not and execute-if-not instructions. The error printouts indicate invalid operations.

EXAMPLE 3

Execute part 2 on a type 2 computer:

THIS IS THE 620 INSTRUCTION TEST, PART 2

```

CPU TYPE = 2.
CYCLES = 1,
END INST #2
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 2.
CYCLES = 13.
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER

```

(I/O input test bypassed with SENSE switch 3)

```

CPU TYPE = 3-2 (Note backarrow to correct input)
CYCLES = 3,
END INST #2
END INST #2
END INST #2

```

THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU

```

NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 2.
CYCLES = 100.

```

```

THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFFFF      Input Error
( 003311 )      000301      000306      003350
( 003311 )      000323      000306      003351
CPU TYPE =

```

(Runs until terminated with SENSE switch 3)

THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE A LOWER CASE CHARACTER

(I/O test bypassed with SENSE switch 3)

CPU TYPE =



INSTRUCTION TESTS

```
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE =
```

EXAMPLE 8

Execute part 1 on a type 4 computer (8K memory), but specifying other computer types:

```
THIS IS THE 620 INSTRUCTION TEST, PART 1
```

```
CPU TYPE = 1.
CYCLES = 1,
END INST #1
CPU TYPE = 1.
CYCLES = 1.
CPU TYPE = 1.
CYCLES = 10,
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
CPU TYPE = 1.
CYCLES = 10.
CPU TYPE = 2.
CYCLES = 3,
END INST #1
END INST #1
END INST #1
CPU TYPE = 2.
CYCLES = 100.
CPU TYPE =
```

EXAMPLE 9

Execute part 2 on a type 4 computer (8K memory), but specifying other computer types:

```
THIS IS THE 620 INSTRUCTION TEST, PART 2
```

```
CPU TYPE = 1.
CYCLES = 1,
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER-CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 2.
CYCLES = 1,
( 002337 )    000005    000003    001623
( 002337 )    000005    000001    001631
( 002337 )    000001    177777    001700
( 002337 )    000001    177777    001704
( 002337 )    000001    000001    001747
( 002337 )    000001    000001    001753
END INST #2
```

```
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 3.
CYCLES = 1,
END INST #2
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 4.
CYCLES = 1,
END INST #2
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE =
```

Note the error printouts when the type 2 computer is specified. The program tested the 620-only divide instructions on a 620/f.

EXAMPLE 10

Execute the instructions test program on a 622 computer (18 bit) with optional instructions (type 6) and 16K of memory:

```
THIS IS THE 620 INSTRUCTION TEST, PART 1
```

```
CPU TYPE = 5.
CYCLES = 2,
END INST #1
END INST #1
CPU TYPE = 6.
CYCLES = 7,
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
END INST #1
CPU TYPE =
```

```
THIS IS THE 620 INSTRUCTION TEST, PART 2
```

```
CPU TYPE = 5.
CYCLES = 3.
THIS IS THE I/O INSTRUCTION TEST
PLEASE TYPE IN A LOWER CASE CHARACTER
THANK YOU
NOW TYPE ASDFASDFASDFAS
      ASDFASDFASDFAS
CPU TYPE = 6.
CYCLES = 3,
END INST #2
END INST #2
END INST #2
```

continued



SECTION 4

MEMORY-TEST PROGRAM

The **Memory-Test Program of MAINTAIN II** tests the operation of memory in both 16- and 18-bit 620-series computers. It does not test the read-only memory (ROM). The program ascertains the operational status of the computer memory and assists in locating and correcting faults. Parity errors are also reported if the memory parity option is included in the system. All available memory sizes can be tested (4K through 32K).

The memory-test program is designed to test the minimum configuration of a 620-series computer with 4K of memory (maximum, 32K), a 33/35 ASR TTY (Varian-modified), and, if applicable, the memory parity option.

The format of the memory-test program is normally a punched paper tape for loading from the Teletype or high-speed paper-tape reader. Other media are available (e.g., card object deck).

The memory test program comprises two parts. Both parts of the program consist of five basic subtests:

Unique address (test 1) -- This routine tests the memory address register and associated circuits. It loads each memory address with the address itself and compares the expected and actual values.

All-zero (test 2) -- This routine loads zeros in all addresses and tests each address for an actual content of zero.

All-ones (test 3) -- This routine loads ones in all addresses and tests each address for an actual content of one.

Checkerboard (test 4) -- This routine loads memory with alternate word patterns (125252 and 052525 for 16-bit memories and 525252 and 252525 for 18-bit memories). The pattern is reversed on alternate cycles of the test routine.

Worst-case pattern (test 5-10) -- This routine loads and reads a worst case pattern and its complement in memory. The pattern creating maximum sense winding noise during reading operations is stored in memory. Memory is addressed sequentially from the lowest numbered address in the test block.

The worst case pattern masks are:

Test	620/f	620/L	620-622/i
5	004001	000140	000202
6		000144	000203
7			004001
10			004010

Part 1 of the memory test program tests those areas of the first 4K memory module that are not tested by part 2 (i.e., addresses 000000, 000001, 000040 through 000043, 000400 through 000621, and 003550 through 007755). It contains a modified test executive; the standard test executive program (section 2) must be reloaded before further tests can be executed.

The modified part 1 test executive contains the following utility routines: (1) print/change pseudoregisters A, B,

and X; (2) dump core memory on the TTY printer; (3) trap; and (4) transfer to specified locations.

Part 2 of the memory test program verifies the operation of all of memory or of specific 4K modules. If module 0 is specified, only addresses 000002 through 000037, 000044 through 000077, 000120 through 000377, and 000622 through 003547 are tested.

Memory is enabled at the beginning of both parts of the memory test program. If the memory-parity option is included in the system, a parity error interrupts the program. The parity error types are instruction, address, operand, and trap.

Because the memory test does not otherwise test interrupts, a trap parity error indicates a parity hardware malfunction. Parity errors produce error messages indicating the type of error and the associated memory address (section 4.3).

The memory test program does not test the memory parity option; it merely reports the occurrence of a memory parity interrupt.

4.1 INITIAL CONDITION SELECTION

To load the memory test:

- Load the test executive (section 2).
- Position the memory test program tape (part 1 or part 2) in the paper-tape reader with leader at the reading station. After executing part 1 of the program, always reload the test executive for further testing (the bootstrap routine remains intact).
- Type L, followed by a period, on the Teletype keyboard, or load 000001 in the A register and 007600 in the P register, press RESET, and, in run mode, press START or RUN.

When loaded, the program halts with 000777 in the instruction register. The A register then contains a code indicating the type of computer:

Code	Computer
000000	620-622 i
000001	620/L
000002	620/f

If this value is incorrect for the computer to be tested, load the correct code in the A register. For part 1 only, load the TTY device address in the B register. Press START or RUN to continue.

At loading time, the A register is preset to 000002, and the B register, to 000001 (standard TTY device address). The CPU type designator selects the worst-case data patterns for the respective CPU.



MEMORY-TEST PROGRAM

When test execution is complete, the program outputs a message indicating the number of errors detected and the number of cycles the test was run. Control is then returned to the beginning of the program, which again outputs the message memory test.

Error conditions are described in section 4.3.

Console Mode

Operate the test executive in accordance with the procedures when executing a test program in control panel mode.

Start the test executive with 006152 in the P register to establish control panel mode. After successful loading of the memory test program and verification of the computer type (section 2.1.1), the computer halts with 000037 in the instruction register, the highest memory address in the X register (part 2 only), and 0100000 in the A register (0400000 if testing the 18-bit 622/i computer).

To test the applicable portions of memory (part 1 or part 2):

- a. Load the desired number of test cycles in the A register (zero specifies continuous execution), leaving the sign bit (bit 15) set.
- b. Press START or RUN.

To test specific memory modules (part 2 only):

- a. Reset the A register sign bit.
- b. Load a right-justified octal digit corresponding to the memory module to be tested in the A register (e.g., to test addresses 030000 through 037777, load 000003).
- c. Press START or RUN.
- d. Repeat steps b and c for each block of memory to be tested.
- e. After entering the last digit, set the sign bit.
- f. Load the desired number of test cycles in the A register (zero specifies continuous execution).
- g. Press START or RUN.

In both part 1 and part 2 of the program, the five subtests are executed the specified number of cycles or until SENSE switch 3 is set. If an error is detected and SENSE switch 2 is not set, the overflow indicator lights momentarily during test execution.

After testing is complete, the A register contains the total number of detected errors; the B register, the number of cycles the test was executed; and the instruction register, 000777. Pressing START or RUN returns control to the beginning of the memory test program.

Error conditions are described in section 4.3.

To terminate the memory test and return to the test executive when testing the 620/i, 620/L, or 622/i computer:

- a. Clear the instruction register.
- b. Load 007000 in the P register.
- c. Press SYSTEM RESET.
- d. Press RUN two times.

When testing the 620/f computer, return control to the test executive by pressing the INT switch.

To return to part 1 of the memory test program from the test executive, type:

G17.

This is the common entry point for start-over of the test. Type:

G7.

for initial start-up (specify the CPU type and TTY device address). Type:

G27.

for entry to the part 1 modified test executive.

To return to part 2 of the memory test program from the test executive, type:

G500.

The value 500 represents the starting address.

4.3 ERROR INDICATIONS

When operating with the Teletype

TOO MANY PARAMETERS

indicates that more than fifteen parameters were supplied in response to nk module(s) to be tested. Specify the correct number of parameters (15 or less). Also, is a specified module of memory is outside memory range, the message:

MODULE NOT WITHIN MEMORY RANGE

is output. Enter the corrected parameters. If an illegal entry is typed in response to:

CYCLES =

the message:

INVALID

Is output, and the inquiry is repeated. Correctly type the entry.



4.4 TEST VALIDATION EXAMPLES

The results presented in this section were extracted from TTY hardcopy collected during validation of the program.

EXAMPLE 1 -- 620/f Computer

Part 1:

```
MEMORY TEST
CYCLES = 3.
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000003
```

```
MEMORY TEST
CYCLES = 2,
END MEMO
END MEMO
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000002
```

(SENSE switch 3 set)

```
MEMORY TEST
CYCLES =
MEMORY TEST
CYCLES = W INVALID
CYCLES =
```

Part 2:

```
MEMORY TEST
MEMORY SIZE IS 32K
```

```
4K MODULE(S) TO BE TESTED = 0, 1, 2.
CYCLES = 3.
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000003
MEMORY SIZE IS 32K
```

```
4K MODULE(S) TO BE TESTED = 1.
CYCLES = .
ERROR TOTAL = 000000
```

(SENSE switch 3 set)

```
NUMBER OF CYCLES RUN = 000004
MEMORY SIZE IS 32K
```

```
4K MODULE(S) TO BE TESTED = 0, 1.
CYCLES = 4,
END MEMO
END MEMO
END MEMO
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000004
MEMORY SIZE IS 32K
```

EXAMPLE 2 -- 622/i Computer

Part 1:

```
MEMORY TEST
CYCLES = .
ERROR TOTAL = 000000
```

(SENSE switch 3 set)

```
NUMBER OF CYCLES RUN = 000134
```

```
MEMORY TEST
CYCLES = 2,
END MEMO
END MEMO
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000002
```

```
MEMORY TEST
CYCLES = W INVALID
CYCLES = 2 - 3.
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000003
```

```
MEMORY TEST
CYCLES = \
CYCLES =
```

Part 2:

```
MEMORY TEST
MEMORY SIZE IS 16K
```

```
4K MODULE(S) TO BE TESTED = 0, 1.
CYCLES = 2,
END MEMO
END MEMO
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000002
MEMORY SIZE IS 16K
```

```
4K MODULE(S) TO BE TESTED = 0, 0, 0, 0, 0, 0,
TOO MANY PARAMETERS
MEMORY SIZE IS 16K
```

```
4K MODULE(S) TO BE TESTED = 7,
MODULE NOT WITHIN MEMORY RANGE
MEMORY SIZE IS 16K
```

```
4K MODULE(S) TO BE TESTED = 1.
CYCLES = 3.
ERROR TOTAL = 000000
NUMBER OF CYCLES RUN = 000003
MEMORY SIZE IS 16K
```

EXAMPLE 3 -- 620/i Computer

Part 1:

```
MEMORY TEST
CYCLES = 3.
```

continued



SECTION 5

TELETYPE TEST PROGRAM

The Teletype (TTY) test program of MAINTAIN II tests the operation of the TTY and isolates malfunctions. The Teletype units that can be tested are models 33 ASR, 35 ASR, and 35 KSR (Varian-modified) and compatible CRT units.

Acceptable ASCII characters and their representations are listed in table 5-1.

The Teletype test program operates under the control of the test executive (section 2), which provides the user interface, utility aids, and standard subroutines. The following are the elements of the Teletype test program.

The printer test (PT) tests the printed output of the TTY. All 64 TTY characters are output in a specified pattern (section 2.2). Each line output starts with the second character of the previous line, thereby testing all characters in each of the 72 possible print positions.

The keyboard echo (KE) test accepts the input of characters from the TTY keyboard and outputs them to the

printer so that input can be compared with output (section 2.3).

The keyboard character (KC) test verifies correct operation of the TTY keyboard. The user enters the characters, both upper and lower case, by pressing the applicable keys. The specified characters are immediately output on the TTY printer for visual comparison (section 2.4).

For ASR models only, the reader test (RT) verifies that the TTY paper tape reader reads known data patterns correctly and that it starts and stops in response to on and off commands (section 2.5). Varian supplies the patterned paper tape (part number 92V0107-005).

For ASR models only, the punch/reader (PR) test verifies punch and reader accuracy and correct response to on and off commands (section 2.6).

The print suppression (PS) test verifies proper print suppression for the model 35 ASR only (section 2.7).

Table 5-1. (ASCII) Standard Characters

BITS					COLUMNS										
b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	0	1	1	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	0	1	1	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	1	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	0	1	1	4	EOT	DC4	\$	4	D	T	d	t
0	1	0	1	1	1	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	0	1	1	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	0	1	1	8	BS	CAN	(8	H	X	h	x
1	0	0	1	1	1	1	9	HT	EM)	9	I	Y	i	y
1	0	1	0	1	1	1	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	1	1	1	11	VT	ESC	+	;	K	[k	{
1	1	0	0	1	1	1	12	FF	FS	,	<	L	\	l	!
1	1	0	1	1	1	1	13	CR	GS	-	=	M]	m	}
1	1	1	0	1	1	1	14	SO	RS	.	>	N	^	n	~
1	1	1	1	1	1	1	15	SI	US	/	?	O	_	o	DEL



TELETYPE TEST PROGRAM

- c. With the SHIFT key depressed, type an identical line. If input is correct, the program responds by outputting the reference line of lower case characters.
- d. Set, then reset, SENSE switch 3 to terminate the test and return control to the test selection routine.

To operate the reader test:

- a. Position the test tape in the reader on any frame past the first RUBOUT (all-holes) character.
- b. Select SENSE switch options, if desired (section 2.1.2).
- c. Select RT.

The program:

- a. Reads the test tape, and, if errors are detected, stores the expected results and actual values in an error table.
- b. Executes the reader-off test.
- c. Outputs the error table in accordance with SENSE switch settings.
- d. Executes the reader-on test.
- e. Repeats the cycle.

All 256 data bit combinations are tested, except:

Code	Subcode	Function
0214	014	Form
0221	021	Reader on
0223	023	Reader off
0222	022	Punch on
0224	024	Punch off

Set, then reset, SENSE switch 3 to terminate the test and return control to the test selection routine. When the test is terminated, the program outputs:

- a. The number of times the tape was repeated (looped)
- b. The number of errors (data and reader on/off)
- c. The number of reader-on errors
- d. The number of reader-off errors

PUNCH/READER TEST

To operate the punch/reader test:

- a. Select PR. The program responds by outputting the message:

TYPE OF TTY (33 OR 35) =

- b. Type the digits corresponding to the TTY type. The program responds by punching approximately 10 inches of leader, then pauses.

- c. Position the punched leader in the reader with approximately two inches of slack.

- d. Select SENSE switches, if desired.

- e. Turn on the reader.

The program:

- a. Punches an ascending binary pattern (excluding certain control codes).
- b. Executes the punch on/off test.
- c. Outputs 10 inches of blank tape.
- d. Reads the tape in the reader and enters errors in the error table.
- e. Prints the error table in accordance with SENSE switch settings.
- f. Repeats the test.

Set, then reset, SENSE switch 3 to terminate the test and return control to the test selection routine. When the test is terminated, the program outputs:

- a. The number of test cycles
- b. The number of errors (data and punch on/off)
- c. The number of punch on/off errors

Error conditions are described in section 3.5.

PRINT SUPPRESSION TEST

To operate the print suppression test:

- a. Select PS. The program responds by continuously outputting:

ASR TTY PRINT SUPPRESSION TEST

- b. Set, then reset, SENSE switch 3 to terminate the test and return control to the test selection routine

Error conditions are described in section 3.6.

Note: The Print Suppression Test is only applicable to Teletype model 35. The Teletype model 33 does not have print suppression capability.

RETURNING TO THE TEST EXECUTIVE

To terminate the TTY test and return to the test executive when testing the 620/i, 620/L, or 622/i computer:

- a. Clear the instruction register.
- b. Load 007000 in the P register.

continued



After test termination, the program outputs error verification information of the form:

```
000477
000000
000000
000000
```

The first line represents the number of times the test was repeated. There were no errors.

PUNCH/READER TEST

The punch/reader test error output consists of a printout of expected and actual values.

Data error indications are of the form:

```
000xxx    000aaa
```

where xxx represents the expected result and aaa is the actual value.

EXAMPLE:

EXPECTED	ACTUAL
000104	000100

The expected bit configuration was:

```
000 000 000 001 000 100
```

The punch, however, produced:

```
000 000 000 001 000 000
```

Punch on/off errors are indicated by the following output:

EXPECTED	ACTUAL
000000	000000

After test termination, the program outputs error verification information of the form:

```
000477
000000
000000
```

The first line represents the number of times the test was executed. Lines 2 and 3 indicate there were no data or punch on/off errors (section 2.6).

PRINT SUPPRESSION TEST

If errors occur during the print suppression test, asterisks appear in the continuous output.

5.4 TEST VALIDATION EXAMPLES

The results presented in this section were extracted from TTY hardcopy collected during validation of the program.

Begin testing:

THE TELETYPE TEST IS LOADED

TELETYPE DA =

Input valid device address:

TELETYPE DA = 01.

Test selection request:

TTY TEST IDENTIFIER =

Input valid test identifier:

TTY TEST IDENTIFIER = PT.

Examples of invalid test identifier inputs:

TTY TEST IDENTIFIER = 7 INVALID FG.

INVALID TEST IDENTIFIER

TTY TEST IDENTIFIER = HIJ INVALID K INVALID

INVALID TEST IDENTIFIER

Keyboard echo test heading:

KEYBOARD ECHO TEST

Keyboard character test reference lines:

```
123456789: QWERTYUIOPASDFGHJKL;ZXCVBNM,./
!"#$%&'()*=-@[\+!]<>?
```

Example of reader test error printout:

TTY TEST IDENTIFIER = RT.

EXPECTED	ACTUAL
000363	000364
000364	000365
000001	
000002	
000000	
000000	

Example of punch/reader test error printout:

TTY TEST IDENTIFIER = PR.

TYPE OF TTY (33 or 35) = 33.

EXPECTED	ACTUAL
000373	000374
000374	000375
000375	000376
000376	000377
000000	000000

```
000001
000006
000001
```




SECTION 6

POWER-FAILURE/RESTART TEST

The Power-Failure/Restart Test Program of Maintain II tests the operation of the 620-series and 73 systems power failure/restart (PF/R) option.

The PF/R provides an orderly shutdown in case of power failure or turn-off and, when power is restored, restarts the program in progress when power was lost.

Power input to the computer is indirectly monitored by the PF/R. A power-failure-monitor voltage in the computer power supply is constantly being sensed to determine power status. If the monitor voltage drops (due to power failure or power switch turn-off), the PF/R causes an interrupt. This interrupt has the highest priority in the system (unless the memory protect option is used, then this interrupt will follow it in the priority order). The CPU then executes a user-programmed service routine (table 6-1) that places the contents of volatile registers (A, B, X, P, and overflow) into memory. The program halts, the memory is disabled, and the system is reset. The power-down service routine (SAVE) cannot be interrupted by lower-priority options or controllers.

When power is restored, the PF/R enables the memory. The CPU executes a user-programmed power-up service routine (RESTORE) that restores the contents of the volatile registers, and the system resumes service of the program in progress at the time of the interrupt.

For a detailed description of the PF/R, refer to the applicable 620-series option manual.

The PF/R test program is designed to test the minimum configuration of a 620-series computer with 4K of memory, PF/R, and 33/35 ASR Teletype (TTY). The test can be performed in both TTY and control panel modes of operation.

The PF/R test program object format is normally a punched paper tape for loading from the TTY reader or a high-speed paper tape reader. Other media are available (e.g., card object deck).

Background programs and other test programs cannot be executed simultaneously with the PF/R test program, and the operations of other internal computer options (i.e., priority interrupt module, buffer interface controller, real-time clock, etc.) are not monitored.

Table 6-1. Typical PF/R Service Routine

```

ORG 040
JMPM PWRD
JMP PWRU

      POWER-DOWN PROCESSOR (SAVE)

ORG 1000
PWRD ENTR
  
```

Table 6-1. Typical PF/R Service Routine (continued)

```

STA SAVA      SAVE A, B, X REG
STB SAVB
STX SAVX
TZA           CHECK/SAVE OVFL
DATA 005511   INCR A IF OVFL SET
STA SAVO
INR HLTF      SET PF/R FLAG
PHLT HLT
  
```

POWER-UP PROCESSOR (RESTORE)

```

PWRU LDA HLTF  CHK PWRUP FROM RUN
      JAZ PHLT
      TZA      CLEAR PF/R FLAG
      STA HLTF
  
```

(Coding to reinstate optional hardware after a power failure, if desired, must be defined here; refer to the PF/R manual for timing restrictions. The PF/R test program makes no provision for monitoring or restoring option conditions.)

```

LDA SAVO      SETUP OVFL FLAG
ROF
JAZ *+3
  
```

```

SOF
LDA SAVA      RETU A, B, X REG
LDB SAVB
LDX SAVX
JMP* PWRD     RETU TO INT ADDR

SAVA DATA 0
SAVB DATA 0
SAVX DATA 0
SAVO DATA 0
HLTF DATA 0
END
  
```

The PF/R test program consists of the following subtests:

- Halt test
- Volatile registers test
- Memory test

The HALT test checks PF/R operation in computer halt mode. If power loss occurs in this mode:

- The PF/R interrupt is not acknowledged.
- The CPU and memory are immediately disabled.
- The contents of the volatile registers are lost.
- The program halts when power is restored to indicate that the PF/R power-down SAVE routine was not initiated.



To continue volatile-register test execution:

- a. Turn off, then turn on, CPU power.
- b. The program executes the first pass of this two-pass test; outputs an error message, if errors were detected (section 3); and rings the TTY bell.
- c. Turn off, then turn on, CPU power to execute pass 2.

At the completion of pass 2, the program outputs an error message, if errors were detected; terminates the volatile registers test; and outputs the message:

CORE VALIDITY CHECK

on the TTY printer. The program waits in a loop, and the TTY bell rings.

To continue memory test execution:

- a. Turn off, then turn on, CPU power.
- b. The program executes the first pass of the memory test; outputs an error message (section 3) if errors were detected, and rings the TTY bell.
- c. Repeat steps a and b for the remaining passes of this four-pass test.

At the completion of pass 4, the program terminates the memory test and outputs the message:

HALT TEST

To terminate the PF/R test program and return to the test executive when testing the 620/i, 620/L, or 622/i computer:

- a. Clear the instruction register.
- b. Clear the P register.
- c. Press SYSTEM RESET.
- d. Press RUN.

When testing the 620/f computer, return control to the test executive by pressing the INT switch.

To return to the PF/R test program from the test executive, type G500. The value 500 represents the starting address of the PF/R test program.

If the TTY is not included in the system or is partially inoperative, the PF/R test program can be executed in control panel mode. In this case, start the test executive program with 006152 in the P register (section 2).

After successful loading:

- a. Load 000500 in the P register.
- b. Press START or RUN.

- c. The program halts with 000772 in the P register and 000777 in the instruction register and waits for time delay input.
- d. Calculate the time-delay factor for a system as calculated for initial operation and load the A register with the octal value thus derived.
- e. Press START or RUN.
- f. The program halts with 000001 in the instruction register defining the halt test ready for execution.
- g. Initiate a power-down/power-up sequence by turning off, then restoring, CPU power each time the computer halts after completing a pass of the four-pass halt test.

To continue execution of the volatile registers and memory tests, initiate a power-down/power-up sequence six times at 2 second intervals. If the program halts between power-down/power-up sequences during these tests, an error was detected.

6.3 ERROR INDICATIONS

HALT TEST

If, during the halt test, the program detects a discrepancy between the specified background bit configurations and the actual value, an error message of the form:

ERROR-CORE	MODIFIED	xx	TIMES
LOC	INITIAL	FINAL	
(xxxxxx)	xxxxxx	xxxxxx	

is output at the completion of each pass. Up to 20 such errors can be listed.

Sense switch options are described in section 6.1.

Refer to the applicable system and PF/R maintenance manuals for correction procedures.

Volatile-Registers Test

During this two-pass volatile-registers test, if the program detects a discrepancy between the specified bit configurations and the actual value, an error message of the form:

	REGISTER	ERROR
	INITIAL	FINAL
A	xxxxxx	xxxxxx
B	xxxxxx	xxxxxx
X	xxxxxx	xxxxxx
P	xxxxxx	xxxxxx
OF	ON or	ON or
	OFF	OFF

is output at the completion of both passes.



SECTION 7

PRIORITY-INTERRUPT-MODULE TEST

The **Priority Interrupt Module Test** of MAINTAIN II tests the operation of the model 620-16 priority interrupt module (PIM).

The PIM establishes eight levels of interrupt priority for selected peripheral device controllers and stores and processes, in the order of their priority, interrupt requests from these controllers.

The PIM automatically scans the interrupt lines every 900 nanoseconds or 468 nanoseconds for the 620/L-100. If signals occur on more than one interrupt line, the highest-priority signal is acknowledged. The remaining interrupt requests are stored until each has been acknowledged. The

PIM permits any or all of the eight interrupt lines to be enabled or disabled.

Acknowledgement of an interrupt by the CPU executes the instruction at the memory address specified by the PIM. This instruction can be any of the instruction set, excluding I-O instructions. Thus, an interrupt can be serviced in one instruction execution period.

The PIM responds to five external control and three data transfer instructions (table 7-1). A typical PIM service routine is given in table 7-2.

For a detailed description of the PIM, refer to the applicable option manual.

Table 7-1. PIM Input/Output Instructions

Mnemonic	Code	Description
External Control		
EXC 014x*	010014x*	Clear interrupt registers
FXC 024x	010024x	Enable the PIM
EXC 0244	0100244	Enable all PIM's
FXC 034x	010034x	Clear interrupt registers and enable the PIM
EXC 044x	010044x	Disable the PIM
EXC 0444	0100444	Disable all PIM's
EXC 054x	010054x	Clear interrupt registers and disable the PIM
Data Transfer		
OME 004x	010304x	Transfer memory to the mask register
OAR 014x	010314x	Transfer A register contents to the mask register
OBR 024x	010324x	Transfer B register contents to the mask register

* x = PIM device address.

**SUBTEST 1**

After the interrupt addresses are selected the user can select the subtest to run:

- a. The program outputs the message:

ENTER SUBTEST NUMBER

- b. For subtest 1 type a one, followed by a period. The program then outputs the message:

SET INTERRUPTS

- c. Momentarily ground selected PIM interrupt lines (IL00-IL07) (refer to the PIM manual) or use an interrupt simulator to set selected interrupts; press the TTY space bar.
- d. Step c can be repeated any time during the delay period after the **SET INTERRUPTS** message. This delay is 5 seconds for the 620/i, 620/L, and 622/i computers and 2 seconds for the 620/f or 73.

The program executes subtest 1, in which all interrupts are inhibited, and outputs the message:

NO INTERRUPTS

SUBTEST 2

For subtest 2 type a two, followed by a period. The program then outputs the message:

ENTER NUMBER OF 5-SECOND INTERVALS

This message requires operator input of the delay time he requires to set interrupt requests. He can opt to test all lines or selected groups of lines in one or more passes, or repeatedly test a single line, selected groups of lines, or all lines.

The 5-second interval is applicable to the 620/i, 620/L, and 622/i computers. On the 620/f or 73, this interval is approximately 2 seconds.

Set selected interrupts.

Type the desired number of delay intervals, followed by a period.

If a zero is typed, the program will wait for further interrupt simulation until terminated by setting, then resetting, SENSE switch 3.

The program executes subtest 2, and outputs the number of the interrupt line on which an interrupt occurred. If multiple interrupts were set, the line numbers are in order of priority (1 through 8).

SUBTEST 3

At the successful completion of a subtest:

- a. The program outputs the message:

ENTER SUBTEST NUMBER

- b. For subtest 3 type a three, followed by a period. The program then outputs the message:

SET INTERRUPTS

- c. Set selected interrupts, press the Teletype space bar.
- d. Repeat step c as desired during the delay period.

The program executes subtest 3, in which the PIM is disabled and should recognize no interrupts, and outputs the message:

NO INTERRUPTS

Error conditions are described in section 3.

To execute subtest 4 type a four, followed by a period. The program then outputs the message:

SET INTERRUPTS

Set selected interrupts press the Teletype space bar.

The program executes subtest 4, in which the PIM is disabled and the interrupt line register is cleared, and outputs the message:

NO INTERRUPTS

When the four subtests have been executed, set SENSE switch 3 to return to the beginning of the PIM test program to restore the contents of memory in the selected interrupt addresses to pretesting status.

The program can be reexecuted to test another PIM or control returned to the test executive.

To terminate the PIM test program and return to the test executive when testing the 620/i, 620/L, or 622/i computer:

- a. Clear the instruction register.
- b. Load 007000 in the P register.
- c. Press SYSTEM RESET.
- d. Press RUN two times.

When testing the 620/f computer, return control to the test executive by pressing the INT switch.



PRIORITY-INTERRUPT-MODULE TEST

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
12345678

Interrupts were raised on all eight lines and line numbers correctly reported (in order of priority).

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
1234567866666666

Subtest 2 was again run; additional interrupts were raised on line 6 during the delay interval.

ENTER SUBTEST NUMBER 3.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER 4.
SET INTERRUPTS
NO INTERRUPTS

ENTER SUBTEST NUMBER
PIM TEST

SENSE switch 3 was set, then reset, to return to the beginning of the program and restore the contents of memory.

ENTER PIM DEVICE ADDRESS 40.
ENTER ORIGIN OF TRAP ADDRESSES 100.

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 1.
INVALID INTERRUPT

An incorrect interrupt address origin was specified and an interrupt raised on line 1, producing the **INVALID INTERRUPT** message.

ENTER SUBTEST NUMBER
PIM TEST
RESET SENSE SWITCH 3
RESET SENSE SWITCH 3

Sense switch 3 was set to return to the beginning of the test, but was not then immediately reset so that testing could continue.

ENTER PIM DEVICE ADDRESS 40.
ENTER ORIGIN OF TRAP ADDRESSES 120.

ENTER SUBTEST NUMBER 2.
ENTER NUMBER OF 5 SECOND INTERVALS 2.
12342345678

ENTER SUBTEST NUMBER 4.
SET INTERRUPTS
12345678

Interrupts were raised during the delay interval in subtest 4 resulting in the printout of interrupt line numbers instead of the correct message: **NO INTERRUPTS**.



SECTION 8

REAL-TIME CLOCK TEST PROGRAM

The Real-Time Clock (RTC) on the 73/620 series computers generates interrupts at a specified rate. On the 73 and 620/f, this rate is variable under program control. In addition, the 73 and 620/f model RTC drives a readable 16-bit free-running Counter. The purpose of the RTC test program will be to provide the user with an interface to evaluate the performance of these features of the Real-Time Clock.

The RTC test program has two main goals. The first is to provide output with which the user can validate the correct operation of the features of the RTC. The second is to operate in as many environments as the RTC is found while interfacing with the user as simply as possible.

A software timer which could validate correct RTC operation would have been the ideal solution to the first goal. Due to variations in cycle time, however, such a software

timer would be very CPU model sensitive. Thus, in interest of the second goal, an alternative method was adopted. The RTC output will be translated as directly as possible into output which the user can evaluate by checking against an external time source, such as a stop watch.

8.1 FUNCTIONAL CAPABILITIES

The RTC test program will provide two main services. First, an I/O instruction and interrupt test will be run. This will check the correct functioning of the RTC-oriented I/O instructions. The test will also verify that RTC interrupts are occurring, though it makes no attempt to time them or interpret them. The second test will allow timing of the interrupts. This is done by using the interrupts to drive an elapsed-time counter and an interval timer. By comparing their outputs with an external time source, RTC performance can be evaluated.

I/O INSTRUCTIONS

73 and 620/f Instructions

Mnemonic	Octal	Function	Description
EXC 0147	100147	Enable RTC	Enables both variable interval interrupts and overflow interrupts.
EXC 047	100047	Clear Free Running Counter (FRC)	The only way to clear the FRC.
EXC 0447	100447	Inhibit RTC (Initialize)	Inhibits all interrupts; resets interrupts register and divide-by-eight counter.
EXC 0247	100247	Inhibit Overflow	Inhibits only overflow interrupts
EXC 0347	100347	Enable Increment/Inhibit Overflow	Enables variable interval interrupts; inhibits overflow interrupts
EXC 0647	100647	Initialize Variable Interval Interrupt (VII) counter	Loads (VII) counter from Interval Select Register
EXC 0747	100747	Inhibit Variable Interval Interrupt (VII)	Disallows VII's
OAR 047	103147	Output to Interval Select Register	
OBR 047	103247		
*OME 047	103047		
INA 047	102147	Input FRC	
INB 047	102247		
*IME 047	102047		
CIA 047	102547	Clear and input	
CIB 047	102647	FRC	

* These commands should not be used if the RTC is used in a system containing the PMA option.



- c. 620/L-10X CPU or 620/L-00X CPU
- d. 620/i CPU with RTC option (620-13)
- e. 622/i CPU with RTC option (622-13)

A Teletype (620-06, -08) will be supported if available.

8.3 SOFTWARE DESIGN SUMMARY

The Real-Time Clock Test consists of two parts, one testing the basic I/O instructions and interrupts and another for interrupt timing.

8.3.1 I/O Instruction and Interrupt Test

This test is executed once upon entrance to the RTC test. All RTC I/O instructions and the computers ability to detect (variable) interval interrupts and memory overflow interrupts are verified. Upon detection of an error, the computer will either halt with an error code in the instruction register or print an error message. This test must be passed before executing the interrupt timing test.

8.3.2 Interrupt Timing Test

The test program will request that the operator specify the selectable hardware connections (for the free-running counter on the 73 and 620/f) and for the (Variable) Interval Interrupt.

The performance of the RTC may be checked in two ways. First, either the FRC or the (V)II may be used to drive an interval timer. Second, both may be used to run an elapsed time counter. These produce outputs which may be compared to an external time source for checking RTC performance. No software timing checks are included in this test program.

8.4 USER FACILITIES

8.4.1 Interval Timer

The interval timer will ring the Teletype bell (if a Teletype is available) every 'n' seconds, where 'n' is the current display interval. The time for groups of rings can then be measured with a stop watch and an estimate made on RTC performance.

In addition to ringing the bell, the overflow light is complemented. Thus, a signal is visible when operating without a Teletype. Finally, since the 73 has no overflow light, its console lights will be complemented.

The display interval may be varied, but may be no greater than the number of seconds equivalent to the capacity of

the interval timer. The capacity is 040,000 interrupts (= 16,384 interrupts). Thus,

Interrupts Per Second	Maximum Display Interval
10,000	1 second
1,000	16 seconds
60	273 seconds

The test program checks the range of the display period when input and will signal if it is too large.

8.4.1.1 Interval Timer Accuracy

The interval timer has an accuracy of ± 1 interrupt per interval at best. Thus, for a VII at 10,000 interrupts per second and a select count of 1, this inaccuracy is only one ten thousandths of a second. However, with a select count of 4095, this changes to an accuracy of about \pm one-half second. Thus, using the interval timer to time 1 second intervals would produce gross error in the latter case. In general, when the number of interrupts per second is small, (e.g., large VII select count), a long display period is best.

8.4.2 Elapsed Time Counters

The elapsed time counters maintain a total of elapsed minutes and seconds since the beginning of the interrupt timing test. They run at the same time as the interval timer but produce no external display unless requested. When a request is made, the current elapsed time is computed and output. During this computation, the interval timer takes second priority and thus may miss intervals. Shortly after the elapsed time has been output, the interval timer will return to normal operation.

The elapsed time counter may also be requested to reset its counters. This will also restart the interval timer.

On the 620-22 i, 620 L, the interval interrupt drives the elapsed time counter and its current value is output on request. On the 73 and 620 f, both the variable interval interrupt and the free running counter drive elapsed time counters and thus two values are output when a request is made.

8.5 LOADING PROCEDURE

The test executive must be loaded before the real-time clock test program will operate correctly. Teletype input/output subroutines resident in the test executive are called by the RTC program.

- a. Load the test executive, which includes the binary object tape loader, per the procedure outlined in section 2. Begin execution either at the Teletype mode starting address or the console-mode starting address.

continued



REAL-TIME CLOCK TEST PROGRAM

For all CPU's, the test program will request:

INPUT BASIC INTERRUPTS PER SECOND

The operator inputs the decimal number followed by a period. The correct value depends on the hardwired selectable clock source. The following are acceptable inputs and their corresponding sources. The first is the standard value.

For 73 and 620/f:

SOURCE	BASIC INTERRUPTS PER SECOND
Crystal Controlled Oscillator	10000
Line Frequency	60 (or 50 for 50 Hz)
Customer's External Source	Appropriate Value

For 620/i, 620/L and 622/i:

SOURCE	BASIC INTERRUPTS PER SECOND
Standard Source	1000
Customer's External Source	Frequency (in Hz) divided by 8.

8.6.2.3 Interrupt Timing Test Inputs

After the RTC hardware setup has been defined, the interrupt-timing test is begun. The test types 'INTERRUPT TIMING TEST' to identify itself and then requests the test parameters.

For the 73 and 620/f the following requests are made:

INTERVAL TIMER =

Typing '0.' will result in the FRC driving the interval timer. Typing '1.' will result in the VII being used instead.

VII SELECT COUNT =

This count is used to vary the VII rate. The user should type in a decimal number from 1 to 4095, followed by a period. 10 is the standard value.

INTERVAL DISPLAY PERIOD IN SECONDS =

This sets the number of seconds to be measured by the interval timer. Type in a decimal number followed by a period. If the number typed exceeds the interval timer capacity, 'unacceptable' will be typed out and the request repeated.

For the 620/i, 620/L and 622/i, only the 'interval display period' request will be made out of the above three questions. This is because the interval interrupt alone is available on those CPU's for timing intervals. Also, those CPU's do not permit varying the interval interrupt with the select count.

8.6.2.4 Interrupt Timing Test Execution

Once the above initialization has been completed, the test program outputs

BEGIN TEST

and starts the interval timer and elapsed time counters. During execution, communication through the Teletype is in the following manner:

CHARACTER TYPED	RESULT
Space	Values of elapsed time counters typed
R	All counters and timers reset
K	Return to initialization
Any other character	No effect

The test continues until interrupted by sense switch settings or console interrupt.

The format for the elapsed-time printout is as follows:

For 73 and 620/f:

```
(V)II:    x MIN.    y SEC.
FRC:      x MIN.    y SEC.
```

For 620/i, 620/L and 622/i:

```
(V)II:    x MIN.    y SEC.
```

8.6.3 Computer Console Mode of Operation

If a Teletype is not available or is partially inoperative, execute the RTC test using the following procedure:

The Loading Procedure is the same as that for Teletype operation.

8.6.3.1 Initialization

Execute the RTC test. The test will first halt with 0 in the instruction register. The user then sets the A register to "0" if the computer is a 620/i, 620/L or 622/i. Set the A register to "1" if the computer is a 73 or 620/f. The computer is then restarted either by hitting "RUN" or by setting the "STEP/RUN" switch to "RUN" and then hitting "START".

For the 73 and 620/f, the test program next halts with 020 in the instruction register. The operator should enter the FRC increments per second in double-precision octal in the A and B registers. Restart from the halt as before. This halt will not be made for the 620/i, 620/L, and 622/i.



INTERVAL TIMER = x.

Where x = 0 for FRC
= 1 for VII

VII SELECT COUNT = xxxx.

Where xxxx. is a decimal number followed by a period, from 1 to 4095.

INTERVAL DISPLAY PERIOD IN SECONDS = xxx.

Where xxx. is a decimal number, followed by a period.

8.9 ERROR INDICATIONS

ERROR CODE DESCRIPTION (Error code is in the instruction register)

ERROR CODE	DESCRIPTION
1	Initialized RTC and enabled RTC interrupt did not cause a (Variable) Interval Interrupt.
2	Inhibit (Variable) Interval Interrupt did not inhibit interrupt.
3	Initialize Variable Interval Interrupt and enable (Variable) Interval Interrupt did not cause interrupt.
4	Initialize RTC and enable RTC with increment and replace count of 037775 did not cause an overflow interrupt.
5	Upon receiving MOI the memory count value was not 040001.
6	Inhibit MOI did not inhibit MOI interrupt.
7	Inhibit MOI inhibiting (V)II also.
10	Enable (V)II and inhibiting MOI not inhibiting MOI.
11	Free running counter not incrementing.
12	Clear FRC not clearing counter.

ERROR HALT DESCRIPTIONS

Instruction Register	Description
000400 to 00777	Illegal interrupt to a non-real-time clock interrupt address. 000 to 0377; A, B, and X have no meaning.
000	Console-mode halt A = 0 Operator set A register to 1 for 73 and 620/f or leaves as 0 for the other CPU's.
020	Console-mode halt. X = B = A = 0 The operator stores the following in each register and pushes run. A, B = Double precision free running counter increments per second.
021	Console-mode halt. X = B = A = 0 The operator stores the following in each register and pushes run. A, B = Double precision (Variable) Interval Interrupts per second.
022	Console-mode halt X = B = A = 0 Initialization for interrupt timing test operator stores the following in each register and pushes run: A = Interval timer B = VII Select count X = Display period.
023	Console mode halt for communication with elapsed time counters. A, B registers contain the elapsed time.
001 to 012	I/O Instruction and Interrupt Test error. A = Error Code No. (01 to 012) (see 2.6 for error description) B = Location calling error routine X = 0



SECTION 9

620/f AND V73 MEMORY-PROTECTION TEST PROGRAM

The Memory Protection Test Program of MAINTAIN II tests the operation of the 73 system and 620/f memory protection (MP) option, which is not applicable to other 620-series computers.

The MP partitions core memory so that the contents of certain memory areas (designated protected areas) cannot be altered by programs operating in unprotected areas. Memory is partitioned into equal blocks of 512 words. A 4,096-word memory increment is divided into eight such blocks. Each area can then be selectively designated protected or unprotected.

When a program is operating from an unprotected area, the following operations are prohibited:

- a. Writing in a protected area
- b. Jumping to a protected area
- c. All I/O instructions from an unprotected area
- d. Program overflow into a protected area
- e. Executing a halt instruction

If these operations are attempted, the program aborts and jumps to one of eight preassigned memory addresses. From these addresses, the program can be directed to a user-written subroutine for analysis and correction.

Programs operating from a protected area of memory do not have the above-described limitations.

For a detailed description of the MP, refer to the appropriate maintenance manual.

The MP test program is designed to test ONLY the 620/f and V73 MP options.

9.1 PROGRAM DESIGN SUMMARY

The MP test program consists of two subtests:

- a. Mask-register test
- b. Instruction interrupt address test

9.1.1 Mask-Register Test

This test verifies that the MP establishes protected and unprotected areas in memory. The MP contains one 16-bit mask register for each 8,192 words of memory. Each mask register bit controls 512 words. If the mask register bit is zero, the corresponding 512-word area is protected; if one, unprotected. Mask register 0 controls the lowest-order 8,192 words of memory, and mask register 3, the highest-

order 8,192 words. This test is identical for the 620/f and V73.

The mask register test executes the following seven subtests on each 512-word memory block.

- a. Enable MP
- b. Disable MP
- c. Set mask registers
- d. Reset mask registers
- e. High block boundary
- f. Low block boundary
- g. Instruction address register

At the beginning of each block test, memory addresses to be modified in the test are saved; they are restored at the conclusion of a block test. Interrupt addresses contain Jump and Mark (JMPM) instructions to an error-reporting subroutine, except programmed interrupts.

The mask Register Test assumes that the memory-protect Jump-error detection is working properly.

9.1.2 Instruction Interrupt Address Test

This test verifies that the MP detects invalid operations and initiates appropriate interrupt action. Invalid operations and their solutions are:

- a. **Write Error.** Data cannot be stored in a protected area. If this is attempted, the write instruction is modified to a read instruction to protect memory, the A, B, and instruction registers are unchanged, and the program executes a JMPM to the error-processing subroutine at address 000024 (or 000034 if overflow also exists).
- b. **Jump Error.** When a program is operating from an unprotected area, it cannot execute a Jump (JMP) instruction to a protected area. If this is attempted the P register remains unchanged, and, if the instruction is a JMPM, the write instruction is modified to a read instruction. The program then executes a JMPM to address 000026 (or 000036 if overflow also exists).
- c. **I/O Error.** If execution of an I/O instruction is attempted from an unprotected area, the I/O instruction is inhibited, and the program executes a JMPM to address 000022 (or 000032 if overflow also exists).

continued



620/f AND V73 MEMORY-PROTECTION TEST PROGRAM

- b. If 620/f is specified, the following message is output:

OPTIONAL INST. PRESENT 0 = YES 1 = NO

If testing the 620/f containing the optional instruction set (document number 98 A 9908 430), type a 0, followed by a period. If the 620/f does not contain the optional instruction set, type a 1, followed by a period.

- c. The program then outputs the message:

START TEST 0. =MASK REG. OR 1. =INST TEST

- d. Type a 0, followed by a period, to execute the mask register test or type a 1, followed by a period, to execute the instruction interrupt-address test first.

- e. The program then outputs the message:

CYCLES =

- f. Type one of the following:

Response	Description
A period	Specifies continuous testing and suppression of nonerror messages
A comma	Specifies continuous testing and output of nonerror messages
An octal number, followed by a period	Specifies test termination after the designated number of cycles and suppression of nonerror messages
An octal number, followed by a comma	Specifies test termination after the designated number of cycles and output of nonerror messages

With each response, the test can be terminated at the completion of the current cycle by setting SENSE switch 3. The maximum number of cycles that can be specified is 077777 (32,768 decimal). Zero specifies continuous test execution.

- g. The program then outputs the message:*

MASK REG. TEST

- h. The mask register test is automatically executed and, if nonerror message output is not suppressed, the program outputs the message:

INST. INT. ADDR. TEST

- i. The instruction interrupt address test is automatically executed, and, when the requested number of cycles of

the complete test are complete, the program outputs the message:

**MP TEST COMPLETE
CYCLES =**

* If the test is started with the INST. TEST, the message outputs of steps g and h will be reversed.

9.5.2 Control Panel Mode of Operation

If the TTY is not included in the system or is partially inoperative, the MP test program can be executed in control panel mode. In this case, start the test executive program (chapter II) with 006152 in the P register.

After successful loading:

- Load 003010 in the P register.
- Press START.

The program halts with 000077 in the instruction register and zero in the A, B, and X registers.

- Load the number of cycles in the A register.
- In the B register, load zero if the optional instruction set is included in the system, one if it is not.
- In the X register, load zero to execute the mask register test first, one to execute the instruction interrupt address test first.
- Press START.
- The program halts with 000077 in the I register and nonzero in the A register. If the A register contains minus one, indirect addressing is not limited. If the A register contents are positive, they indicate the indirect addressing level attained.
- Press START.

The test then runs continuously until the specified number of cycles have been executed or until terminated by the operator.

Return control to the test executive by pressing the INT switch.

To return to the MP test program from the test executive, type:

G500.

The value 500 represents the starting address for the MP test program initialization routine. The actual starting address of the program is 003010, after initial conditions are established.



620/f AND V73 MEMORY-PROTECTION TEST PROGRAM

Error Code	Test Description	Expected Result
07	Execute a JMP instruction with the jump condition not met and the second word in the last address of an unprotected memory block	Interrupt to over-flow address
010	Execute an XEC instruction that executes a halt in unprotected memory and with the second word in the last address of an unprotected memory block	1. Interrupt to over-flow address for 620/f 2. Interrupt to halt address for 73 system
011	Execute an INRE (indirect) through protected-to-unprotected memory with the second word on INR in the last address of an unprotected memory block	Interrupt to over-flow address
012	Execute a two-word extended read instruction (non-INR) with the second word in the last address of unprotected memory	Interrupt to over-flow address
013	Execute an extended write to unprotected memory instruction with the second word of the instruction in the last address of unprotected memory	Interrupt to over-flow address
014	Execute a one-word I/O instruction in unprotected memory	Interrupt to I/O address
015	Execute a one-word I/O instruction in unprotected memory using an XEC instruction in protected memory	No error
016	Execute a one-word I/O instruction in unprotected memory using an XEC instruction in unprotected memory	Interrupt to I/O address
017	Execute a one-word I/O instruction in protected memory using an XEC instruction in unprotected memory	Interrupt to I/O address
020	Execute a two-word I/O instruction with the second word in the last address of unprotected memory	Interrupt to I/O overflow address
021	In unprotected memory, execute a one-word write instruction that writes in protected memory	Interrupt to write address
022	In unprotected memory, execute a two-word write instruction that writes in protected memory	Interrupt to write address
023	In unprotected memory, execute a one-word write instruction that writes in unprotected memory	No interrupt



Control Panel Mode of Operation

In this mode, if the program halts during execution, the instruction register contains one of the following error codes describing the type of error; the volatile register contents define error conditions.

Mask Register Test

Error Code	Description
000001 to 000007	<p>If the A register contents are not equal to zero, indicates one of seven possible errors in this subtest:</p> <p>A register = one of the 512-word memory blocks</p> <p>000001 = addresses 001000 to 001777</p> <p>000002 = addresses 002000 to 002777</p> <p>etc.</p> <p>B register = error code</p> <p>000001 = bottom of block boundary test failed</p> <p>000002 = top of block boundary test failed</p> <p>000003 = interrupt occurred when disabled in unprotected area</p> <p>000004 = interrupt occurred when disabled in protected area</p> <p>000005 = interrupt occurred when enabled in protected area</p> <p>000006 = interrupt did not occur when enabled in protected area</p> <p>000007 = incorrect address in the instruction address register</p> <p>X register = error address</p>

Instruction Interrupt Address Test

Error Code	Description
000001 to 000037	<p>Defines a type of instruction interrupt address halt:</p> <p>A register = zero</p> <p>B register = error code (refer to section 3.1.1, column Expected Result)</p> <p>X register = error address</p>
000101 to 000137	<p>Defines a particular instruction address test error:</p> <p>A register = zero</p> <p>B register = error code (refer to section 3.1.1, column Description of Test)</p> <p>X register = error address</p>
000400 to 000777	<p>Illegal interrupt to a non-MP interrupt address (000000 to 000377). A, B, and X register contents have no significance.</p>



EXAMPLE 4

V73

```
MEMORY PROTECT TEST
ENTER CPU TYPE 0 = 620/f      1 = V73
1.
START TEST      0. = MASK REG. OR 1. = INST. TEST
0.
CYCLES = 4,
MASK REG. TEST
INSTR. INT. ADDR. TEST
MASK REG. TEST
INSTR. INT. ADDR. TEST
MASK REG. TEST
INSTR. INT. ADDR. TEST
MASK REG. TEST
INSTR. INT. ADDR. TEST
MP TEST COMPLETE
CYCLES =
```

EXAMPLE 5

Running the test on a V73 but specifying 620/f.

```
MEMORY PROTECT TEST
ENTER CPU TYPE 0 = 620/f      1 = V73
0.
OPTIONAL INST. PRESENT  0. = YES,      1. = NO
0.
START TEST      0. = MASK REG. OR 1. = INST. TEST
0.
CYCLES = 2,
MASK REG. TEST
INSTR. INT. ADDR. TEST
ERROR TYPE = 000101
ERROR TYPE = 000010
MASK REG. TEST
INSTR. INT. ADDR. TEST
ERROR TYPE = 000101
ERROR TYPE = 000010
MP TEST COMPLETE
CYCLES =
```




SECTION 10

BUFFERED-I/O-CONTROLLER TEST PROGRAM

The buffered I/O controller test program of MAINTAIN II tests the operation of the 73 system and 620-series buffered I/O controller (BIOC) options.

The BIOC monitors 16- or 18-bit word transfers between the CPU I/O bus and an external device. The data are transferred under program control or, optionally, under the control of the buffer interface controller (BIC). The BIOC can also send a control signal (on up to four channels) to the external device and receive a sense signal (on up to eight lines) from it. In addition, the BIOC processes four interrupt lines in route to the priority interrupt module (PIM) if included in the computer system.

Computer control is extended to external devices through the BIOC. All BIOC functions are programmable.

The BIOC responds directly to three external control, one sense, and three data transfer instructions (table 10-1). A typical service routine is given in table 10-2.

Program Design Summary

The BIOC test program consists of five subtests:

- a. I/O register test (subtest 1)
- b. Pulse output test (subtest 2)
- c. Sense line test (subtest 3)
- d. Load input buffer via BIC (subtest 4)
- e. Load output buffer via BIC (subtest 5)

The subtests can be individually selected for execution; the number of test cycles can also be specified.

If the tested system contains more than one BIOC, each can be tested by specifying the appropriate device address at the beginning of the test.

Table 10-1. BIOC Input/Output Instructions

Mnemonic	Code	Description
External Control		
EXC 0x62	0100x62	Output a control pulse on line x (x = 00 through 03)
EXC 0662	0100662	Connect the BIOC for output
EXC 0762	0100762	Connect the BIOC for input
Sense		
SEN 0x62	0101x62	Test the state of line x (x = 00 through 07)
Data Transfer		
OME 062	0103062	Load the output buffer register from memory
OAR 0162	0103162	Load the output buffer register from the A register
OBR 0262	0103262	Load the output buffer register from the B register

Data input transfers are under the control of the BIC.



10.2 EXECUTING THE BIOC TEST PROGRAM

10.2.1 Teletype Mode of Operation

The BIOC can be operated in either Teletype or control-panel mode. In Teletype mode after successful loading of the BIOC test program, the test program outputs the messages:

BUFFERED I/O TEST

ENTER BUFFER I/O DEVICE ADDRESS

On the TTY, type the appropriate device address, followed by a period. The program then outputs the message:

BIC TO BE USED (Y/N)

If the BIC capability is not to be tested, type an N. If it is, type a Y. If the response is Y, the program outputs the message:

ENTER BIC DEVICE ADDRESS

Type the BIC device address, followed by a period. The program then outputs the message:

ENTER SUBTEST NUMBER

CAUTION

Before attempting subtest execution, connect the appropriate test cable to circulate data between the BIOC input and output registers.

Subtests 1, 4, 5	Test cable A
Subtests 2, 3	Test cable B

Refer to the applicable system test specification and/or engineering description for connection procedures.

A clock signal for testing under BIC control must also be provided.

Type the desired subtest number, followed by a period. This last message is output immediately after the **BIC TO BE USED** message if the response to that message is an N.

Following entry of the subtest number, the program outputs the message:

CYCLES =

Type the desired number of test cycles, followed by a period. If a zero is input, the test cycles continuously until terminated by the setting of SENSE switch 3. The program indicates termination of each subtest by requesting a new subtest number.

If more than one BIOC is included in the system, set, then reset, SENSE switch 3 to return to the beginning of the BIOC test program for a new device assignment.

10.2.2 Control Panel Mode of Operation

If the Teletype is not included in the system or is partially inoperative, the BIOC test program can be executed in control panel mode. In this case, start the test executive program (section 2) with 06152 in the P register.

After successful program loading:

- Load 000500 in the P register.
- Press START or RUN.

The program halts with 000001 in the instruction register and zeros in the A, B, and X registers.

- Load the BIOC device address in the A register.
- Load the BIC device address in the B register, if applicable.
- Press START or RUN.

The program halts with 000002 in the instruction register.

- Load the number of the subtest to be executed (section 1.1) in the A register.
- Load the number of test cycles in the B register (all ones specifies continuous execution).
- Press START or RUN.

The program will run continuously until the specified number of cycles have been executed and halt with 000002 in the instruction register for selection of another subtest.

To return to the beginning of the BIOC test program, set, then reset, SENSE switch 3.

To terminate the BIOC test program and return to the test executive when testing the 620/i, 620/L, or 622/i computers:

- Clear the instruction register.
- Load 007000 in the P register.
- Press SYSTEM RESET.
- Press RUN two times.

When testing the 620/f computer, return control to the test executive by pressing the INT switch.

To return to the BIOC test program from the test executive, type:

G500.

on the TTY. In control panel mode, load 000500 in the P register and press START or RUN.



BUFFERED-I/O-CONTROLLER TEST PROGRAM

EXAMPLE 3:

Execute subtests 1 and 4 using the wrong test cable (B).

BUFFERED I/O TEST

ENTER BUFFERED I/O DEVICE ADDRESS 60.

BIC TO BE USED (Y/N) N

ENTER SUBTEST NUMBER 1.

CYCLES = 1.

OUTPUT	000001	INPUT	000000
OUTPUT	000002	INPUT	000000
OUTPUT	000003	INPUT	000000
OUTPUT	000004	INPUT	000000
.	.	.	.
.	.	.	.
.	.	.	.

ENTER SUBTEST NUMBER 4.

CYCLES = 1.

OUTPUT	177777	INPUT	000000
OUTPUT	177777	INPUT	000000
OUTPUT	177777	INPUT	000000
OUTPUT	177777	INPUT	000000
OUTPUT	177777	INPUT	000000
.	.	.	.
.	.	.	.
.	.	.	.

ENTER SUBTEST NUMBER

EXAMPLE 4:

Execute subtests 2 and 3 using the wrong test cable (A).

BUFFERED I/O TEST

ENTER BUFFERED I/O DEVICE ADDRESS 60.

BIC TO BE USED (Y/N) Y

ENTER BIC DEVICE ADDRESS 20.

ENTER SUBTEST NUMBER 2.

CYCLES = 1.

000377
000377
000377
000377
000377
000377
000377
000377
000377

ENTER SUBTEST NUMBER 3.

CYCLES = 1.

IR RESET ERROR

IR RESET ERROR

IR RESET ERROR

IR RESET ERROR

IR RESET ERROR

IR RESET ERROR

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EXAMPLE 5:

Execute subtest 4, specifying continuous execution. Terminate the test by setting SENSE switch 3.

ENTER SUBTEST NUMBER 4.

CYCLES = 0.

BUFFERED I/O TEST

RESET SENSE SWITCH 3

RESET SENSE SWITCH 3

Note that if the test is restarted with SENSE switch 3 remaining set the program requests that the switch be reset.



APPENDIX A

CONSOLE OPERATION:

Differences Between Varian 73 and 620-f

	620/f	Varian 73
Power Switch	"OFF" - All power voltages off.	"OFF" Same as 620/f
	No corresponding position.	"HOLD" - All power voltages off except those required to preserve contents of semiconductor memory.
	"PWR ON" - All power voltage on and console switches enables.	"ON" Same as 620/f
	"PWR ON DISABLE" All power voltages on and all console switches (except powerswitch) disabled.	"CONSOLE DISABLE" All power voltages on and all console switches (except power switch and display select) disabled.
STEP/RUN Switch and STEP and RUN Indicators	<p>The "STEP/RUN" switch locks in either STEP or RUN position.</p> <p>If computer is in step mode:</p> <p>a. Pressing STEP/RUN switch to RUN position primes the computer to enter the run mode when the START switch is pressed. The step indicator remains on.</p> <p>b. Pressing the START switch executes the instruction in the I register, and fetches the next instruction from the address specified by contents of the P register and places it in the I register. The STEP indicator goes out and the RUN indicator lights</p> <p>If computer is in run mode:</p> <p>a. Lifting STEP/RUN switch to STEP halts computer after completing execution of the current instruction and fetches the</p>	<p>The "STEP/RUN" switch is alternate action.</p> <p>If computer is in step mode:</p> <p>a. Pressing STEP/RUN switch primes the computer to enter the run mode when the START switch is pressed. The step indicator is extinguished and the RUN indicator links.</p> <p>b. Same as 620/f</p> <p>If computer is in run mode:</p> <p>a. Pressing the STEP/RUN switch halts the computer after completing execution of the current instructions and fetches the next instruction and sets it in the I register. The RUN</p>



620/f

Switches mechanically latch on. Previously selected switch must be turned off before next selection is made.

REG SELECT (1
2, 4, 8) CLEAR
and INCR Switches
and Indicators

These switches correspond to A, B, and X REGISTER switches in use.

REGISTER Entry
Switches and
DISPLAY Indicators
(DISPL CLR)
(LOAD)

- a. The 16 indicators display contents of a selected register when the computer is in the step mode.
- b. To display the contents of a register place the STEP/RUN switch to STEP and press the REGISTER switch for the desired register.
- c. The display indicators light when they

Varian 73

display. A, B, and X are general registers 0, 1, and 2 respectively.

Only one register can be selected at a time. Pressing two or more register switches simultaneously can result in an invalid display.

Switches electronically latch on. Indicators above switches designate selected registers. Pressing a new selection automatically cancels the previous selection.

Used in conjunction with the REG switch. Used to designate one of 16 general registers for display or entry. The desired register is selected by entering the appropriate binary code via the register select switches. The binary values of each switch are indicated above (8, 4, 2, 1). Switches are momentary. Pressing any of the 4 select switches causes that bit to be set and the corresponding indicator to light. To reset all 4 bits press the CLEAR switch. The INCR switch causes the selected register number to be incremented by one each time the switch is pressed. The binary codes for the A, B, and X registers are:

	8	4	2	1
A	0	0	0	0
B	0	0	0	1
X	0	0	1	0

- a. Same as 620/f
- b. To display the contents of a register press the STEP/RUN button (if the RUN indicator is on) and press the desired switch in the DISPLAY SELECT group. If REG is selected set the proper binary code into the REG SELECT group.
- c. Same as 620/f.



620/f

Varian 73

ister press REPEAT, and then press START. The instruction is executed again and the program counter advanced. However, the contents of the I register remain the same. This switch is used in entering or displaying memory data in sequential locations.

SENSE Switches (and Indicators)

The three SENSE switches are toggle switches permitting program modification by the operator.

The three SENSE switches are alternate action switches permitting program modification by the operator. The indicators display the current status of the switches. Pressing any sense switch changes the status of the corresponding switch from off to on or on to off.

INT (Interrupt) Switch

INT is a momentary switch used to interrupt the computer. It is functional only when the computer is in the run mode.

INT is a momentary switch used to interrupt the computer. It is functional only when the computer is in the run mode (RUN indicator on constantly).

RESET Switch

RESET is a momentary switch used for initializing control and for stopping I/O operations. Pressing this switch halts the computer and initializes the computer and peripherals. This switch is electrically interlocked with the STEP/RUN switch and is disabled when the latter is in RUN.

RESET is a momentary switch used for initializing control and for stopping I/O operations. Pressing this switch halts the computer and initializes the computer and peripherals. It is not interlocked with the STEP/RUN switch on display.

OVFL (Overflow) Indicator (Bit 8 of STATUS Display)

OVFL lights whenever an overflow exists. This is true when the computer is in either STEP or RUN mode.

Overflow may only be observed with the computer halted (STEP indicator on or RUN indicator blinking.) It may be observed by pressing the STATUS switch noting to state of bit 8. Bit 8 is on whenever an overflow condition exists.

ALARM Indicator

Alarm lights to signal an overheated system.

No corresponding indicator exists.

Loading Sequential Memory Addresses

a. Set STEP/RUN to STEP and press REPEAT

a. Place the computer in the STEP mode by pressing



	620/f	Varian 73
Executing of a Stored Program (Manually)	<p>a. Select step mode and turn off REPEAT.</p> <p>b. Set the P register to the first address of the program.</p> <p>c. Clear the I register.</p> <p>d. Press START</p> <p>e. Press START again to execute the instruction and to load the next instruction with the I register.</p> <p>f. Repeat step e once for each instruction.</p>	<p>a. Select step mode by pressing the STEP/RUN switch if the RUN light is on blinking.</p> <p>b. Same as 620/f</p> <p>c. Same as 620/f</p> <p>d. Same as 620/f</p> <p>e. Same as 620/f</p> <p>f. Same as 620/f</p>
MISCELLANEOUS		<p>a. Alternation of the contents of general registers $\equiv 4$ while the step mode (run indicator blinking or step indicator on) is equivalent to altering the contents of I.</p> <p>b. General register R3 contains zeroes while in the step mode and cannot be manually altered.</p> <p>c. General register R5 contains ones while in the step mode and cannot be manually altered.</p> <p>d. Pressing the I Display Selection clears the REG select display.</p> <p>e. To use the TSA instruction the MEM display selection should be made.</p> <p>f. While the computer is running I/O data input or operations to device code octal 77 addresses the console display.</p> <p>g. Console display indicators only represent actual register contents while the computer is not in the run mode.</p>

