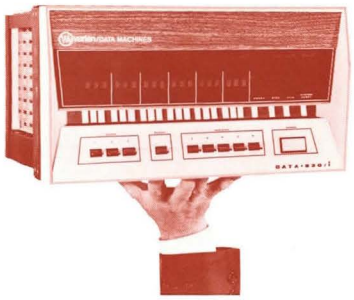

DATA 620/i
systems computer

varian data machines

varian/DATA MACHINES
SENSE
1
2
3
REPEAT
REGISTER
X
B
A
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FEATURES OF THE DATA 620/i SERIES COMPUTERS

- Field Proven Software
- Silicon Monolithic Integrated Circuits (DTL and TTL)
- 9 Hardware Registers
- Over 100 Basic Commands
- 6 Addressing Modes
- Direct Addressing to 2,048 or 32,768 Words
- 16 or 18 Bit Words
- Expansion to 32,768 Words
- Hardware Index Registers
- Party Line I/O Facility
- Micro-EXEC Option
- 10-1/2″ of Rack Space
- Less than 70 lbs. (mainframe and power supply)
- 340 Watts
- NPN or PNP (Optional) I/O Levels
- Interface Ease
- Compatible with DATA 620 Computer
- Plug-in Expandable
- Low Cost

INTRODUCTION

DATA 620/i is a system-oriented digital computer, designed as a powerful system computer to fill the gap between special purpose digital hardware and general purpose computers. DATA 620/i meets all the requirements of a true system computer—powerful computing ability, easy interfacing, modular design and construction for expandability, integrated circuit reliability, low cost, and compact size.

In addition, DATA 620/i offers a number of features simply not available on other computers—like Party Line communication, quick and easy memory expandability from 4096 to 32,768 words of 16 or 18 bits, and a unique micro-EXEC microstep sequencing technique. DATA 620/i comes with a complete set of field-proven software, developed and perfected on the DATA 620.

DATA 620/i has a bigger instruction set, 1/2 the components, and costs less than any computer in its class. This is why it so efficiently and economically solves system problems previously considered too difficult or expensive for computer solution.

DATA 620/i offers a wide variety of peripherals and options, allowing the user to select only those features specifically required for his application, and providing the optimum amount of computer power per dollar.

THE DATA 620/i

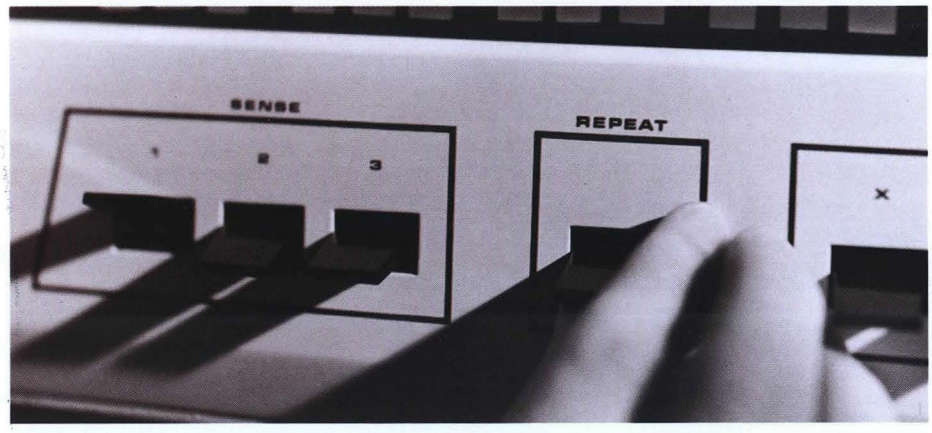
As a physical system component, DATA 620/i processors are compact in size, occupying only 10.5 inches of rack space. They are accessible from the front like other system components, and they are reliable and

maintainable. The contents of five operational registers can be displayed on the front panel.

Eighty-five percent of the processor operation can be verified from the front panel without the use of an oscilloscope. As the controlling element in a system, a DATA 620/i has the "raw" data manipulating power of a much more costly computer. The instruction set includes over 100 basic machine commands. The register change command is micro-programmable with over 100 useful combinations. The processing characteristic can be adapted to specific requirements through an optional Micro-EXEC facility that permits software programs to be hardware implemented.

THE DATA 620/i INTERFACE

The DATA 620/i series was designed to not only provide the complete



spectrum of interface capabilities required in a system computer, but to also allow the user to tailor the computer for his specific application. To attain this goal, all of the Input/Output features are offered as options. Among these facilities are: Direct Memory Access, Real Time Clock, Power Failure Protect, and the Buffer Interlace Controller. These features, combined with priority interrupts, external sense lines, external control lines and the proprietary Micro-EXEC technique give the DATA 620/i family virtually every I/O capability available.

THE DATA 620/i USER INTERFACE

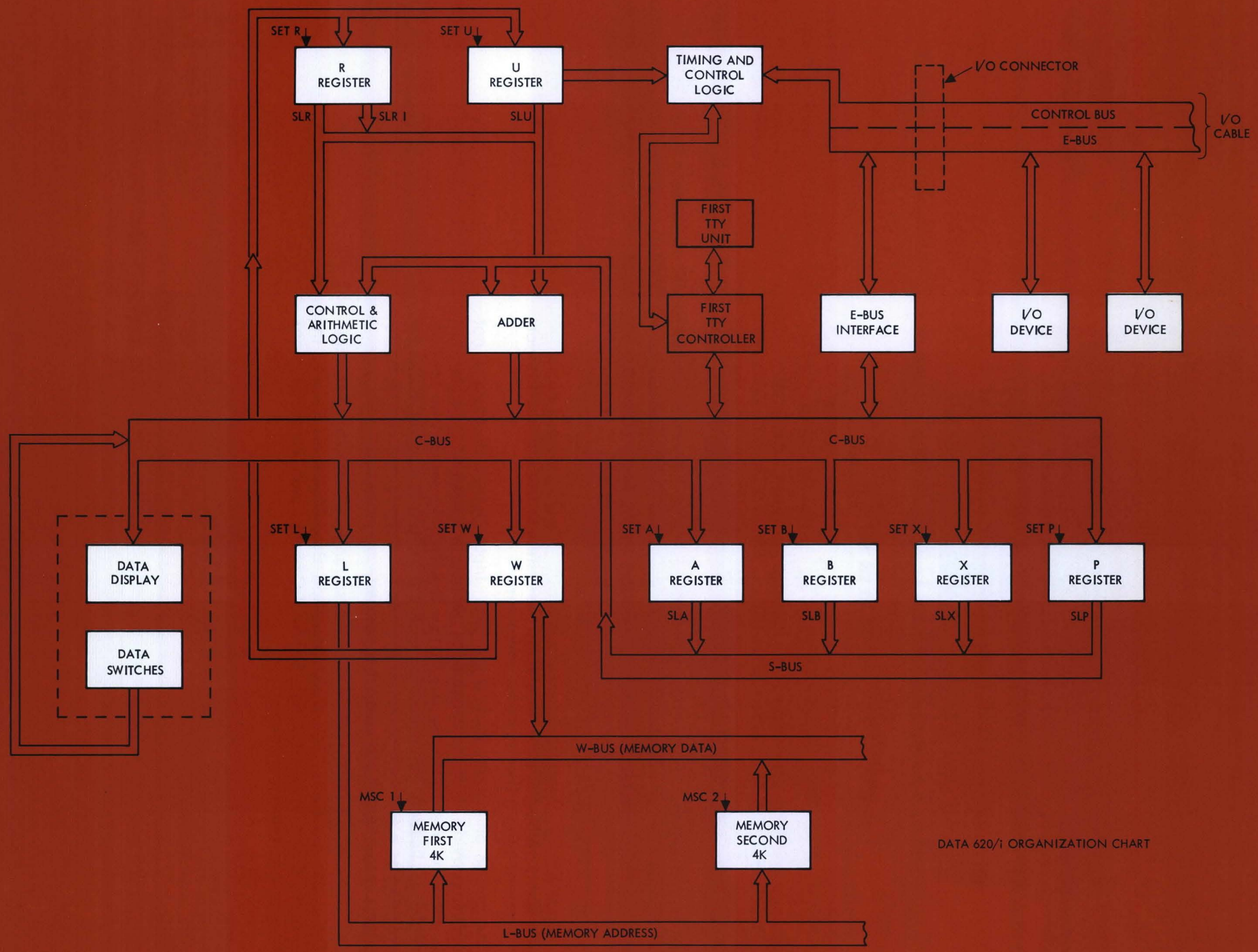
As must be the case in any machine that is required to do—and do well—a large number of data manipulation tasks which are unspecifiable in advance, flexibility was the motif in designing the DATA 620/i software package. The goal was to achieve flexibility without creating big problems on the one hand, or falling into the easy habit of accepting hardware/software tradeoffs on the other hand. In the DATA 620/i, hardware and software features reinforce each other. For example, there are five modes of single-word addressing, one of which permits direct addressing of four times as many words in store as is normally possible with conventional designs. Multiply/divide instructions are available as options to meet more demanding computation speed requirements.

SYSTEM INTERFACE

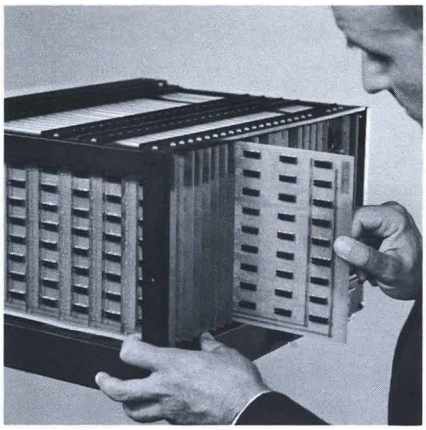
The ability of the computer to adapt to the system is an excellent criterion for determining a true systems computer.

The design philosophy behind the 620/i Input/Output structure is not only to provide all of the capabilities needed in a system computer, but to allow the user to choose the particular capability needed for his particular application. The reasoning is: If the feature is needed, it can be provided as a low cost option; if the need is uncertain, it can be easily added in the field if and when it is needed.

The DATA 620/i family offers the widest range of interface facilities. These include Party Line Communication Bus, Multilevel Priority Interrupts, External Sense Lines, External Control Lines, Direct Memory Access, and Interlace Control.



DATA 620/i ORGANIZATION CHART



ORGANIZATION

The DATA 620/i is organized with a unique bus structure, selection logic, and nine registers. The organization provides universal internal information routing, buffered processing, micro-register change programming facility, information indexing without time penalty, and the optional Direct Memory Access (cycle stealing) facility.

The organization optimizes the DATA 620/i for maximum I/O throughput, minimum elapsed time between successive input or output transfers, and minimum programming.

This unique organization makes possible the optional Micro-EXEC facility by which complex algorithms or additional instructions can be implemented with external hardware. The Micro-EXEC technique produces an increase in processing speed in excess of 500 percent over conventional stored program techniques. The bus structure of this computer

family permits the system designer to overcome traditional barriers of processing speed, high-rate volume throughput, and fixed mainframe characteristics. The four available busses are:

"L" Bus provides a 12-bit parallel communications path from the L Reg to the address decoders in the memory modules

"W" Bus provides a parallel data communications path (16/18 bit) from the W Reg to the memory module(s) (up to 8).

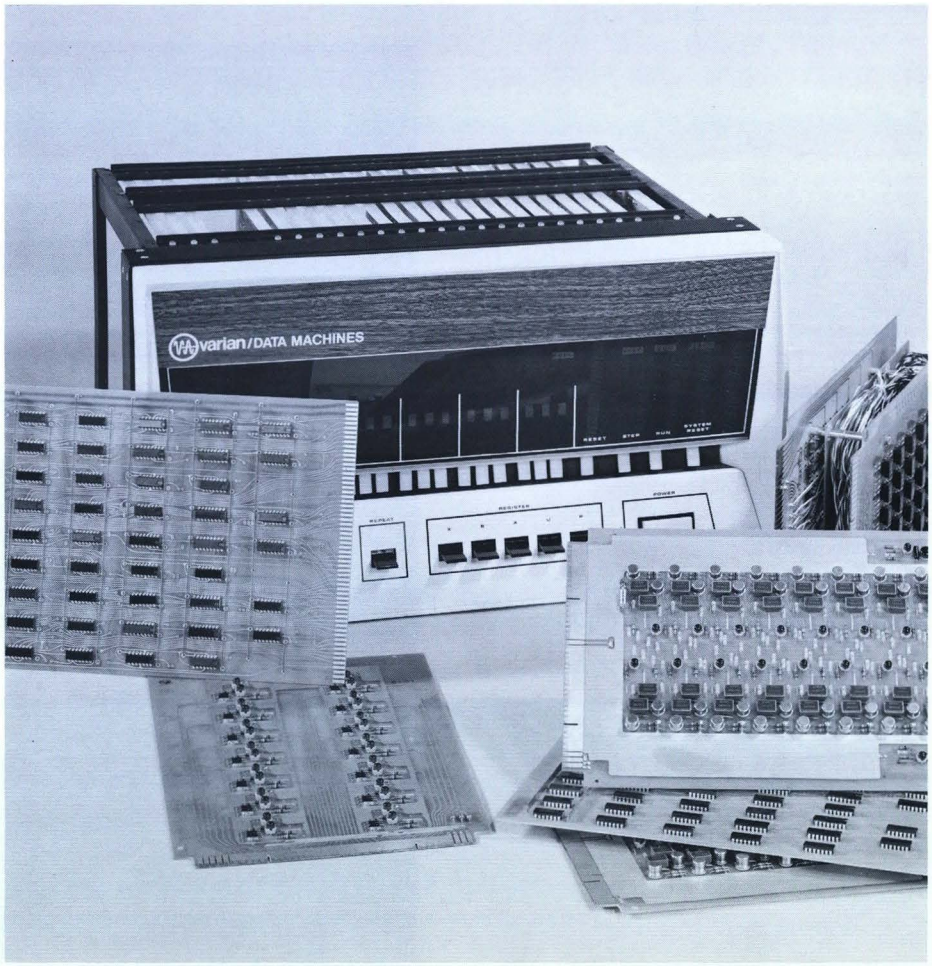
"C" Bus provides the parallel path and selection logic for routing data between the arithmetic unit, the I/O unit, and the operational registers. This bus permits data to be uniquely or commonly transferred to the operational registers. It performs the distribution function for micro-programming, and provides a bi-directional parallel word path to the "Party Line". "C" Bus is the central communication avenue and connects with all internal units of the processor. It is the key facility that permits Micro-EXEC to be implemented.

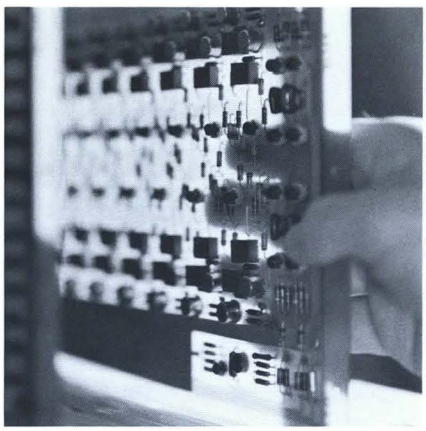
"S" Bus provides the parallel path and selection logic for routing data between the operational registers and the arithmetic unit. It implements the select, gather, and route function for micro-programming and Micro-EXEC.

Party Line I/O Bus provides a 16/18-bit parallel bi-directional I/O communication path. This bus includes the control lines for transfer ready, sense, control, interrupt address and acknowledge, and information entry. The "Party Line" is packaged as one-cable, and each peripheral device has a Party Line connector and a Party Line extender connector. The device and the Party Line form a "daisy chain" whereby additional I/O controllers can be added on site and on a plug-in basis.

REGISTERS

Nine registers are provided with a basic processor. Four of the nine registers are incorporated to provide buffering to satisfy real-time system requirements. All the arithmetic and control unit registers are multipurpose and can serve a unique micro-programming and Micro-EXEC function.





"A" Register is a full-word register and is the high-order half of the accumulator. A is a source and destination for programmed input/output and micro-programming. Micro-EXEC can select, set, shift, and perform arithmetic and logical operations on A.

"B" Register is a full-word register and is the low-order-half of the accumulator. B is a source and destination for programmed input/output, is micro-programmable, and can serve as the second hardware index register. Micro-EXEC can select, set, shift, and perform arithmetic and logical operations on the *"B" Register.*

"X" Register is a full-word register which permits indexing of memory addressing without adding time to accessing an indexed location. The X Register is addressable by the micro-programming instruction set where it serves logical, storage and counting functions. Micro-EXEC can use the X Register for arithmetic and multiple other functions.

"P" Register is a full-word register and is the program counter. P can serve multiple purposes under Micro-EXEC.

"U" Register is a full-word buffer which holds the instruction being executed. The U Register buffers the control unit from memory to permit interlace I/O operation to occur on a memory-cycle by memory-cycle-basis. It is also a multipurpose register available to Micro-EXEC.

"S" Register is a 5-bit register which, in combination with the U Register controls the length of shift instructions. This register also buffers memory from the control unit. S Register is available to Micro-EXEC.

"L" Register is the 12-bit memory location register. Micro-EXEC can select and set the L Register.

"W" Register is the memory word register and is full length (16 or 18 bits). W is selectable and can be set by Micro-EXEC.

"R" Register is a full-word buffer which holds the multiplicand and divisor in arithmetic operations. R Register buffers the arithmetic unit from memory to permit interlace I/O operations to occur on a memory-cycle-steal basis. It is also a multipurpose register available to Micro-EXEC.

Micro-EXEC (Optional) is a technique by which the system designer has the option of externally combining and sequencing the processor's micro-steps to perform a complex macro-function. Over 30 micro-step control lines are made available to the system user. These control functions are the micro-steps normally controlled by machine instructions.

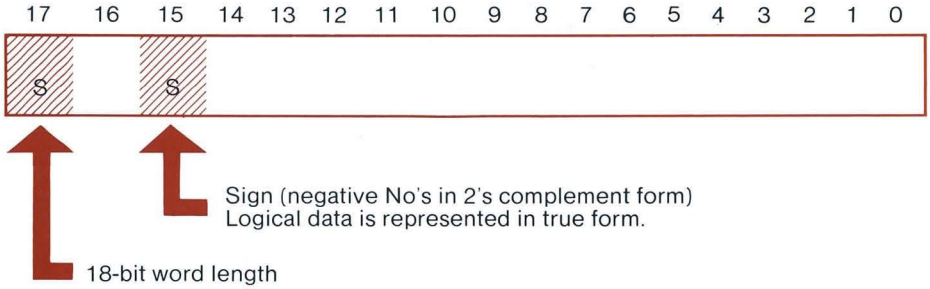
They control memory, arithmetic unit, control unit, all registers, I/O and communication networks. The external control can operate the micro-steps as fast as five every 900 nanoseconds by utilizing the processor clock to synchronize the micro-step operations. Micro-EXEC can be used to implement many types of algorithms. Typical functions are: convolutions, coordinate transformations, double precision arithmetic, table look ups, square root, limit checking, etc. Micro-Control can produce up to 10-to-1 speed advantage over stored programs and does not require core memory for the program. Opening new dimensions to the data system designer, Micro-EXEC makes practical an extremely fast processor with small or large memories. It permits the mode of processing to be controlled externally, and processing to be optimized for the system.

The processor organization and hardware provides the system engineer with the most flexibility available in off-the-shelf equipment. The standard options of Micro-EXEC, machine instructions, memory, and I/O facilities provide functional adaptability and system optimization without engineering risk or unpredictable costs.

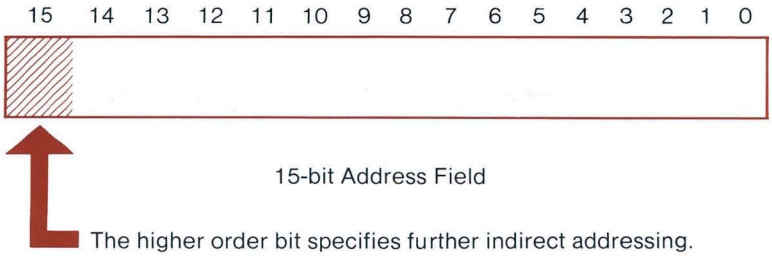
WORD FORMATS

The word formats separate into two categories: data and instruction. Each category has been optimized for the system environment. DATA 620/i processors are available in 16 or 18 bit word length. The 16-bit is the 620/i; the 18-bit version is the 622/i. The data format is extendable for 18-bit words with the sign bit in the high-order positions.

DATA WORD FORMAT



INDIRECT ADDRESS FORMAT

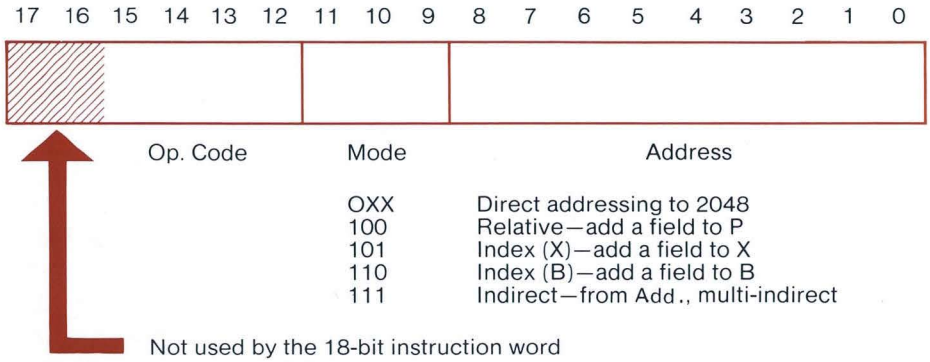


INSTRUCTION WORD FORMAT

The four instruction word formats—single word, double word, generic and macro-command—are illustrated in the following paragraphs:

1. *Single word* Twelve basic commands and two optional commands have single word memory reference formats. The single word instruction is divided into three fields as shown below. There are six addressing modes including direct addressing to 2,048 words, relative to P with a delta range of 512, index by X or B, indirect from the contents of the memory location addressed, immediate.

SINGLE WORD INSTRUCTION FORMAT



Single Word Instructions include: LDA LDB LDX INR ADD SUB MUL* STA STB STX ERA ORA ANA DIV*

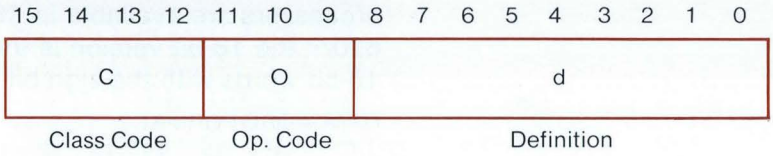
All basic single word instructions are executed in two cycles, including relative and index addressing modes. One cycle is added for each level of indirect addressing.

The single word instruction format is designed to enable the system user to write his programs in the minimum number of memory locations and have his program executed in minimum time. The format is uncomplicated and the fields divide into convenient octal groupings so that programs can be written and checked rapidly.

* *Optional instruction*

2. *Generic* Twenty-six instructions are single word generics and divide into the three fields of class code, operation code and definition.

GENERIC INSTRUCTION FORMAT



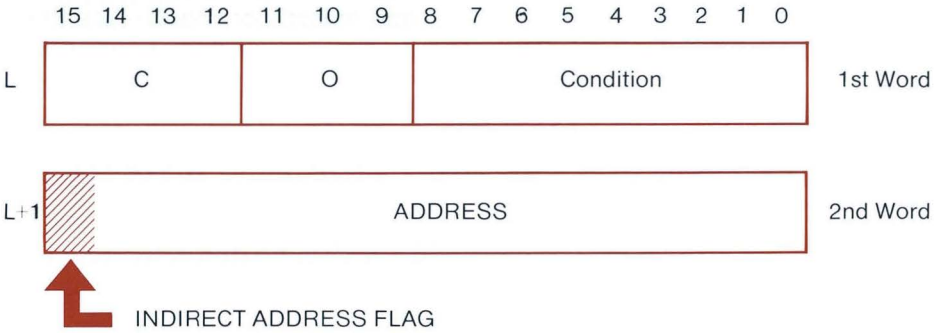
These instructions perform arithmetic unit, control unit and input/output functions. The operations are: HLT, NOP, SHIFTS (12), OVERFLOW (2), SENSE, EXTERNAL FUNCTIONS, INPUT AND OUTPUT, A or B (11).

The shift instructions can shift up to 32 places. The sense and external function instructions can address up to 64 peripheral devices and define up to 8 functions. The input and output commands can select A or B, A and B; clear and input to A or B, A and B. The input/output instructions can address up to 64 devices. (The in-memory and out-memory instructions and the interrupt priority control are two word instructions.)

The generics are octal grouped for user convenience. They provide flexibility to optimize input/output processing.

3. *Two word* Two classes and six types of instructions are two word instructions. The types include: JUMP, JUMP and MARK, EXECUTE, IMMEDIATE, IN/OUT MEMORY, SENSE.

JUMP, JUMP and MARK, EXECUTE



The first word contains three fields: The C field contains the class code, the O field contains the operation code, and the condition field specifies any combination of nine conditions. The nine conditions are: SS1, SS2, SS3, XO, B O, A O, A Neg., A Pos., and Overflow. The second word contains the jump address, jump mark address, or the address of the instruction to be executed. Indirect addressing is permitted. If the specified conditions are all met, the instruction is executed. If the conditions are not met, the second word is skipped and the P Register incremented.

The IN/OUT MEMORY has a similar two word instruction format. The condition field of the IME/OME instruction addresses the device selected; the second word contains the memory address for the data. Indirect addressing is permitted.

IMMEDIATE is a special type instruction. The type includes twelve (plus two optional) two word instructions. The instructions include: LDAI LDBI LDXI ADDI SUBI INRI MULI* STAI STBI STXI ERAI ORAI ANAI DIVI*

* *Optional*

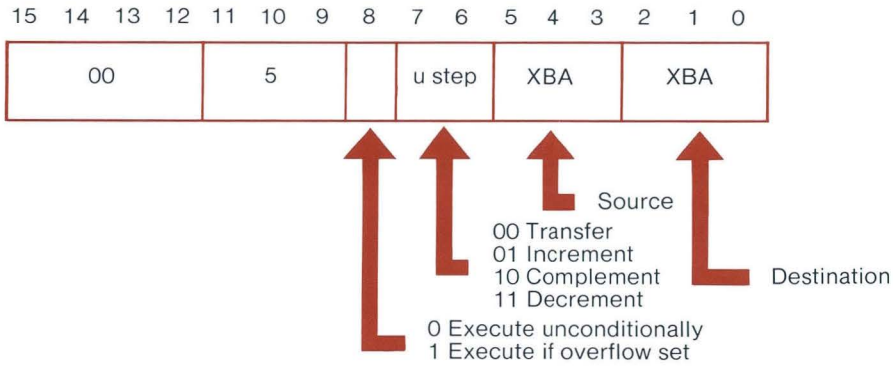
IMMEDIATE INSTRUCTION FORMAT

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
L	00					6					Op. Code						1st Word
L+1	OPERAND																2nd Word

Bits 3 through 6 define one of the instructions above. The IMMEDIATE type instructions provide literal addressing. Literal addressing, being the operand address field, contains the operand. This type automatically increments the P counter; after the execution, the next instruction is obtained from P + 2.

There are a total of 45 standard instructions and over 16 optional two word instructions. The efficiency and power of the two word instructions becomes more and more apparent with use. They provide direct and random addressing and accessing to 32,768 words. In most cases, they permit a two memory location sequence of instruction to replace the usual three memory location sequence. The amount of memory conserved and time saved by these instructions depends on the application, and ranges from 5 to 25 percent.

4. *Macro-commands* A number of micro-steps are programmable into a macro-instruction with the single word "Macro-Command." This command has over 128 useful combinations including those listed in the instruction set. The macro-command format is:



The X, B, and A Register contents can be logical "ORed," cleared, transferred, set to a common value, complemented, "NORed," incremented, decremented, and, if desired, executed conditionally on an overflow. Sequences of micro-commands can be used to perform additional logical functions customary in a system environment.

OPTIONAL INSTRUCTIONS

The hardware multiply/divide and extended addressing option provides an additional 16 instructions to the basic instruction set. The extended address mode is similar in format to the immediate address instructions, except that the second word of the double-word instruction contains the effective address. All single word commands can use extended addressing.

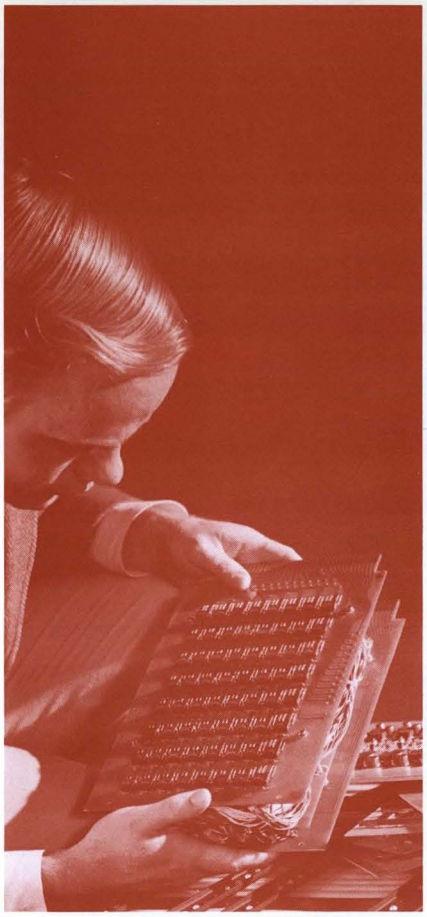
The instruction set is the most comprehensive available with "compact" computers or processors. The optional instruction sets have specific value to certain applications and are available to refine the processors to those applications. The instruction set, variety, simplicity, and power equates to economic optimization. The instruction list is presented in the following table.

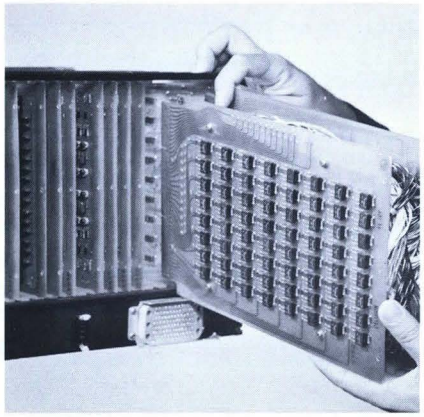
DATA 620/i INSTRUCTION LIST

Type	*Mnemonic*	*Description*	*Time Cycles*
Load	LDA	Load A Register	2
	LDB	Load B Register	2
	LDX	Load X Register	2
Store	STA	Store A Register	2
	STB	Store B Register	2
	STX	Store X Register	2
Arithmetic	ADD	Add to A Register	2
	SUB	Subtract from A Register	2
	INR	Increment and Replace	3
	MUL*	Multiply B Register, Double Length	10
	DIV*	Divide AB Register, Double Length	10-14
Logical	ERA	Exclusive OR to A Register	2
	ORA	Inclusive OR to A Register	2
	ANA	And to A Register	2
Jump	JMP	Jump UNCONDITIONALLY	2
	JOF	Jump if Overflow SET	2
	JAN	Jump if Register NEGATIVE	2
	JAZ	Jump if A Register ZERO	2
	JAP	Jump if Register POSITIVE	2
	JSSI	Jump if Sense Switch 1 is SET	2
	JSS2	Jump if Sense Switch 2 is SET	2
	JSS3	Jump if Sense Switch 3 is SET	2
	JXZ	Jump X Register ZERO	2
	JBZ	Jump B Register ZERO	2
Jump and Mark	JMPM	Jump UNCONDITIONALLY and Mark	2
	JOFM	Jump Overflow SET and Mark	2-3
	JANM	Jump A Register Negative and Mark	2-3
	JAZM	Jump A Register ZERO and Mark	2-3
	JAPM	Jump A Register Positive and Mark	2-3
	JS1M	Jump Sense Switch 1 SET and Mark	2-3
	JS2M	Jump Sense Switch 2 SET and Mark	2-3
	JS3M	Jump Sense Switch 3 SET and Mark	2-3
	JXZM	Jump X Register ZERO and Mark	2-3
	JBZM	Jump B Register Zero and Mark	2-3
Execute	XEC	UNCONDITIONAL Execute	2
	XOF	Execute Overflow SET	2
	XAN	Execute A Register NEGATIVE	2
	XAZ	Execute A Register ZERO	2
	XAP	Execute A Register POSITIVE	2
	XS1	Execute Sense Switch 1 SET	2
	XS2	Execute Sense Switch 2 SET	2
	XS3	Execute Sense Switch 3 SET	2
	XXZ	Execute X Register ZERO	2
	XBZ	Execute B Register ZERO	2
Immediate	LDAI	Load A Register Immediate	2
	LDBI	Load B Register Immediate	2
	LDXI	Load X Register Immediate	2
	STAI	Store A Register Immediate	2
	STBI	Store B Register Immediate	2
	STXI	Store X Register Immediate	2
	ADDI	Add to A Register Immediate	2
	SUBI	Subtract from A Register Immediate	2
	MULI*	Multiply B Register Immediate Double Length	10
	DIVI*	Divide AB Register Immediate Double Length	10-14
	INRI	Increment and Replace Immediate	3
	ERAI	Exclusive OR to A Register Immediate	2
	ORAI	Inclusive OR to A Register Immediate	2
	ANAI	And to A Register Immediate	2

Type	*Mnemonic*	*Description*	*Time Cycles*
Input/Output	EXC	External Control Function	1
	CIA	Clear and Input to A Register	2
	CIB	Clear and Input to B Register	2
	CIAB	Clear and Input to A and B Registers	2
	INA	Input to A Register	2
	INB	Input to B Register	2
	INAB	Input to A and B Registers	2
	IME	Input to Memory	3
	OAR	Output A Register	2
	OBR	Output B Registers	2
	OAB	Output OR of A and B Registers	2
	OME	Output from Memory	3
	SEN	Sense Input/Output Lines	2 .25
Register Change	IAR	Increment A Register	1
	DAR	Decrement A Register	1
	IBR	Increment B Register	1
	DBR	Decrement B Register	1
	IXR	Increment X Register	1
	DXR	Decrement X Register	1
	CPA	Complement A Register	1
	CPB	Complement B Register	1
	CPX	Complement X Register	1
	TAB	Transfer AR to B Register	1
	TBA	Transfer BR to A Register	1
	TAX	Transfer AR to X Register	1
	TBX	Transfer BR to X Register	1
	TXA	Transfer XR to A Register	1
	TXB	Transfer XR to B Register	1
	TZA	Transfer Zero to A Register	1
	TZB	Transfer Zero to B Register	1
	TZX	Transfer Zero to X Register	1
	AOFA	Add OF to A Register	1
	AOFB	Add OF to B Register	1
	AOFX	Add OF to X Register	1
	SOFA	Subtract OF from A Register	1
	SOFB	Subtract OF from B Register	1
	SOFX	Subtract OF from X Register	1
	SOF	Set Overflow	1
	ROF	Reset Overflow	1
Logical Shift	LSRA	Logical Shift Right AR k places	1 +.25 k
	LRLA	Logical Rotate Left AR k places	1 +.25 k
	LSRB	Logical Shift Right BR k places	1 +.25 k
	LRLB	Logical Rotate Left BR k places	1 +.25 k
	LLSR	Long Logical Shift Right k places	1 +.25 k
	LLRL	Long Logical Rotate Left k places	1 +.25 k
Arithmetic Shift	ASRA	Arithmetic Shift Right AR k places	1 +.25 k
	ASRB	Arithmetic Shift Right BR k places	1 +.25 k
	ASLA	Arithmetic Shift Left AR k places	1 +.25 k
	ASLB	Arithmetic Shift Left BR k places	1 +.25 k
	LASR	Long Arithmetic Shift Right k places	1 +.25 k
	LASL	Long Arithmetic Shift Left k places	1 +.25 k
Control	HLT	Halt	1
	NOP	No Operation	1

*Denotes optional instruction. Times given are for 16-bit computer. Add 1 cycle for each level of indirect addressing.





MEMORY

The DATA 620/i uses general purpose random access ferrite magnetic core memories. They contain a proprietary thermal compensation technique which preserves the operating margins over the temperature range (5° to 45°C) without adjustment.

The memory communicates with the processor through a memory data bus and an address bus. Additional external (to mainframe) memory modules can be added simply by adding an optional memory adapter to the processor that permits the additional module to be "plugged in." The external memory module includes an adapter for the next memory module. The memory can be expanded to 32,768 words by the addition of 4K memory modules.

Memory cycle time is 1.8 μsec; access time is 750 nanoseconds.

RELIABILITY AND MAINTAINABILITY

DTL & TTL integrated circuits are used throughout the DATA 620/i. These integrated circuits are general purpose digital logic, and are noted for low power consumption, high packing density, high noise rejection, and reliability throughout the operating temperature range of 0°to 45°C. The low power equates to low heat generation and high reliability.

DATA 620/i's are produced under a quality control program designed and practiced to meet MIL-Q-9858A, and to the intent of NPC 200-3. The mean-time-between-failures (MTBF) has been calculated for the basic processors to be over 7,500 hours. The mean-time-to-repair is estimated to be a few minutes.

DATA 620/i's are packaged to simplify maintenance. The integrated circuit board layout is unique using a "Bit Slice" layout. "Bit Slice is a technique whereby all register and gating circuits associated with six bits are packaged on one card.

The structure is designed for easy access. All units of the processor are mounted to be easily removed to make all components and wiring easily accessible. The "big board" concept is used to permit easy trouble shooting.

Failure Detection: The source of faults in solid-state electronic equipment with conservative circuit and timing designs is from external causes. The external causes are power failures, power frequency failures, excessive heat and the failure of electro-mechanical peripheral devices. The DATA 620/i has been designed to prevent each of these fault sources from destroying the integrity of the system computer function.

- *Power Failure*—An optional Power Failure Protect System monitors power line voltage. If voltage is outside safe limits, a power fail interrupt is generated. The interrupt subroutine assures an orderly, safe shutdown. Upon restoration of power, the computer is automatically restarted at a designated memory location, and appropriate software provides an orderly restart.

- *Temperature*—A thermal sensor is embedded in the core memory to continually monitor internal temperature. If the temperature rises above the specified limit (45°C), the sensor produces a thermal alarm signal that is used to light the console alarm indicator and/or generate an interrupt line.

- *Operator Errors*—The control panel is electrically disconnected during "RUN" mode.

- *Memory Protect*—This option permits a top-priority executive, control, alarm, processing, or monitor system to remain resident in memory while other programs are being processed.

These facilities provide the system engineer with the level of assurance needed to tackle the most demanding process control or real-time application where one failure can be extremely costly.

PHYSICAL

Packaging—The DATA 620/i family is packaged to offer the user maximum convenience, positioning, flexibility and space-saving economies. The memory, arithmetic and control unit, and the power supply and control console are three separate packages that, when connected, produce a compact unit that is 10½ inches high, 22 inches deep and 19 inches wide. The compactness and light weight of the DATA 620/i series enables it to be used in facilities such as submarines, aircraft, etc.

Control Panel—The user-oriented design philosophy of the DATA 620/i console utilizes sound human engineering practices. The console has been developed to produce a pleasing image and still be functionally easy to use. Proximity of related functions, minimum reflectivity, and other more subtle features such as length and distance of switches were used in the development of the console. The basic function of the console—to modify and monitor all operational registers—was achieved without a cluttering of switches that tend to confuse. A simple straight-forward instrument is the result.

ENVIRONMENTAL

The DATA 620/i connects to standard commercial single-phase 115 vac power. Power regulation is not required under normal commercial power conditions. Subflooring or conditioned air are not required. The DATA 620/i is equally at home in the shop, field, instrumentation room, classroom, and laboratory.

varian/DATA MACHINES
SENSE
1 2 3
REPEAT
DATA-620/i

PROGRAMMED INPUT/OUTPUT

The basic 620/i Processor is equipped with positive voltage level Party Line I/O bus. The Party Line is a bidirectional common communication channel containing the data and control lines required for system communication. Time-shared between the peripherals, it is designed to prevent conflicts or traffic jams under heavy communication loads. Each transmission contains the routing information as well as the data. It is transmitted as an entity which is not separable by interrupt. Thus, numerous devices can time share the Party Line. The transmission has two phases: The first phase is the route set-up, the second is the data transmission.

The Party Line permits plug-in expansion of all peripheral devices. The Party Line contains line drivers and line receivers to service up to ten peripheral devices. Each peripheral device contains a data buffer and Party Line adapter. Thus, no device can tie-up the Party Line, and modifications to the computer are not required to add peripherals. Each device has a Party Line connector and a Party Line extender connector. The last device on the Party Line has a termination shoe on the extender connector. When another device is added, a Party Line cable is provided between the added and the last device. The termination shoe is moved to the added device.

The Party Line technique solves the troublesome problems usually encountered in time-shared operation and on-site system expansion.

The following types of I/O commands can be executed with the basic machine:

- Single word to/from memory
- Single word to/from A and B registers
- Test External Sense line
- Generated External Control line

The following interface features can be added to the basic Party Line.

DIRECT MEMORY ACCESS AND INTERRUPT LOGIC

This option provides direct memory access (cycle steal capability) from the Party Line I/O bus. With this feature, the user can design special system devices that cause the program to hesitate for 2.7 microseconds, during which time memory is accessed for data, or data is stored in memory. This trap operation bypasses the A, B, X and P registers, thus allowing the program to proceed normally. One interrupt level is provided with the option.

INTERRUPT SYSTEM

The DATA 620/i has a multilevel priority interrupt system with single-instruction execute, group enable/disable, and selective arm/disarm capability. Each interrupt line is assigned a unique memory destination address that is the first of a pair of locations. The system is modular and expandable in groups of eight levels,up to 64 levels.

The interrupt system is automatically scanned every 900 nanoseconds and the interrupt is recognized before the fetch cycle of the next instruction to be executed. If signals exist on one or more interrupt lines, the highest priority is recognized. An interrupt functional response to an external device can be accomplished in as little as two memory cycles.

Each group of eight interrupts can be enabled/disabled, and contains an 8-bit mask register that controls the individual interrupt lines. The program can maintain the hardware order of priority or reorder to meet dynamic queueing.

Acknowledgement of an interrupt by the Central Processor causes the instruction located at the memory destination address of the interrupt to be executed. The instruction can be any of the DATA 620/i instruction set. This technique permits the interrupts to be of the single-execute type, whereby single-instruction responses to external signals can be serviced in one instruction period. If the executed instruction is a jump and mark (JMPM), the interrupt system is automatically inhibited to permit the inhibit to be terminated under program control. The DATA 620/i interrupt system provides the high speed reaction time, expansion capability, priority and queuing versatility required for real-time control.

BUFFER INTERLACE CONTROLLER

Many system devices require computer facilities to transmit I/O data at high rates and volumes and at random periods. Such devices are best serviced with automatic channels which do not require programming or interfere with the processing. The Buffer Interlace Controller (BIC) unit option services such requirements.

The BIC contains two 15-bit registers, the Party Line addressing and control logic, priority logic, and 620/i control logic. The two registers contain the stop address and the current memory address. These registers are set by the program with the start address and the stop address. These addresses define the sequential locations in memory from or to which the data is communicated. Connecting the desired controller to the BIC activates the BIC. The I/O operation is automatic thereafter until the stop address

has been met. Each data word transferred requires less than two memory cycles. Information can be transferred at a rate over 200,000 words per second. The BIC automatically synchronizes the data transmission rate to the device requirement.

The BIC connects to the Party Line and controls the data transmission of the devices with BIC adapters when operating in the "Interlace" mode. Interlace I/O occurs on a memory cycle basis and shares priority with the Control Processor. The BIC will capture the next memory cycle and stall the computer for 2.7 microseconds for each word transmitted. The processing resumes automatically at the completion of the word transferred. Any device connected to the BIC can be operated under control of the BIC or under program control. Up to eight devices can be connected to one Buffer Interlace Controller unit. The current address can be read under program control.

REAL-TIME CLOCK

The DATA 620/i Real-Time Clock is an option that provides a flexible time-orientation system that can be used in a variety of real-time functions, including time-of-day accumulation and as an interval timer.

The Real-Time Clock consists of two interrupts. The first interrupt is a time-base signal that when recognized by the computer, executes an increment memory instruction stored in the interrupt address. The second interrupt occurs when the incremented memory location reaches a count of 40,000.

SENSE LINE

Discrete sense lines are available as options in sets of eight. Each sense line has a unique address. Up to 512 sense lines can be addressed. The sense instruction is a two word conditional jump command. If a signal exists on the sense line addressed, the program jumps to the effective address; otherwise, the program continues at location P+2. The sense lines can be configured in combination with the interrupt lines to permit more than one device to share an interrupt line. All DATA 620/i peripheral equipment include the sense lines required.

EXTERNAL CONTROL LINES

Discrete control lines are available as options in sets of eight. Each control line has a unique address. Up to 512 control lines can be addressed. The external control instruction is a one word instruction that places a pulse on the addressed control line. These are general purpose control lines that can be used to perform external control functions throughout a system.

PARALLEL I/O CHANNELS

The usual system application requires special devices to be connected to the computer. These devices can be interfaced with the computer in many ways. The system designer can implement the interface with his own electronics, purchase and assemble the appropriate logic modules (Micro-VersaLOGIC), or utilize the Varian Data Machine interface controller.

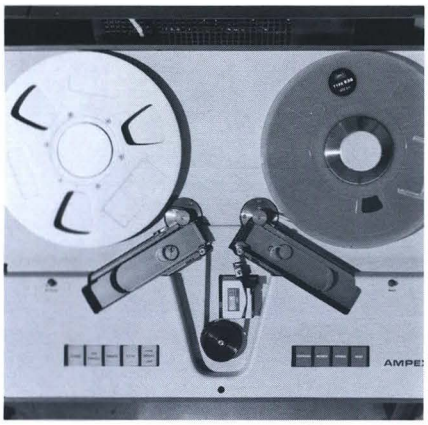
DIGITAL I/O

The digital I/O controller provides the timing, gating and selection logic needed to communicate with the Party Line I/O lines under program control. The controller has:

- Eight Sense Lines
- Eight External Control Lines
- Buffered Input Channel—Provides an 18-bit register to receive pulsed inputs for subsequent input to the Party Line.
- Buffered Output Channel—Provides 18 stored logic levels (flip-flops) for level output from the Party Line.

The controller is 18-bit parallel (on the 16-bit computer, 2 bits are not used) and greatly alleviates the interface problem.

PERIPHERAL EQUIPMENT

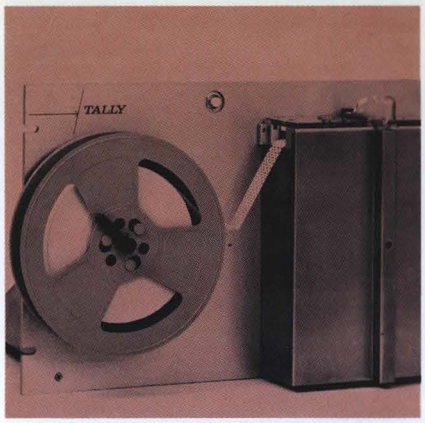


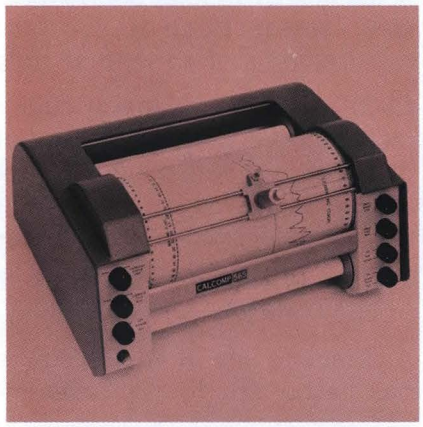
A full line of compatible peripheral equipment is available for the DATA 620/i series. Each device has been selected to meet the functional requirements of a real-time data system.

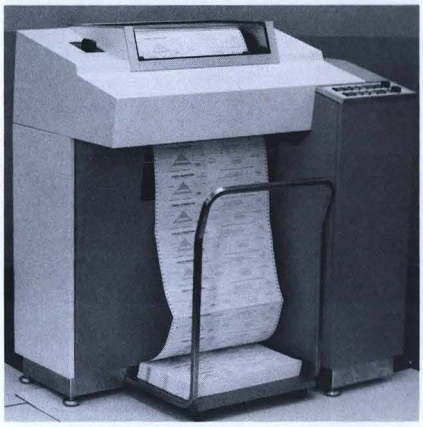
Each piece of peripheral equipment is provided with a controller that includes a Party Line adapter, buffering and control lines. The line printer, disc storage, and magnetic tapes include word assembly/disassembly registers. The magnetic tape control units contain double buffers to permit multiple simultaneous high-performance magnetic tape operation.

The peripherals will operate with the Party Line under program control, or automatically with an (optional) Buffer Interlace Controller.

A complete line of analog conversion equipment is offered on a custom basis according to the requirement.







DATA 620/i SERIES PERIPHERAL EQUIPMENT

MAGNETIC TAPE SYSTEMS

Tape Controllers—Master controller for up to four tape transports. Will control 7 or 9 track transport and includes assembly/disassembly register.

Tape Transports—Speeds of 45, 75, and 120 ips. Densities of 200, 556, and 800 bpi. Seven and nine track industry compatible units.

AUXILIARY STORAGE

Fixed head rotating memory systems with capacities from 32K words to 262K words. Access time is 17 milliseconds. Transfer rates from 30 to 120 KC.

READERS AND PUNCHES

Card Reader—1000 cpm
Paper Tape Reader—300 cps
Paper Tape Punch—60 and 120 cps

DIGITAL INPUT/OUTPUT

KEYBOARD

ASR 33 Teletypewriter
ASR 35 Teletypewriter
KSR 35 Teletypewriter

GRAPHIC DEVICES

Oscilloscope Displays
High Speed Printers—300 and 600 LPM
Electrostatic Plotters
Digital Plotters—300 steps per sec.

MODEM INTERFACES

103, 201, and 301 types

SYSTEM SOFTWARE

A comprehensive package of operational programs are available with the DATA 620/i. These include a symbolic assembler, FORTRAN compiler, library of mathematical subroutines, debugging package, and a modular maintenance diagnostic package. The complete software package operates in the basic 8,192 words of core memory. In addition, Varian Data Machines has developed many real-time programs for a specific customer application. The more important portions of the Varian Data Machine software library are described below.

SYMBOLIC ASSEMBLER

The DATA 620/i Assembler System (DAS) is a two-

pass assembler that assists in program preparation by allowing instructions, addresses, etc., to be specified in a straight-forward and meaningful manner. DAS recognizes over 20 pseudo-operations that aid the user in coding and debugging problems. Although DAS operates in a minimum system consisting of 4,096 words of core memory, paper tape reader, paper tape punch and typewriter, provisions have been made to utilize additional memory and peripheral equipment available to the system. Extensive syntax checking is performed during both passes of the assembler.

FORTRAN

DATA 620/i FORTRAN conforms with the proposed American standards for Basic FORTRAN as published by the American Standards Association. The 620/i FORTRAN, a one-pass compiler, can operate in a 8,192 word computer equipped with only a model ASR 33 Teletypewriter. Naturally, if higher performance peripherals are on the system, 620/i FORTRAN utilizes them to produce faster compilation.

AID

AID is a collection of useful diagnostic and utility routines for the DATA 620/i computer. With this package, the programmer can call upon a wide variety of functions to aid him in debugging and running his programs. AID includes routines to correct memory, establish breakpoints, search memory, print memory, etc.

Also included in the AID package is a comprehensive binary paper tape handler that is particularly useful in preserving programs modified on the computer. This routine uses a standard address, data, and checksum format that is used by the DAS assembler.

DIAGNOSTIC PROGRAM PACKAGE

The DATA 620/i Diagnostic Program Package is designed to check instructions, memory, and input/output devices, and to isolate errors. It can be used in either the preventative or the corrective mode of operation. In the preventative mode, the complete system is checked for operational readiness. If a malfunction exists, in most cases, the preventative will isolate the error. The corrective mode of operation is used when a malfunction is known to exist and the preventive mode does not decisively show the trouble. Proper application of these diagnostic routines can cut the mean-time-to-repair to minutes. This modular package can be easily expanded to accommodate any special system hardware tests.

SUBROUTINE LIBRARY

This comprehensive library includes the most commonly used subroutines needed in a systems environment. The library includes routines for logarithmic, exponential and trigonometric functions, for fixed and floating-point arithmetic, and for operating standard peripheral equipment. Conventions and instructions are provided so the user can add application programs to the library and be called by DAS, FORTRAN and AID.

USER SERVICES

The purchase of a DATA 620/i includes support services designed to provide the user with start-up and sustaining service.

DOCUMENTATION

The documentation is comprehensive and clear, and contains the information required for the user to fully understand, program, operate and maintain the system. Interface and installation manuals are provided to the user prior to installation for system integration preparation. The program and service manuals are provided in advance of the user training attendance. The software manuals contain a special section covering software modularity and expansion techniques.

PROGRAMMING TRAINING *

Programming training courses are provided on a scheduled basis at Varian Data Machine facilities. The one week course covers instruction for programming in machine language, an introduction to the DATA 620/i software, and machine operation. The course includes time at the console. Supplies required for the course are provided at no charge to the attendees. On-site courses are available on a contract basis.

MAINTENANCE TRAINING *

A two-week-at-the-factory maintenance course is provided on a scheduled basis. The instruction covers machine organization, operation, logic, design, timing, preventive maintenance, trouble-shooting, and repair. Extended training covering special systems hardware is available on an individual customer basis. The course is designed for personnel with existing digital logic design knowledge.

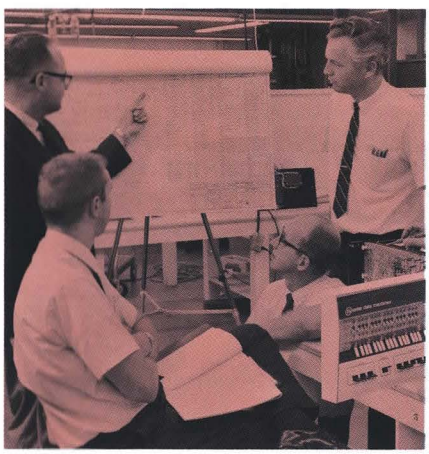
USER ORGANIZATION

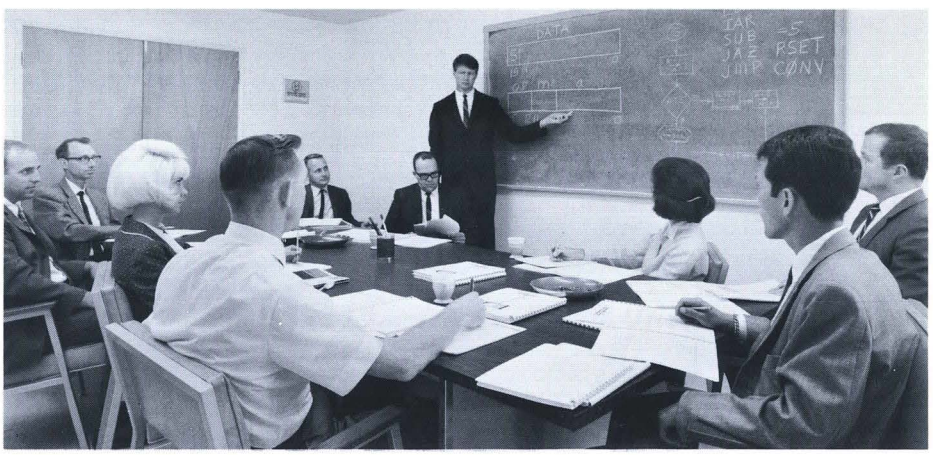
Varian Data Machine Customer Services (CS) provide continuing coordination, program exchange and library maintenance for DATA 620 and DATA 620/i users. Users are notified of new additions to the library, application data, program and hardware modifications and new equipment. CS maintains up-to-date master prints on each system controlled. An inventory of programming forms, paper tapes and spare parts is maintained for expedited or emergency service. Statistical data on field operating experience based on user-submitted reports is maintained and available to users. On-call and on-site maintenance services are available on a contract basis.

APPLICATION PROGRAMMING

Varian Data Machines' technical staff includes senior application programming specialists well-qualified to assist the user in the preparation of application programs. This professional group can assume full responsibility on a contract basis for the preparation of a total solution, including hardware and application programs.

**Available at nominal cost.*




DATA
IAR -5
SUB
JAZ RSET
JMP CØNV

DATA 620/i SPECIFICATIONS

TYPE	A system computer, general purpose digital, designed for on-line data system requirements, magnetic core memory, binary, parallel, single-address, with bus organization and micro-control.
MEMORY	Magnetic Core, 16 bits (18 bits optional), 1.8 microseconds full cycle, 750 nanoseconds access time, 4096 words minimum expandable to 32,768 words.
ARITHMETIC	Parallel, binary, fixed point, 2's complement.
WORD LENGTH	16 bits standard; 18 bits optional.

SPEED (FETCH & EXECUTE)

Add or Subtract	3.6 microseconds
Multiply (optional)	18.0 microseconds, 16-bit 19.8 microseconds, 18-bit
Divide (optional)	18.0 to 25 microseconds, 16-bit 19.8 to 28.8 microseconds, 18-bit
Register change class	1.8 microseconds
Input/Output—from A or B	3.6 microseconds
from memory	5.4 microseconds

OPERATION REGISTERS

A Register—accumulator, input/output, 16/18 bits.
B Register—double length accumulator, input/output, index register, 16/18 bits.
X Register—index register, 16/18 bits.
P Register—program counter, 16/18 bits.

BUFFER REGISTERS

R Register—operand register, 16/18 bits.

U Register—instruction register, 16 bits.

S Register—shift register, 5 bits, operates with the U Register for executing shift instructions.

L Register—memory address register

W Register—memory word register, 16/18 bits

CONTROL

ADDRESSING MODES
- Direct addressing to 2,048 words
- Relative to P Register 512 words
- Index with X Register, hardware, does not add to execution time
- Index with B Register, hardware, does not add to execution time
- Multi-level indirect addressing
- Immediate
- Extended addressing (optional)

INSTRUCTION TYPES
- Single word
- Double word
- Generic
- Micro-command

INSTRUCTIONS: Over 100 standard commands, listed below, plus more than 128 macro-instructions:

3	Load
3	Store
5	Arithmetic (2 optional)
3	Logical
10	Jump
10	Jump and Mark
10	Execute
14	Immediate (2 optional)
13	Input/Output
26	Register Change
6	Logical Shift
6	Arithmetic Shift
2	Control
14	Extended addressing (optional)
	Over 128 micro-instructions

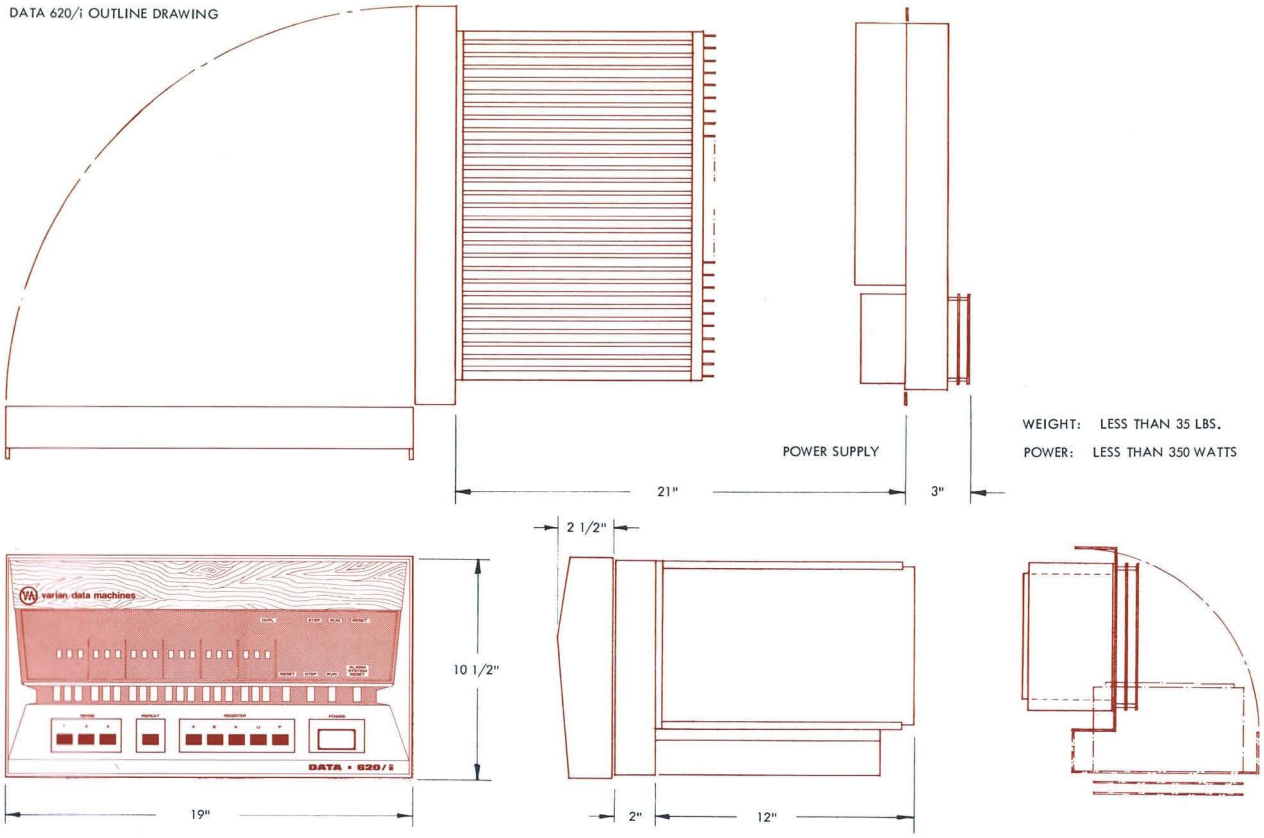
MICRO-EXEC (Optional)

Facility and hardware to construct a hardware program external to the DATA 620/i. Eliminates stored program memory accessing by use of hardware program.

CONSOLE

Display and data entry switches for all operational registers, 3 sense switches, instruction repeat, single step; run; power on/off.

DATA 620/i OUTLINE DRAWING



INPUT/OUTPUT

Processor Input/Output Options
- Programmed Data Transfer
  - Single word to/from memory
  - Single word to/from A and B Registers
  - External control lines
  - External sense lines
- Automatic Data Transfer
  - Direct memory access facility transfer with rates over 200,000 words per second.
  - Priority Interrupts
    Group enable/disable, individually arm/disarm, single instruction interrupt capability.
- Real-Time Clock
  - Adjustable time base: May be programmed as multiple internal timers.
- Power Failure detect/restart
  - Interrupts on power failure and automatically restarts on power recovery.

PHYSICAL

DIMENSIONS
Mainframe—10-1/2 inches high, 19 inches wide 14 inches deep

WEIGHT
Mainframe—35 pounds

POWER
3 amps (340 watts). 115±10v, 60 ± 2hz. Power supplies are regulated. Additional regulation is not required under normal commercial power sources.
Conversion for 50hz and other voltages available at added cost.

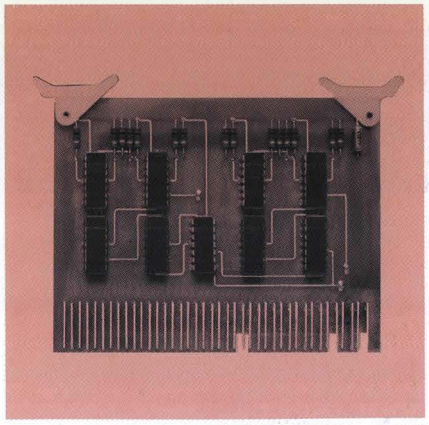
EXPANSION
Main processor contains provisions and space for all internal options.

INSTALLATION
Mounts in standard 19-inch cabinet, no air conditioning, sub-flooring or special wiring and site preparation required.

ENVIRONMENTS
5°C to 45°C; 0 to 90% relative humidity

MAINFRAME LOGIC AND SIGNALS

Integrated circuit, 8.8 mhz clock, logic levels 0v false, + 5 v true.

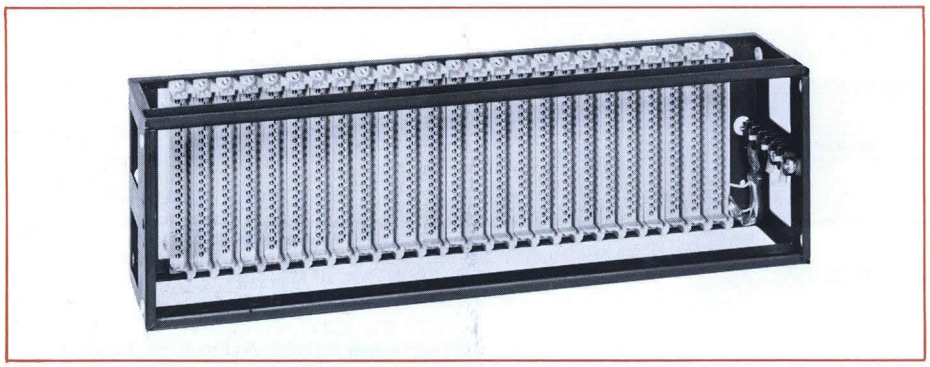


FULLY COMPATIBLE SYSTEM COMPONENTS

To increase your total system capability, Varian Data Machines offers a complete line of high-performance integrated circuit logic modules, small high-speed core memories and large mainframe memories for I/O equipment or additional system requirements. All have been field-proven with the DATA 620/i System, and are fully compatible with its power supply, voltage levels and signal requirements.

MicroVersaLOGIC INTEGRATED CIRCUIT LOGIC MODULES

MicroVersaLOGIC 5 m.c. general purpose IC modules—with NAND, NOR logic, and wired OR capacity at the collector—5v logic levels—and excellent noise rejection over 1v. Over 25 module types, including universal flip-flops, delay multivibrators, clock drivers, 2-, 3- and 4-input expandable gates, and PNP to NPN interface modules. Compatible mounting hardware—including card files and card drawers—is also available.



VersaSTORE II CORE MEMORIES

New high-speed core memory systems—with integrated circuits and all-silicon components for highest reliability—that operate asynchronously at 1.6 microseconds, with 650 nanosecond access time. VersaSTORE II memories are available in increments up to 4,096 words of 36 bits, require only 5¼″ of rack space, and can also be provided as 8k word memories of up to 18 bits.

Options include party line, built-in self-test, and a variety of timing and control flags.

VersaSTORE MAINFRAME MEMORIES

High-reliability VersaSTORE mainframe memories in sizes up to 65k words in 4k increments, with word lengths to 36 or 72 bits. Features include PNP to NPN interface—flexible input levels of 3v to 12v—continuous lamp display of address and data registers—servoed current drive —2 μsec operation—integrated circuit design—and DATAGUARD protection system.

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