Production Test Strategy for the HP E5200A Broadband Service Analyzer

Boundary scan and built-in self-test are supplemented by conventional testing techniques. Eight discrete levels of testing were implemented.

by Cary J. Wright

The HP E5200A broadband service analyzer is a highly complex digital system packed into a field-portable case. During its design, it was essential to achieve the highest densities possible by using some of the latest technologies.

To achieve the functionality required, the main processor printed circuit assembly for the product had to be extremely densely populated. This printed circuit assembly contains over 1000 components, including 29 XFP parts, 30 FP parts, and almost 8700 solder joints (see "***HP E5200A Broadband Service Analyzer Surface Mount Assembly***" for further details). Because of the sheer density of the printed circuit assembly, testing by conventional bed-of-nails in-circuit techniques alone was not feasible.

In addition, normal defect rates specified by surface mount placement vendors were in the order of 200 ppm. From this data, each printed circuit assembly was predicted to have at least one defective solder joint after the placement process. Because of the high cost of this printed circuit assembly, it was very important to be able to accurately and quickly identify defects with high success rates. The target yield for the assembly and commissioning process was set to 100%.

Overall Test Strategy

To overcome the challenges presented, it was necessary to implement a comprehensive test strategy that included boundary scan and built-in self-test, supplemented by conventional testing techniques.

With this complex printed circuit assembly it was decided that a multitiered testing strategy would be used. Such a strategy would increase yield by identifying faults early and by verifying functionality in small discrete stages. Another advantage was that the tests could be reused for other purposes such as service, calibration, or confidence tests.

Fig. 1 shows the production test strategy that was implemented for the service analyzer project. Eight discrete levels of testing were implemented. Each level verifies basic functionality before proceeding to the next stage of assembly or testing. The chance of catastrophic and difficult-to-diagnose failures is minimized.

Boundary Scan Technology

Boundary scan technology forms the key to the production test strategy. Boundary scan is often referred to as JTAG (Joint Test Action Group) and is defined by the IEEE 1149.1 standard. Fig. 2 shows a typical IEEE 1149.1-compliant device.

Boundary scan functions of a device are stimulated via the TDI (test data input), TCK (test clock), TMS (test mode select), and TRST (test mode reset) pins. Responses are received from TDO (test data output). For a printed circuit assembly or system, TDI and TDO pins of each device or submodule are connected in a chain, with the TDO of one device or submodule connected to the TDI of another. The TCK, TMS, and optional TRST pins of devices are connected in parallel (see Fig. 3).

The TAP (test access port) controller is a simple state machine with 16 states. Transitions between states are controlled by TMS and TCK. The TAP controller states determine how data is shifted into or out of the various device registers. Boundary, instruction, and bypass registers are the most important registers of a boundary scan device. The instruction register allows control of the various test modes. Boundary registers capture and control device pin states. The bypass register provides the ability to bypass a device in the chain.

With these three registers and knowledge of the printed circuit board netlist, it is possible to generate and analyze long strings of serial data (test vectors) to detect pins and traces that are shorted or open. Special tests can also be devised for testing nonscannable devices that are surrounded by scannable devices, (i.e., cluster testing). U2 in Fig. 3 is an example of such a device. In addition, the internal logic of a device can also be exercised.

The loaded HP E5200A printed circuit assemblies are first tested using the HP 3070 in-circuit tester. The HP 3070 allows combined testing (boundary scan and test points) for the greatest coverage and resolution. Tests are performed extremely quickly, avoiding component damage.

Test vectors for the service analyzer were also generated using ASSET^{TM} scan software. These vectors are applied using both a PC with an ASSET hardware interface and an embedded scan engine. Greater test coverage is achieved when the PC

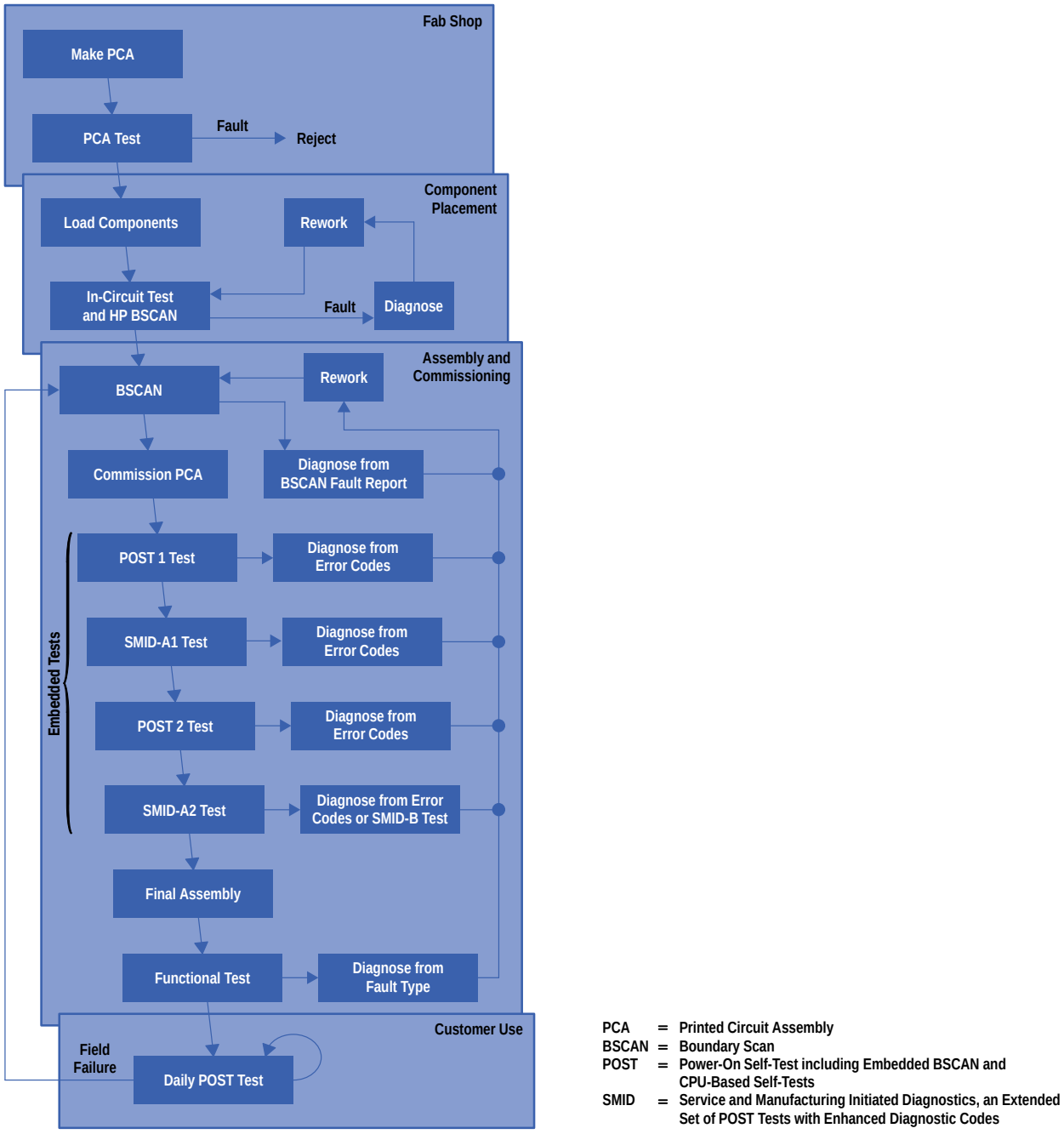

Fig. 1. *Production test strategy for the HP E5200A broadband service analyzer.*

and ASSET hardware interface are used. The embedded scan engine provides less coverage, but is useful as a power-up self-test for the user-initiated or service-initiated diagnostic. Coverage and speed of ASSET tests are not as great as the HP 3070, but setup costs and portability are much more attractive for a service and diagnostic environment.

Boundary Scan Limitations

Boundary scan cannot be used for testing all circuits. Analog devices, nonscannable parts, and passive parts require the use of conventional testing techniques. At-speed testing cannot be performed because of boundary scan's serial architecture. Boundary scan is essentially a static (dc) test. Component costs are increased, although this is offset by savings in real estate, increased production yield, and reduced repair diagnosis time.

Issues that arose during the implementation of boundary scan included difficulties achieving clean TCK waveforms at all nodes, incorrectly supplied component description files, and failures caused by scan chain data corruption.

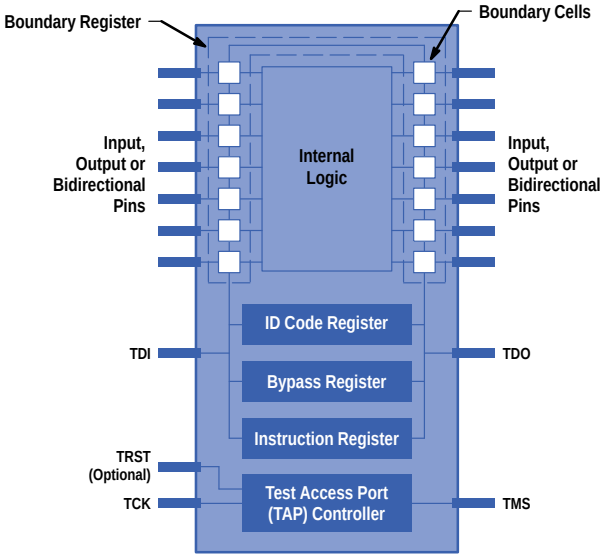

Fig. 2. *Typical IEEE 1149.1-compliant device.*

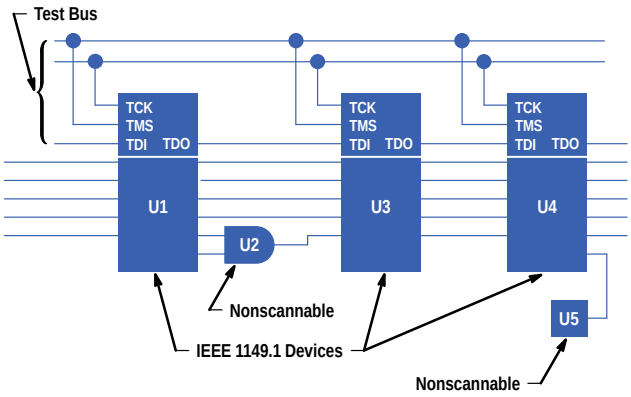

Fig. 3. *Simple boundary scan chain.*

Boundary Scan Benefits

Many benefits were gained by adopting boundary scan for the service analyzer project. The use of boundary scan helped to achieve size requirements for the product, and was invaluable for getting early prototypes running. Embedded boundary scan now provides the user with high confidence in the product, and allows for quick diagnosis at repair centers without expensive tools and fixtures. Production repair and diagnosis time are down and yield is improved. Overall, boundary scan has proved to be a flexible and powerful tool.

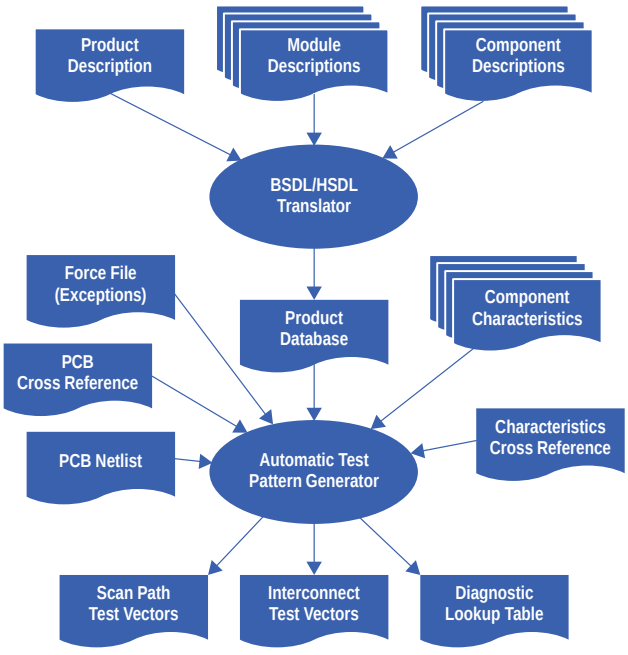

Fig. 4. *Test vector generation.*

Acknowledgments

Design for testability is often an area that suffers neglect during projects that have severe time and resource constraints. It is important to acknowledge the efforts of the service analyzer product design team, which despite these constraints implemented a valuable test strategy.

Bibliography

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