PDP
1
HANDBOOK

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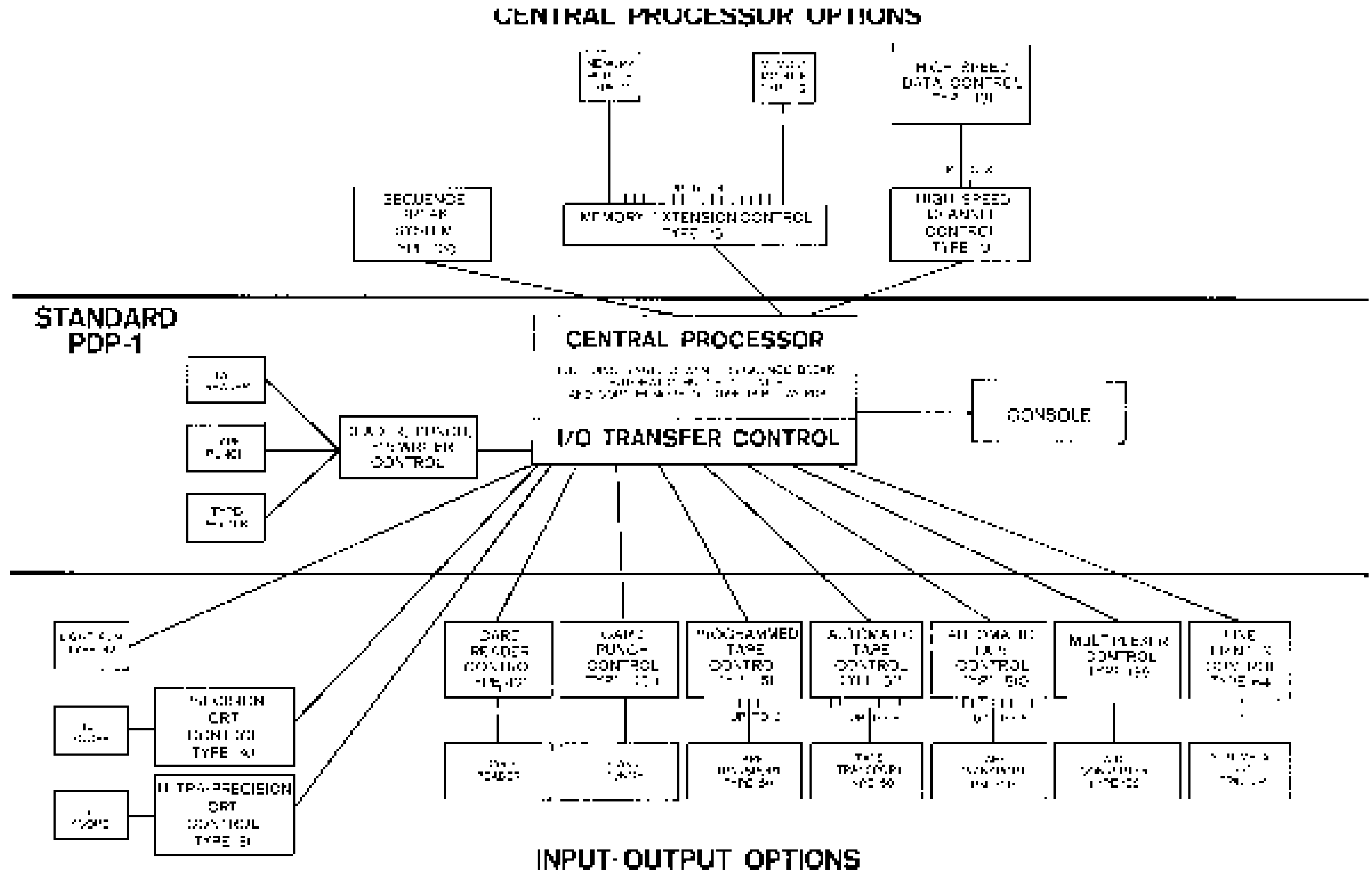
PROGRAMMED DATA PROCESSOR-1 HANDBOOK

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

Programmed Data Processor 1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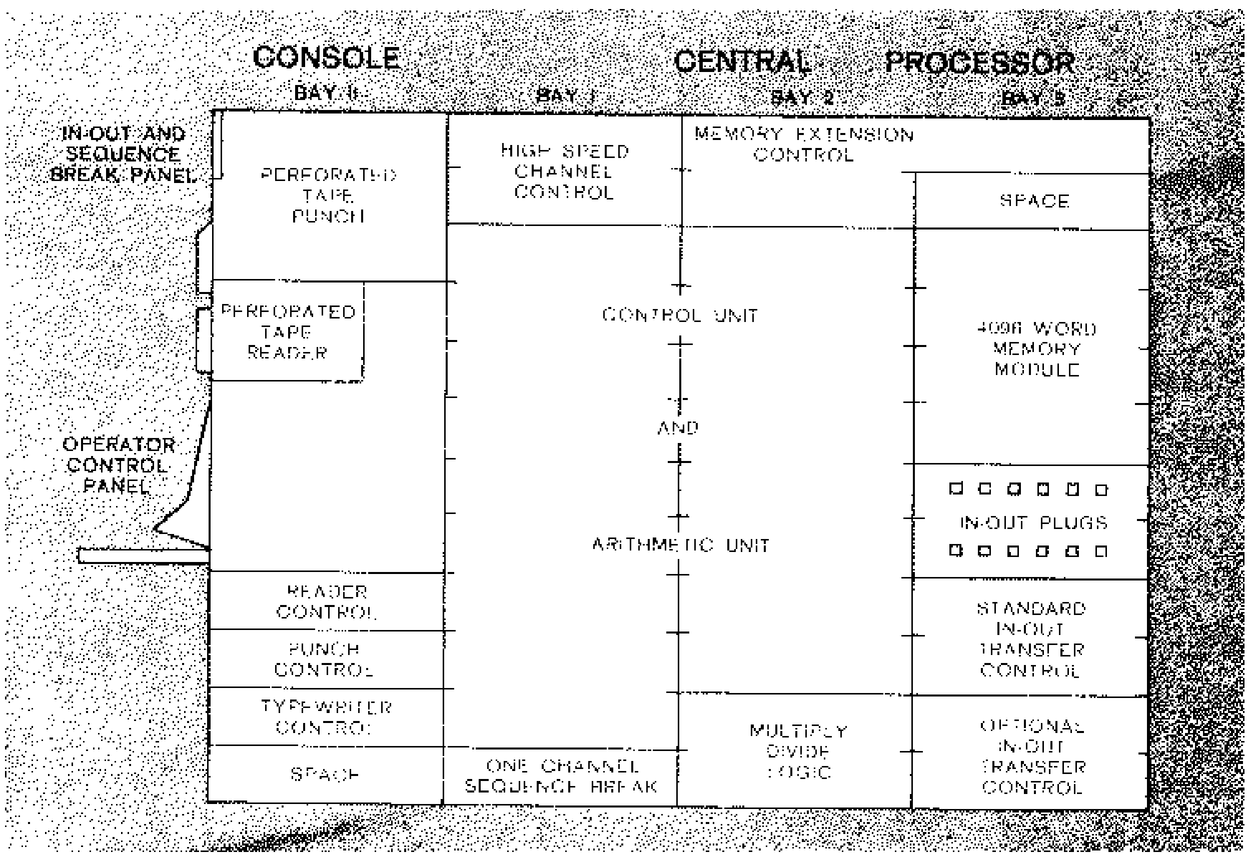
INTRODUCTION

The Programmed Data Processor (PDP-1) is a high speed, solid state digital computer designed to operate with many types of input-output devices with no internal machine changes. It is a single address, single instruction, stored program computer with powerful program features. Five-megacycle circuits, a magnetic core memory and fully parallel processing make possible a computation rate of 100,000 additions per second. The PDP-1 is unusually versatile. It is easy to install, operate and maintain. Conventional 110-volt power is used, neither air conditioning nor floor reinforcement is necessary, and preventive maintenance is provided for by built-in marginal checking circuits.

PDP-1 circuits are based on the designs of DEC's highly successful and reliable System Modules. Flip-flops and most switches use saturating transistors. Primary active elements are Micro-Alloy-Diffused transistors.

The entire computer occupies only 17 square feet of floor space. It consists of four equipment frames, one of which is used as the operating station.



Central Processor Logic Layout, Side View

CENTRAL PROCESSOR

The Central Processor contains the control, arithmetic and memory addressing elements, and the memory buffer register. The word length is 18 binary digits. Instructions are performed in multiples of the memory cycle time of five microseconds. Add, subtract, deposit, and load, for example, are two-cycle instructions requiring 10 microseconds. Multiplication requires and average of 20 microseconds. Program features include: single address instructions, multiple step indirect addressing and logical arithmetic commands. Console features include: flip-flop indicators grouped for convenient octal reading, six program flags for automatic setting and computer sensing, and six sense switches for manual setting and computer sensing.

MEMORY SYSTEM

The coincident-current, magnetic core memory of a standard PDP-1 holds 4096 words of 18 bits each. Memory capacity may be readily expanded, in increments of 4096 words, to a maximum of 65,536 words. The read-rewrite time of the memory is five microseconds, the basic computer rate. Driving currents are automatically adjusted to compensate for temperature variations between 50 and 110 degrees Fahrenheit. The core memory storage may be supplemented by up to 24 magnetic tape transports.

INPUT-OUTPUT

PDP-1 is designed to operate a variety of buffered input-output devices. Standard equipment consistes of a perforated tape reader with a read speed of 400 lines per second, and alphanuermic typewriter for on-line operation in both input and output, and a perforated tape punch (alphanumeric or binary) with a speed of 63 lines per second. A variety of optional equipment is available, including the following:

- Precision CRT Display Type 30
- Ultra-Precision CRT Display Type 31
- Symbol Generator Type 33
- Light Pen Type 32
- Oscilloscope Display Type 34
- Card Punch Control Type 40-1
- Card Reader and Control Type 421
- Magnetic Tape Transport Type 50
- Programmed Magnetic Tape Control Type 51
- Automatic Magnetic Tape Control Type 52
- Automatic Magnetic Tape Control Type 510
- Parallel Drum Type 23
- Automatic Line Printer and Control Type 64
- 18-bit Real Time Clock
- 18-bit Output Relay Buffer Type 140
- Multiplexed A-D Converter Type 138/139

All in-out operations are performed through the In-Out Register or through the high speed input-output channels.

The PDP-1 is also available with the optional Sequence Break System. This is a multi-channel priority interrupt feature which permits concurrent operation of several in-out devices. A one-channel Sequence Break System is included in the standard PDP-1. Optional Sequence Break Systems consist of 16, 32, 64, 128, and 256 channels.

PROGRAMMING PDP-1

The Central Processor of PDP-1 contains the Control Element, the Memory Buffer Register, the Arithmetic Element, and the Memory Addressing Element. The Control Element governs the complete operation of the computer including memory timing, instruction performance and the initiation of input-output commands. The Arithmetic Element, which includes the Accumulator and the In-Out Register, performs the arithmetic operations. The Memory Addressing Element, which includes the Program Counter and the Memory Address Register, performs address bookkeeping and modification.

The powerful programming features of PDP-1 include:

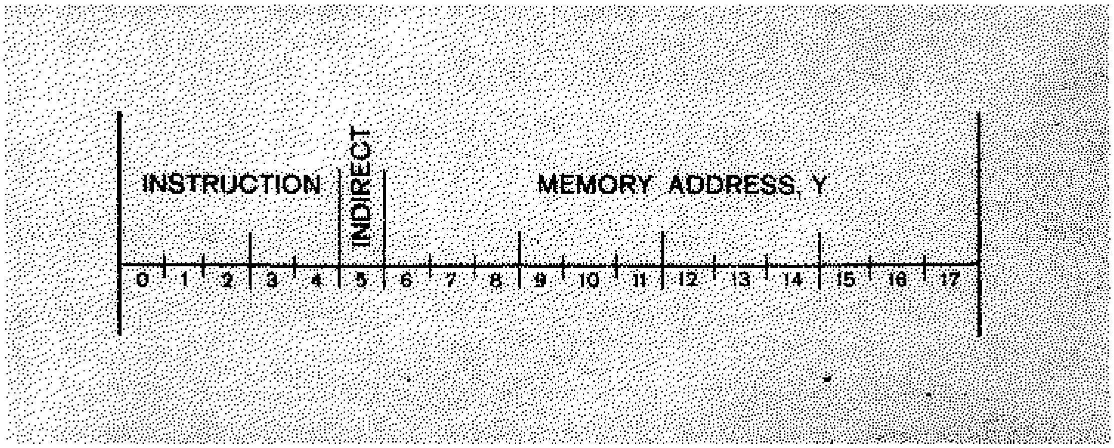
- Multiple step indirect addressing
- Boolean operations
- Twelve variations of arithmetic and logical shifting, operating on 18 or 36 bits
- Fifteen basic conditional skip instructions (expandable by combining to form the inclusive OR of the separate conditions)
- Three different subroutine calling instructions
- Micro-coded operate instructions
- Index and Index-Conditional instructions
- Execute instruction
- Load-immediate instructions
- Built-in multiply and divide instructions

Six independent flip-flops, called program flags, are available for use as program switches or special in-out synchronizers. Multiply and divide operate in about 20 and 35 microseconds respectively.

NUMBER SYSTEM

The PDP-1 is a “fixed point” machine using binary arithmetic. Negative numbers are represented as the one’s complement of the positive numbers. Bit 0 is the sign bit which is ZERO for positive numbers. Bits 1 to 17 are magnitude bits, with Bit 1 being the most significant and Bit 17 being the least significant. To avoid a frequent point of confusion in one’s complement arithmetic, the representation of -0 is automatically changed to +0 in certain arithmetic operations.

The conversion of decimal numbers into the binary system for use by the machine is performed by subroutines. Similarly the output conversion of binary numbers into decimals is done by subroutine. Operations for floating point numbers are handled by interpretive programming.



PDP-1 Instruction Format

INSTRUCTION FORMAT

The Bits 0 through 4 define the instruction code; thus there are 32 possible instruction codes, not all of which are used. The instructions may be divided into two classes:

Memory Reference instructions
Augmented instructions

In the memory reference instructions, Bit 5 is the indirect address bit. The instruction memory address, Y, is in Bits 6 through 17. These digits are sufficient to address 4096 words of memory.

The augmented instructions use Bits 5 through 17 to specify variations of the basic instruction. For example, in the shift instruction, Bit 5 specifies direction of shift, Bit 6 specifies the character of the shift (arithmetic or logical), Bits 7 and 8 enable the registers (01 = AC, 10 = IO, and 11 = both) and Bits 9 through 17 specify the number of steps.

INDIRECT ADDRESSING

A memory reference instruction which is to use an indirect address will have a ONE in Bit 5 of the instruction word. The original address, Y, of the instruction will not be used to locate the operand, jump location, etc., of the instruction, as in the normal case. Instead it is used to locate a memory register whose contents in Bits 6 through 17 will be used as the address of the original instruction. Thus, Y is not the location of the operand but the location of the location of the operand. If the memory register containing the indirect address also has a ONE in bit 5, the indirect addressing procedure is repeated and a third address is located. There is no limit to the number of times this process can be repeated.