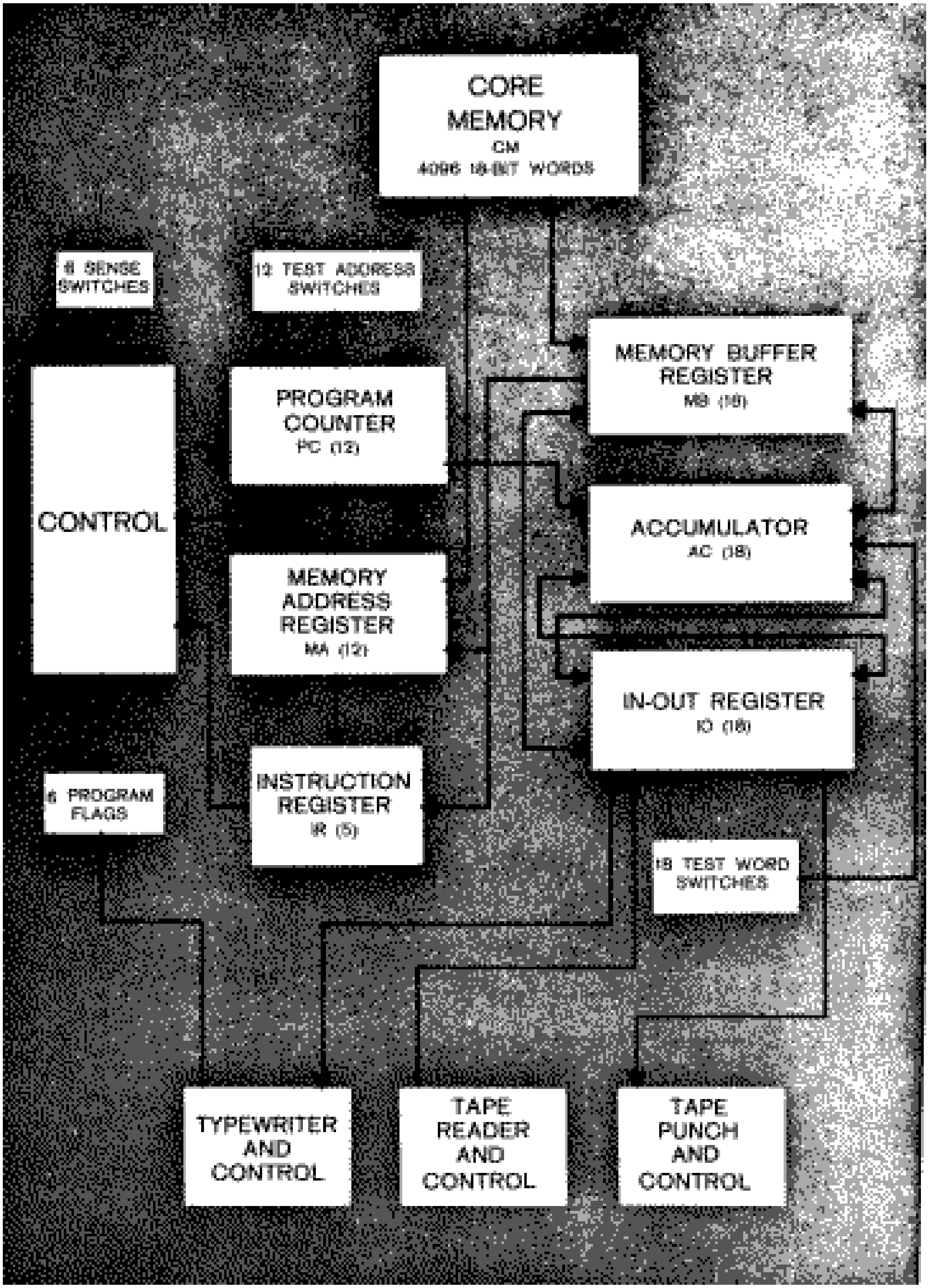


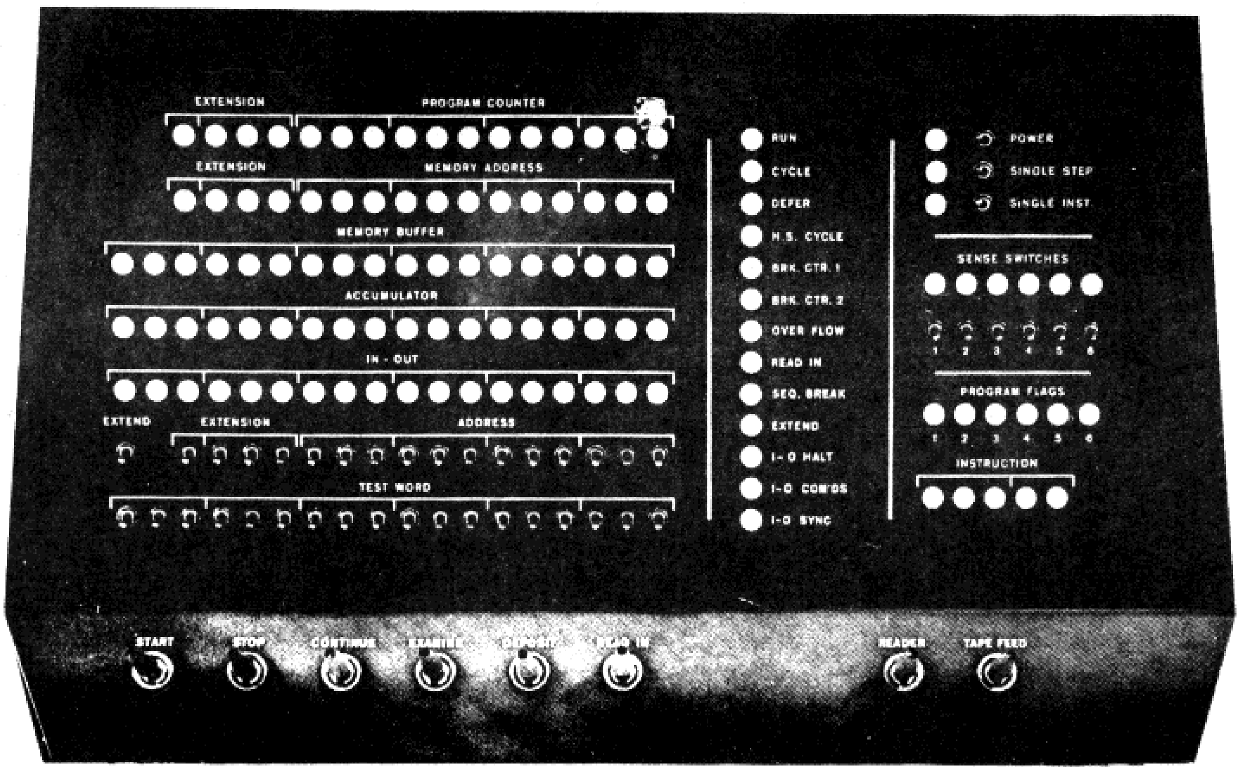
PDP-1 Logic Organization

OPERATING SPEEDS

Operating times of PDP-1 instructions are multiples of the memory cycle of 5 microseconds. Two-cycle instructions refer twice to memory and thus require 10 microseconds for completion. Examples of this are add, subtract, deposit, load, etc. The jump, augmented and combined augmented instructions need only one call on memory and are performed in 5 microseconds.

In-Out Transfer instructions that do not include the optional wait function require 5 microseconds. If the in-out device requires a wait time for completion, the operating time depends upon the device being used.

Each step of indirect addressing requires an additional 5 microseconds.

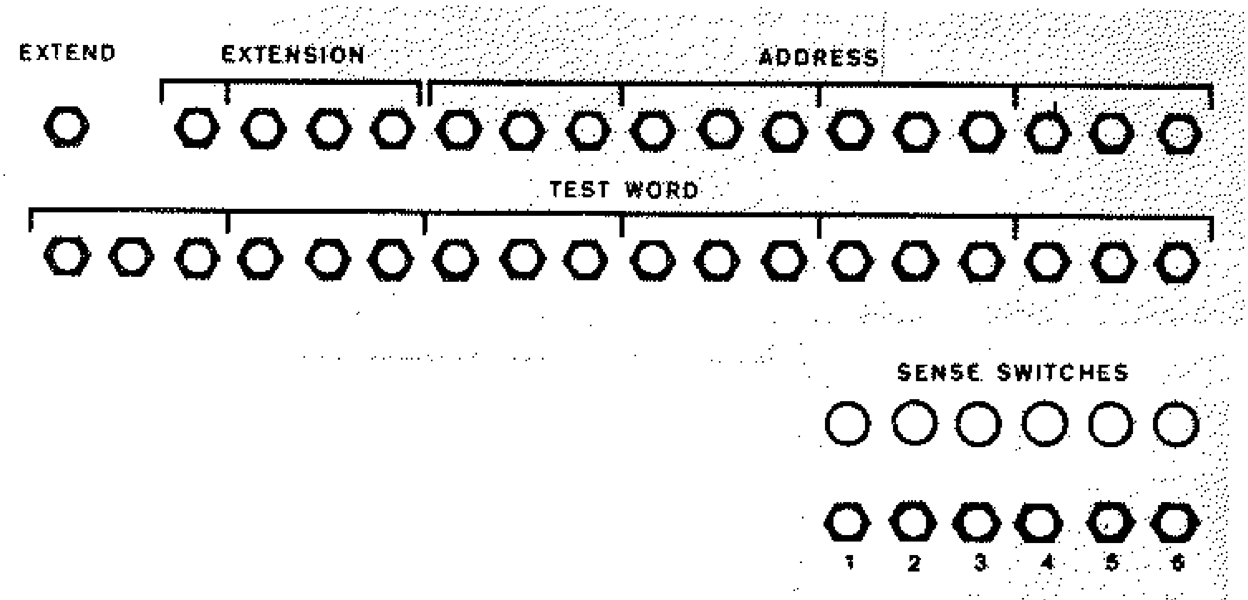


PDP-1 Control Panel

MANUAL CONTROLS

The Console of PDP-1 has controls and indicators for the use of the operator. All active registers have indicator lights on the Console. These indicators are primarily for use when the machine has stopped or when the machine is being operated one step at a time.

Three banks of toggle switches are available on the Console. These are the Address Switches (16 bits), the Test Word Switches (18 bits), and the Sense Switches (6 bits). The first two are primarily used in conjunction with the operating push buttons. The Sense Switches are present for manual intervention. The use of these switches is determnined by the program.



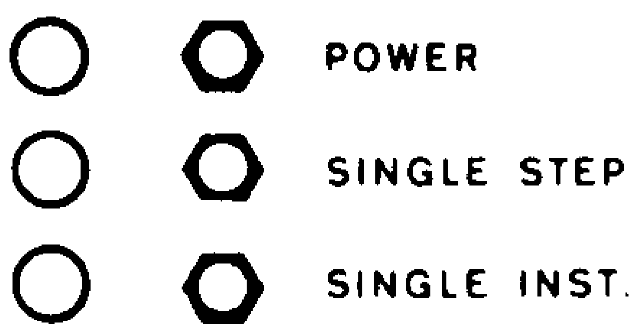
CONSOLE LEVER SWITCHES

START	The first instruction executed comes from the memory location indicated by the Address and Extension Switches. If Start is pushed up, the computer enters the Sequence Break Mode before starting; if pushed down, the computer leaves the Sequence Break Mode. In either case, the overflow flip-flop is cleared and the Extend Switch condition is read into the Extend flip-flop.
STOP	The computer will come to a halt at the completion of the current memory cycle.
CONTINUE	The computer will resume operation starting from the point where it was stopped.
EXAMINE	The contents of the memory register indicated by the Address and Extension Switches will be displayed in the Accumulator and Memory Buffer lights.
DEPOSIT	The word in the Test Word Switches will be put in the memory location indicated by the Address and Extension Switches.

READ IN	The Perforated Tape Reader will start operating in the Read-In mode.
READER	When pushed up, turns Perforated Tape Reader motor on; when pushed down, turns it off.
TAPE FEED	When switch is pressed, Tape Punch feeds blank tape.

CONSOLE TOGGLE SWITCHES

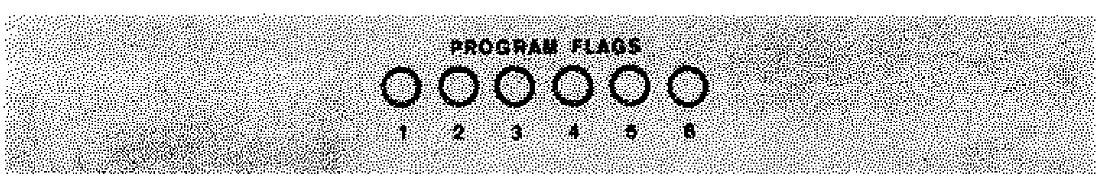
EXTEND	When Start or Read In is pressed, the state of this switch is read into the Extend flip-flop.
EXTENSION	Specify which memory module will be used when Start, Examine, Deposit, or Read In are pressed.
ADDRESS	Specify memory location for Start, Examine, and Deposit.
TEST WORD	Specifies the word to be put in memory when Deposit is pressed. Can be read into the AC under program control.
SENSE SWITCHES	Convenient switches whose conditions may be individually tested by the program.



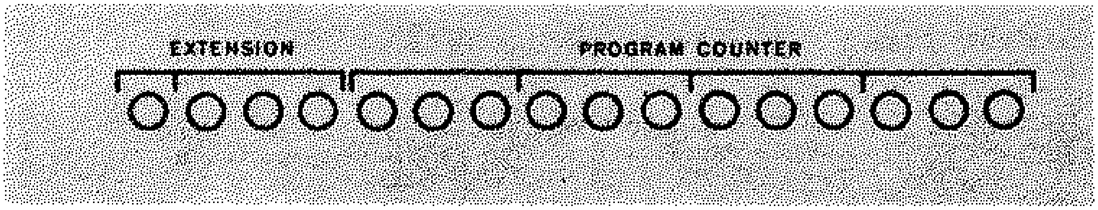
CONSOLE INDICATOR LIGHTS

O RUN	RUN	On while the computer is executing instructions.
O CYCLE	CYCLE	On after the completion of one or more instruction cycles with oneor more to follow.
O DEFER	DEFER	On immediately prior to and during the execution of any deferred cycle.

O H. S. CYCLE	HIGH SPEED CYCLE	On while the computer is executing a High Speed Channel Data Transfer.
O BRK. CTR. 1	BREAK COUNTER 1	On while the computer is executing cycle 1 (deposit Accumulator) and cycle 3 (deposit Input-Output Register) of a sequence break.
O BRK. CTR. 2	BREAK COUNTER 2	On while the computer is executing cycle 2 (deposit Program Counter) and cycle 3 of a sequence break.
O OVER FLOW	OVERFLOW	On if overflow has occurred. (Can only be turned off or cleared by side} executing the Skip on Zero Overflow instruction or pressing Start.)
O READ IN	READ IN	On while the computer is reading punched tape in the Read-In mode.
O SEQ. BREAK	SEQUENCE BREAK	On while the computer is in the Sequence Break mode.
O EXTEND	EXTEND	On while the computer is in the Extend mode.
O I-O HALT	IN-OUT HALT	On while the computer is executing an Input-Output Transfer wait.
O I-O COM'DS	IN-OUT COMMANDS	On while in-out transfer instructions can be executed.
O I-O SYNC	IN-OUT SYNC	On for the time between device completion and end of In-Out wait.

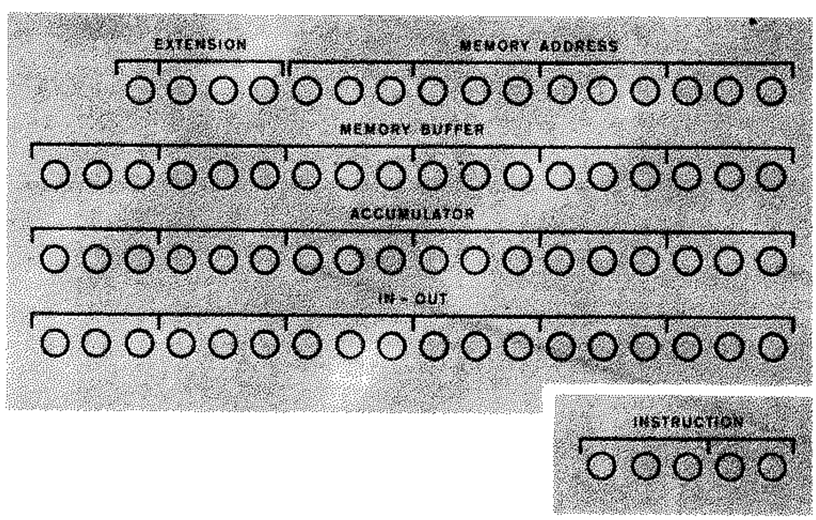


PROGRAM FLAGS — On after the computer has executred the Set Selected Program Flag instruction or an in-out device has been activated, indicating its readiness to be serviced. (Can only be turned off or cleared by executing the Clear Selected Program Flag instruction.)



REGISTER INDICATOR LIGHTS

PROGRAM COUNTER	Displays 12 or 16 bits which represent the address of the next instruction to be executed.
INSTRUCTION	Displays 5 bits which represent the basic operation code of the instruction being executed.
MEMORY ADDRESS	Displays 12 or 16 bits which represent the address of the instruction being executed (during cycle 0) or the address of the operand (in succeeding cycles)
MEMORY BUFFER	Displays 18 bits which represent the instruction being executed (operation code and address part during cycle 0) or the 18-bit operand (in succeeding cycles)
ACCUMULATOR	Displays the 18 bits of the Accumulator which represent the results of arithmetic and logical operations.
IN-OUT	Displays the 18 bits of the Input-Output Register which represent information just transferred in or out of the computer or the results of certain arithmetic and logical operations



Standard PDP-1 Instruction List

This list includes the title of the instruction, the normal execution time of the instruction, (i.e., the time with no indirect address,) the mnemonic code of the instruction, and the operation code number. In the following list, the contents of a register are indicated by C(). Thus C(Y) means the contents of memory at Address Y; C(AC) means the contents of the Accumulator; C(IO) means the contents of the In-Out Register. An alphabetical and numerical listing of the instructions is contained on pages 62 to 67.

MEMORY REFERENCE INSTRUCTIONS

ARITHMETIC INSTRUCTIONS

Add (10 µsec)
add Y Operation Code 40

The new C(AC) are the sum of C(Y) and the original C(AC). The C(Y) are unchanged. The addition is performed with 1's complement arithmetic. If the sum of two like-signed numbers yields a result of the opposite sign, the overflow flip-flop will be set (see Skip Group instructions). A result of minus zero is changed to plus zero.

Subtract (10 µsec)
sub Y Operation Code 42

The new C(AC) are the original C(AC) minus the C(Y). The C(Y) are unchanged. The subtraction is performed using 1's complement arithmetic. When two unlike-signed numbers are subtracted, the sign of the result must agree with the sign of the original Accumulator, or overflow flip-flop will be set (see Skip Group instructions). A result of minus zero can exist in one instance only: (-0) - (+0) = (-0)

Multiply (14 to 25 µsec)
mul Y Operation Code 54

The product of C(AC) and C(Y) is formed in the AC and IO registers. The sign of the product is in the AC sign bit. IO Bit 17 also contains the sign of the product. The magnitude of the product is the 34-bit string from AC Bit 1 throuh IO Bit 16. The C(Y) are not affected by this instruction. If the entire product results in a minus zero it is changed to a plus zero.

Divide (30 to 40 µsec, except on overflow, 12 µsec)
div Y Operation Code 56

The dividend must be in the AC and IO registers in the form indicated in the instruction, Multiply. IO bit 17 is ignored. The divisor is the C(Y). At the completion of the instruction, the C(AC) are the quotient and the C(IO) are the remainder. The sign of the remainder (in IO bit zero) is the sign of the dividend. The instruction that follows a DIV will be skipped unless an overflow occurs. The C(Y) are not affected by this instruction. If the remainder or quotient result is minus zero, that value is changed to plus zero.

If the magnitude of the high order part of the dividend is equal to or greater than the magnitude of the divisor, and overflow is indicated. In this case, the following instruction is not skipped. The original C(AC) and C(IO) are restored. The overflow flip-flop is not affected.

Index (10 µsec)
idx Y Operation Code 44

The C(Y) are replaced by C(Y) + 1 which are left in the Accumulator. The previous C(AC) are lost. Overflow is not indicated. If the original C(Y) equals the integer, -1, the result after indexing is plus zero.

Index and Skip if Positive (10 µsec)
isp Y Operation Code 46

The C(Y) are replaced by C(Y) + 1 which are left in the Accumulator. The previous C(AC) are lost. If, after the addition, the Accumulator is positive, the Program Counter is advanced one extra position and the next instruction in the sequence is skipped. Overflow is not indicated. If the original C(Y) equals the integer, -1, the result after indexing is plus zero and the skip takes place.

LOGICAL INSTRUCTIONS

Logical AND (10 µsec)
and Y Operation Code 02

The bits of C(Y) operate on the corresponding bits of the Accumulator to form the logical AND. The result is left in the Accumulator. The C(Y) are unaffected by this instruction.

LOGICAL AND TABLE

AC Bit	Y Bit	Result
0	0	0
0	1	0
1	0	0
1	1	1

Exclusive OR (10 µsec)
xor Y Operation Code 06

The bits of C(Y) operate on the corresponding bits of the Accumulator to form the exclusive OR. The result is left in the Accumulator. The C(Y) are unaffected by this order.

EXCLUSIVE OR TABLE

AC Bit	Y Bit	Result
0	0	0
0	1	1
1	0	1
1	1	0

Inclusive OR (10 µsec)
ior Y Operation Code 04

The bits of C(Y) operate on the corresponding bits of the Accumulator to form the inclusive OR. The result is left in the Accumulator. The C(Y) are unaffected by this order.

INCLUSIVE OR TABLE

AC Bit	Y Bit	Result
0	0	0
0	1	1
1	0	1
1	1	1