GENERAL INSTRUCTIONS

Load Accumulator (10 µsec)
lac Y Operation Code 20

The C(Y) are placed in the Accumulator. The C(Y) are unchanged. The original C(AC) are lost

Deposit Accumulator (10 µsec)
dac Y Operation Code 24

The C(AC) replace the C(Y) in the memory. The C(AC) are left unchanged by this instruction. The C(Y) are lost.

Deposit Address Part (10 µsec)
dap Y Operation Code 26

Bits 6 through 17 of the Accumulator replace the corresponding digits of memory register Y. C(AC) are unchanged as are the contents of Bits 0 through 5 of Y. The original contents of Bits 6 through 17 of Y are lost.

Deposit Instruction Part (10 µsec)
dip Y Operation Code 30

Bits 0 through 5 of the Accumulator replace the corresponding digits of memory register Y. The Accumulator is unchanged as are bits 6 through 17 of Y. The original contents of Bits 0 through 5 of Y are lost.

Load In-Out Register (10 µsec)
lio Y Operation Code 22

The C(Y) are placed in the In-Out register. C(Y) are unchanged. The original C(IO) are lost.

Deposit In-Out Register (10 µsec)
dio Y Operation Code 32

The C(IO) replace the C(Y) in memory. The C(IO) are unaffected by this instruction. The original C(Y) are lost.

Deposit Zero in Memory (10 µsec)
dzm Y Operation Code 34

Clears (sets equal to plus zero) the contents of register Y.

Execute (5 µsec plus time of instruction executed)
xct Y Operation Code 10

The instruction located in register Y is executed. The Program Counter remains unchanged (unless a jump or skip were executed). If a skip instruction is executed (by xct y), the next instructions to be executed will be taken from the address of the xct y plus one or the the address of the xct y plus two depending on the skip condition. Execute may be indirectly addressed, and the instruction being executed may use indirect addressing. An xct instruction may execute other xct commands.

Jump (5 µsec)
jmp Y Operation Code 60

The next instruction executed will be taken from Memory Register Y. The Program Counter is reset to Memory Address Y. The original contents of the Program Counter are lost.

Jump and Save Program Counter (5 µsec)
jsp Y Operation Code 62

The contents of the Program Counter are transferred to bits 6 through 17 of the AC. The state of the overflow flip-flop is transferred to bit zero, the condition of the Extend flip-flop to bit 1, and the contents of the Extended Program Counter to bits 2, 3, 4, and 5 of the AC. When the transfer takes place, the Program Counter holds the address of the instruction following the jsp. The Program Counter is then reset to Address Y. The next instruction executed will be taken from Memory Register Y. The original C(AC) are lost.

Call Subroutine (10 µsec)
cal Y Operation Code 16

The address part of the instruction, Y, is ignored. The contents of the AC are deposited in Memory Register 100. The contents of the Program Counter (holding the address of the instruction following the cal) are transferred to bits 6 through 17 of the AC. The state of the overflow flip-flop, the Extend flip-flop, and Extended Program Counter are saved as described under jsp. The next instruction executed is taken from Memory Register 101. The cal instruction requires that the indirect bit be zero. The instruction may be used as part of a master routine to call subroutines.

Jump and Deposit Accumulator (10 µsec)
jda Y Operation Code 17

The contents of the AC are deposited in Memory Register Y. The contents of the Program Counter (holding the address of the instruction following the jda) are transferred to bits 6 through 17 of the AC. The state of the overflow flip-flop, the Extend flip-flop, and Extended Program Counter are saved as described under jsp. The next instruction executed is taken from Memory Register Y + 1. The jda instruction requires that the indirect bit be a one, but indirect addressing does not occur. The instruction is equivalent to the instruction dac Y followed by jsp Y + 1. Skip if Accumulator and Y differ (10 usec) sad Y Operation Code 50 The C(Y) are compared with the C(AC). If the two numbers are different, the Program Counter is indexed one extra position and the next instruction in the sequence is skipped. The C(AC) and the C(Y) are unaffected by this operation.

Skip if Accumulator and Y are the same (10 µsec)
sas Y Operation Code 52

The C(Y) are compared with the C(AC). If the two numbers are identical, the Program Counter is indexed one extra position and the next instruction in the sequence is skipped. The C(AC) and the C(Y) are unaffected by this operation.

AUGMENTED INSTRUCTIONS

Load Accumulator with N (5 µsec)
law N Operation Code 70

The number in the memory address bits of the instruction word is placed in the Accumulator. If the indirect address bit is ONE, (-N) is put in the Accumulator.

Shift Group (5 µsec)
sft Operation Code 66

This group of instructions will rotate of shift the Accumulator and/or the In-Out Register. When the two registers operate combined, the In-Out Register is considered to be and 18-bit magnitude extension of the right end of the Accumulator.

Rotate is a non-arithmetic cyclic shift. That is the two ends of the register are logically tied together and information is rotated as though the reigster were a ring.

Shift is an arithmetic operation and is, in effect, multiplication of the number in the register by 2^N, where N is the number of shifts; plus is left and minus is right. As bits are shifted out from one end of a register they are replaced at the other end by ones if the number negative and zeroes if the number is positive. The sign bit is not shifted.

The number of shift or rotate steps to be performed (N) is indicated by the number of ONE's in Bits 9 through 17 of the instruction word. Thus Rotate Accumulator Right nine times is 671777. A shift or rotate of one place can be indicated nine different ways. The usual convention is to use the right end of the instruction word (rar 1 = 671001).

When operating the PDP-1 in the single-step or single-instruction mode, shift group instructions may appear to operating incorrectly (i.e., judging from the indicator lights of the control console). This occurs because some shift group instructions overlap into the beginning of the next instruction.

Rotate Acumulator Right (5 µsec)
rar N Operation Code 671

Rotates the bits of the Accumulator right N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Rotate Acumulator Left (5 µsec)
ral N Operation Code 661

Rotates the bits of the Accumulator left N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift Acumulator Right (5 µsec)
sar N Operation Code 675

Shifts the contents of the Accumulator Right N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift Acumulator Left (5 µsec)
sal N Operation Code 665

Shifts the contents of the Accumulator left N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Rotate In-Out Register Right (5 µsec)
rir N Operation Code 672

Rotates the bits of the In-Out Register right N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Rotate In-Out Register Left (5 µsec)
ril N Operation Code 662

Rotates the bits of the In-Out Register left N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift In-Out Register Right (5 µsec)
sir N Operation Code 676

Shifts the contents of the In-Out Register right N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift In-Out Register Left (5 µsec)
sil N Operation Code 666

Shifts the contents of the In-Out Register left N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Rotate AC and IO Right (5 µsec)
rcr N Operation Code 673

Rotates the bits of the combined registers right in a single ring N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Rotate AC and IO Left (5 µsec)
rcl N Operation Code 663

Rotates the bits of the combined registers left in a single ring N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift AC and IO Right (5 µsec)
scr N Operation Code 677

Shifts the contents of the combined registers right N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Shift AC and IO Left (5 µsec)
scl N Operation Code 667

Shifts the contents of the combined registers left N positions, where N is the number of ONE's in Bits 9-17 of the instruction word.

Skip Group (5 µsec)
skp Operation Code 64

This group of instructions senses the state of various flip-flops and switches in the machine. The address portion of the instruction selects the particular function to be sensed. All members of this group have the same operation code. The instructions in the Skip Group may be combined to form the inclusive OR of the separate skips. Thus, if Address 3000 is selected, the skip would occur if the overflow flip-flop equals ZERO or if the In-Out Register is positive.

The combined instruction would still take 5 microseconds.

The intent of any skip instruction can be reversed by making Bit 5 (normally the Indirect Address Bit) equal to One. For example, the Skip on Zero Accumulator instruction, with Bit euqal to one, becomes Do Not Skip on Zero Accumulator.

Skip on ZERO Accumulator (5 µsec)
sza Address 0100

If the Accumulator is equal to plus ZERO (all bits are ZERO), the Program Counter is advanced one extra position and the next instruction in the sequence is skipped.

Skip on Plus Accumulator (5 µsec)
spa Address 0200

If the sign bit of the Accumulator is ZERO, the Program Counter is advanced one extra position and the next instruction in the sequence is skipped.

Skip on Minus Accumulator (5 μsec)
sma Address 0400

If the sign bit of the Accumulator is ONE, the Program Counter is advanced one extra position and the next instruction in the sequence is skipped.

Skip on ZERO Overflow (5 μsec)
szo Address 1000

If the overflow flip-flop is a ZERO, the Program Counter is advanced one extra position and the next instruction in the sequence is skipped. The overflow flip-flop is cleared by the instruction. This flip-flop is set only by an addition or subtraction that exceeds the capacity of the Accumulator. (See definition of add and subtract instructions). The overflow flip-flop is not cleared by arithmetic operations which do not cause an overflow. Thus, a whole series of arithmetic operations can be checked for correctness by a single szo. The overflow flip-flop is cleared by the "Start" Switch.

Skip on Plus In-Out Register (5 μsec)
spi Address 2000

If the sign digit of the In-Out Register is ZERO, the Program Counter is indexed one extra position and the next instruction in the sequence is skipped.

Skip on Plus ZERO Switch (5 μsec)
szs Addresses 0010, 0020, ... 0070

If the selected Sense Switch is ZERO, the Program Counter is advanced one extra position and the next instruction in the sequence is skipped. Address 10 senses the position of Sense Switch 1, Address 20 Switch 2, etc. Address 70 senses all the switches If 70 is selected all 6 switches must be ZERO to cause the skip.

Operate Group (5 μsec)
opr Operation Code 76

This instruction group performs miscellaneous operations on various Central Processor Registers. The address portion of the instruction specifies the action to be performed.

The instructions in the Operate Group can be combined to give the union of the functions. The instruction opr 3200 will clear the AC, put TW to AC, and complement AC.

Clear In-Out Register (5 μsec)
cli Addres 4000

Clears (sets equal to plus zero) the In-Out Register.

Load Accumulator from Test Word (5 μsec)
lat Address 2000

Forms the inclusive OR of the C(AC) and the contents of the Test Word. This instruction is usually combined with Address 0200 (Clear Accumulator), so that C(AC) wil equal the contents of the Test Word Switches.

Load Accumulator with Program Counter (5 μsec)
lap Address 0100

Forms the inclusive OR of the C(AC) and the contents of the Program Counter (which contains the address of the instruction following the lap) in AC bits 6 through 17. Also, the inclusive OR of AC bit zero and the state of the overflow flip-flop is formed in AC bit zero. This instruction is usually combined with address 0200 (clear accumulator) so that the C(AC) will equal the contents of the overflow flip-flop (in AC bit zero) and the contents of the Program Counter (in AC bits 6 through

17). The contents of the Extend flip-flop are transferred to AC bit 1, the contents of the Extended Program Counter to bits 2, 3, 4, and 5.

Complement Accumulator (5 µsec)
cma Address 1000

Complements (changes all ones to zeroes and all zeroes to ones) the contents of the Accumulator.

Halt
hlt Address 0400

Stops the computer. Clear Accumulator (5 usec) cla Address 0200 Clears (sets equal to plus zero) the contents of the Accumulator.

Clear Selected Program Flag (5 µsec)
clf Address 0001 to 0007

Clears the selected program flag. Address 01 clears Program Flag 1, 02 clears Program Flag 2, etc. Address 07 clears all program flags.

Set Selected Program Flag (5 µsec)
stf Address 0011 to 0017

Sets the selected program flag. Address 11 sets Program Flag 1; 12 sets Program Flag 2, etc. Address 17 sets all program flags.

No Operation (5 µsec)
nop Address 0000

The state of the computer is unaffected by this operation, and the Program Counter continues in sequence.

In-Out Transfer Group (5 µsec without in-out wait
iot Operation Code 72

The variations within this group of instructions perform all the in-out control and information transfer functions. If Bit 5 (normally the Indirect Address bit) is a ONE, the computer will enter a special waiting state until the completion pulse from the activated device has returned. When this device delivers its completion, the computer will resume operation of the instruction sequence.

The computer may be interrupted from the special waiting state to serve a sequence break request or a high speed channel request.

Most in-out operations require a known minimum time before completion. This time may be utilized for programming. The appropriate In-Out Transfer can be given with no in-out wait (Bit 5 a ZERO and Bit 6 a ONE). The instruction sequence then continues. This sequence must include an iot instruction 730000 which performs nothing but the in-out wait. The computer will then enter the special waiting state until the device returns the in-out restart pulse. If the device has already returned the completion pulse before the instruction 730000, the computer will proceed immediately.

Bit 6 determines whether a completion pulse will or will not be received from the in-out device. When it is different than Bit 5, a completion pulse will be received. When it is the same as Bit 5, a completion pulse will not be received.

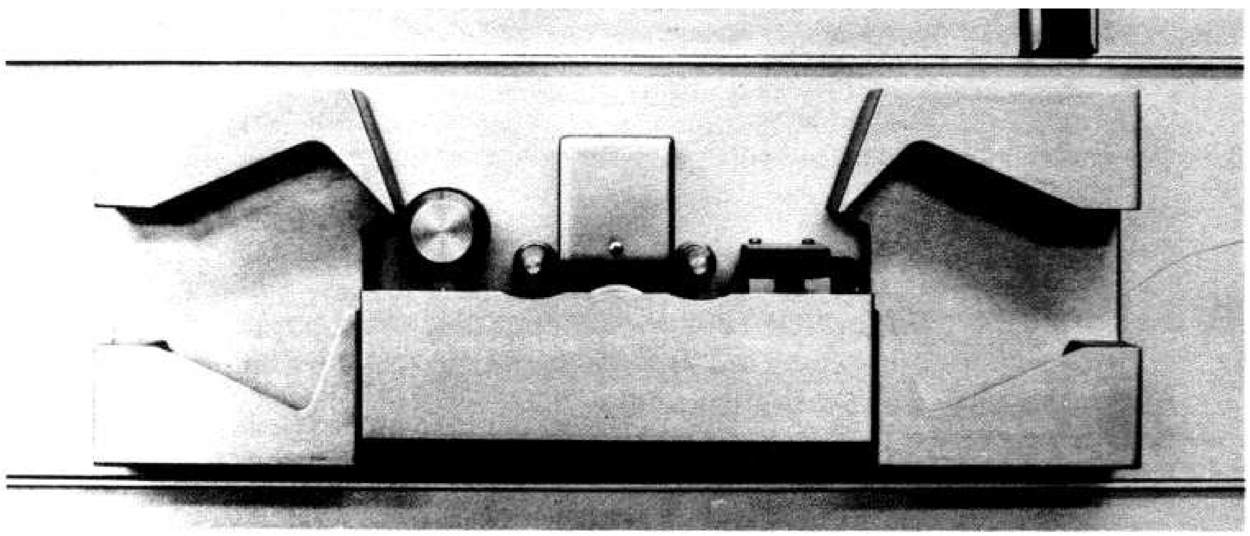
In addition to the control function of Bits 5 and 6, Bits 7 through 11 are also used as control bits serving to extend greatly the power of the iot instructions. For example, Bits 12 through 17, which are used to designate a class of input or output devices such as typewriters, may be further defined by Bits 7 through 11 as referring to Typewriter 1, 2, 3, etc. In several of the optional in-out devices, in particular the magnetic tape, Bits 7 through 11 specify particular functions such as forward, backward etc. If a large number of specialized devices are to be attached, these bits may be used to further the in-out transfer instruction to perform totally distinct functions.

STANDARD AND OPTIONAL EQUIPMENT

Standard Equipment

PERFORATED TAPE READER

The Perforated Tape Reader of the PDP-1 is a photoelectric device capable of reading 400 lines per second. Three lines form the standard 18-bit word when reading binary punched 8-hole tape. Five, six and seven hole tape may also be read.



High Speed Perforated Tape Reader

Read Perforated Tape, Alphanumeric
rpa Address 0001

This instruction reads one line of tape (all eight Channels) and transfers the resulting 8-bit code to the Reader Buffer. If bits 5 and 6 of the rpa function are both zero (720001), the contents of the Reader Buffer must be transferred to the IO Register by executing the rrb instruction. When the Reader Buffer has information ready to be transferred to the IO Register, Status Register Bit 1 is set to one. If bits 5 and 6 are different (730001 or 724001) the 8-bit code read from tape is automatically transferred to the IO Register via the Reader Buffer and appears as follows:

IO Bits	10	11	12	13	14	15	16	17
TAPE CHANNELS	8	7	6	5	4	3	2	1

The remaining bits of the IO Register are set to zero.

The code of the off-line tape preparation typewriter (Friden FIO-DEC Recorder- Reproducer) contains an odd parity bit. This bit may be checked by the read-in program. The FIO-DEC Code can then be converted to the Concise (6-bit) Code used by PDP-1 merely by dropping the eighth bit (parity).

A list of characters and their FIO-DEC and Concise Codes can be found on pages 68 and 69.

Read Perforated Tape, Binary rpb
Address 0002

The instruction reads three lines of tape (six Channels per line) and assembles the resulting 18-bit word in the Reader Buffer. For a line to be recognized by this instruction Channel 8 must be punched (lines with Channel 8 not punched will be skipped over). Channel 7 is ignored. The instruction sub 5137, for example, appears on tape and is assembled by rpb as follows:

Channel	8	7	6	5	4	|	3	2	1
Line 1	X		X			|		X	
Line 2	X		X		X	|			X
Line 3	X			X	X	|	X	X	X

Reader Buffer 100 010 101 001 011 111

(Vertical dashed line indicates sprocket holes and the symbols "X" indicate holes punched in tape).

If bits 5 and 6 of the rpb instruction are both zero (720002), the contents of the Reader Buffer must be transferred to the IO Register by executing a rrb instruction. When the Reader Buffer has information ready to be transferred to the IO Register, Status Register Bit 1 is set to one. If bits 5 and 6 are different (730002 or 724002) the 18-bit word read from tape is automatically transferred to the IO Register via the Reader Buffer.

Read Reader Buffer
rrb Address 0030

When the rpa or rpb instructions are given with bits 5 and 6 both zero (720001 or 720002) information read from tape fills the Reader Buffer, but is not automatically transferred to the IO Register. To accomplish the transfer, these instructions must be followed by a rrb instruction. In addition, the rrb instruction clears Status Register Bit 1.

Read-In Mode

This is a special mode activated by the "Read-In" switch on the console. It provides a means of entering programs which does not rely on programs already in memory. Pushing the "Read-In" switch starts the reader in the binary mode. The first group of three lines, and alternate succeeding groups of three lines, are interpreted as "Read-In" mode instructions. Even-numbered groups o three lines are data. The "Read-In" mode instructions must be either "deposit in-out" (dio Y) or "jump" (jmp Y). If the instruction is dio Y, the next group of three binary lines will be stored in memory location Y and the reader continues moving. If the instruction is jmp Y, the "Read-In" mode is terminated, and the computer will commence operation at the address of the jump instruction.

PERFORATED TAPE PUNCH