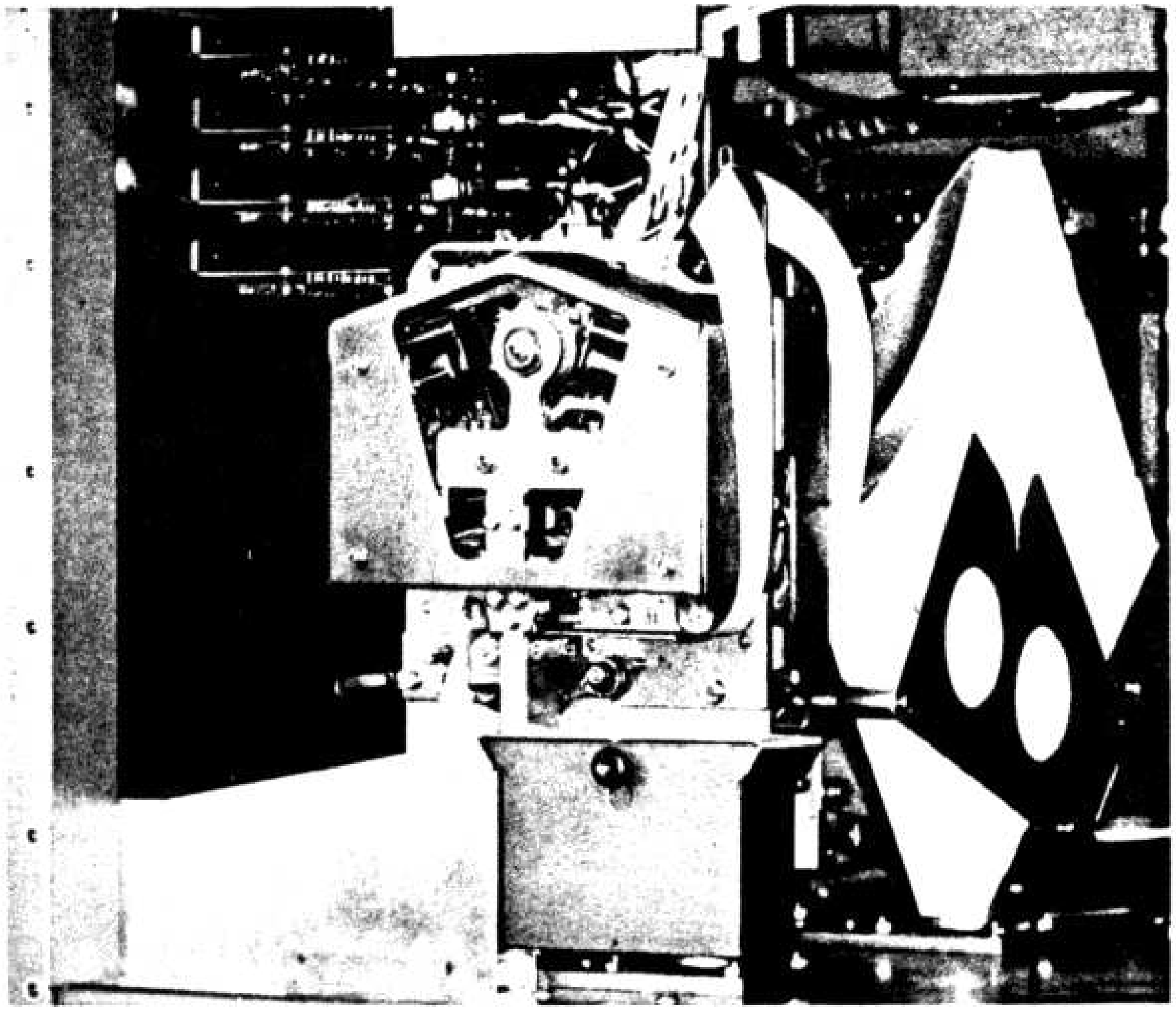
The standard PDP-1 Perforated Tape Punch operates at a speed of 63 lines per second. It can operate in either the alphanumeric mode or the binary mode.



Perforated Tape Punch

Punch Perforated Tape, Alphanumeric
ppa Address 0005

For each In-Out Transfer instruction one line of tape is punched. In-Out Register Bit 17 conditions Hole 1. Bit 16 conditions Hole 2, etc. Bit 10 conditions Hole 8.

Punch Perforated Tape, Binary
ppb Addres 0006

For each In-Out Transfer instruction one line of tape is punched. In-Out Register Bit 5 conditions Hole 1. Bit 4 conditions Hole 2, etc. Bit 0 conditions Hole 6. Hole 7 is left blank. Hole 8 is always punched in this mode.

ALPHANUMERIC ON-LINE TYPEWRITER

The typewriter will operate in the input mode or the output mode.

Alphanumeric Typewriter Keyboard

Type Out
tyo Address 0003

For each In-Out Transfer instruction one character is typed. The character is specified by the right six bits of the In-Out Register.

Type In
tyi Address 0004

This operation is completely asynchronous and is therefore handled differently than any of the preceding in-out operations.

When a typewriter key is struck, the code for the struck key is placed in the typewriter buffer, Program Flag 1 is set, and the type-in status bit is set to one. A program designed to accept typed-in data would periodically check Program Flag 1, and if found to be set, an In-Out Transfer Instruction with address 4 could be executed for the information to be transferred to the In-Out Register. This In-Out Transfer should not use the optional in-out wait. The information contained in the typewriter buffer is then transferred to the right six bits of the In-Out Register. The tyi instruction automatically clears the In-Out Register before transferring the information and also clears the type-in status bit.

SEQUENCE BREAK MODE

The purpose of the Sequence Break Mode (or program interrupt) is to allow concurrent operation of several in-out devices and the main program sequence. It also provides a means of indicating to the computer that an in-out device is ready to accept or furnish data.

Interrupt requests can be received from any number of in-out devices. Each such request sets a unique status bit. If the channel is free, the main program sequence is interrupted after completion of the current memory cycle and the C(AC) are automatically stored in memory location zero, the C(PC) in location 1, and the C(IO) in location 2. The time required to accomplish this is 15 µsec. The C(PC) as stored in location includes the state of the overflow flip-flop in bit zero. The Program Counter is then reset to the address 0003 and the program begins operating in the new sequence. The program beginning at location 0003 is usually designed to inspect the status bits, through the use of the Check Status instruction, to determine which in-out device caused the interrupt. A jump to the appropriate in-out subroutine can then be executed. Each such subroutine is terminated by the following instructions:

lac	0000 (to restore the AC)
lio	0002 (to restore the IO)
jmp (indirect)	0001 (to resume the main program)

The last of these three instructions restores the overflow and PC flip-flops and frees the channel thus allowing the next interrupt request received by the system to be processed. Interrupt requests that occurred while the channel was busy set status bits, and cause interrupts when the channel next becomes free.

In the standard PDP-1 the reader, punch, and typewriter are attached to the One-Channel Sequence Break System and five status bits are defined (see Check Status instruction). The number of status bits is expanded as required by optional in-out equipment.

Three instructions are directly associated wih the One-Channel Sequence Break System on the standard PDP-1:

Enter Sequence Break Mode
esm Address 0055

This instruction turns on the Sequence Break System, allowing automatic interrupts to the main sequence to occur.

Leave Sequence Break Mode
lsm Address 0054

This instruction turns off the Sequence Break System, thus preventing interrupts to the main sequence. Should interrupt requests occur while the system is off, the status bits will, nevertheless continue to be set.

Clear Sequence Break System
cbs Address 0056

This instruction clears certain control flip-flops in the Sequence Break System thus nullifying the effect of any interrupt requests just granted or about to be granted (i.e., just prior to the transfer of the C(AC) to location zero).

CHECK STATUS

Check Status
cks Address 0033

This instruction checks the status of various in-out devices and sets IO Bits 0 through 6 for subsequent program interrogation as follows:

IO Bit Positions	Status Register Defintions
0	Set to 1 when light-pulse strikes pen Set to 0 at the start of each dpy instruction
1	Set to 1 when Punched Tape Reader Buffer has information ready to be transferred to IO Register Set to 0 be the reader return pulse or by the rrb instruction
2	Set to 1 when typewriter is free to receive a tyo instruction Set to 0 at the start of each tyo instruction
3	Set to 1 when typewriter key is struck Set to 0 by completion of tyi instruction
4	Set to 1 when tape punch is free to receive a ppa or ppb instruction Set to 0 at the start of each ppa or ppb instruction
5	Set to 1 when Type 23 Drum address equals address specified by dba instruction Set to 0 by the dcc instruction
6	Set to 1 on entering the Sequence Break mode Set to 0 on leaving the Sequence Break mode

Central Processor Options

PROGRAMMED MULTIPLY AND DIVIDE

In order to maintain compatibility with older programs, and in cases where the maximum automatic multiply and divide times are not allowable, switches are provided to select programmed multiply and divide, using the following instructions:

Multiply Step (10 µsec)
mus Y Operation Code 54

Bit 17 of the In-Out Register is a ONE, the C(Y) are added to C(AC). If IO Bit 17 is a ZERO, the addition does not take place. In either case, the C(AC) and C(IO) are rotated right one place. AC Bit 0 is made ZERO by this rotate. This instruction is used in the multiply subroutine.

Divide Step (10 µsec)
dis Y Operation Code 56

The Accumulator and the In-Out Register are rotated left one place. IO Bit 17 receives the complement of AC Bit 0. If IO Bit 17 is ONE, the C(Y) are subtracted from C(AC).

If IO Bit 17 is ZERO, C(Y) + 1 are added to C(AC). This instruction is used in the divide subroutine A result of minus zero is changed to plus zero.

MEMORY MODULE (TYPE 12)

Each Memory Module consists of 4096, 18-bit words. A maximum of sixteen such modules may be connected to the PDP-1 thus allowing for a maximum memory capacity of 65536 words.

MEMORY EXPANSION CONTROL (TYPE 15)

This control allows for memory expansion beyond 4096 to a maximum of 65536 18-bit words in increments of 4096-word modules. It provides a single-level, indirect address mode called “extend”, in addition to the normal multiple-level, indirect address mode of the standard PDP-1. A toggle switch labelled “extend”, which is on the control console, provides for initial selection of the extend or normal mode in conjunction with the use of the Start of Read-In Push-Buttons. During the operation of the program, the extend or normal mode can be selected as required through the use of two instructions provided with this options:

Enter Extend Mode (5 µsec)
eem 724074

This instruction places the computer in the single-level, indirect address mode called “extend”. In this mode, all memory reference instructions that are indirectly addressed refer to the location of a word which is taken as a 16-bit effective address. This address is contained in bits 2 through 17 of the specified word. The Program Counter (PC) and the Memory Address Register (MA) both become 16-bit registers. When a jsp, jda, cal, or lap (with address 300) instruction is executed, the AC receives the state of the overflow flip-flop in bit zero, the state of the indirect address mode (extend = 1, normal = 0) in bit 1, and the contents of the extended Program Counter in bits 2 through 17. Instructions not indirectly addressed are executed as in the standard PDP-1, but refer to the 4096 words in the memory module designated by the program counter extension, PC bits 2 through 5. Only bits 6 through 17 of the extended Program Counter act as a counter. Therefore, unless a transfer of control is indicated, an instruction in location 7777 is followed by the instruction in location 0000 of the same memory module, as specified by PC bits 2 through 5. In the extend mode, the cal instruction used memory locations 0100 and 0101 in memory module designated by the extended Program Counter, PC bits 2 through 5.

Leave Extend Mode (5 µsec)
lem 720074

This instruction places the computer in the multiple-level, indirect address mode called “normal”. In this mode, the PDP-1 operates as usual and all addresing refers to the 4096 words in the memory module designated by the program counter extension, PC bits 2 through 5. As in the extend mode, the instructions jsp, jda, cal, and lap (with address 300) supply the AC with the contents of the overflow, indirect address mode, and PC flip-flops. In the normal mode, the cal instruction uses memory locations 0100 and 0101 in the memory module designated by the program counter extension, PC bits 2 through 5.

High Speed Channel transfers performed with extended memory refer directly to any of

65536 memory locations, regardless of the state of the indirect address mode (extend or normal).

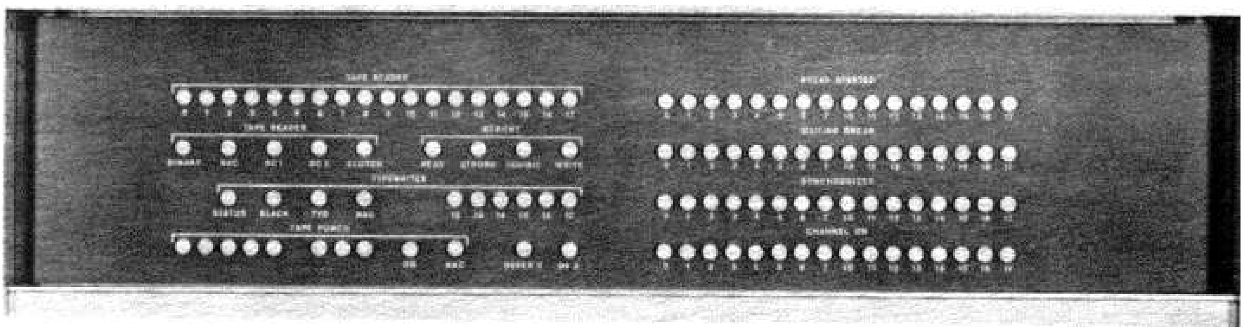
Sequence break operations with extended memory use Memory Module zero, locations 00 through 03 (one-channel system) or 00 through 77 (sixteen-channel system) to store the C(AC), C(PC), and C(IO) and to jump to the new sequence. The C(PC) as stored in the second fixed location assigned to each channel includes the state of the overflow flip-flop in bit zero, the state of the indirect address mode (extend = 1, normal = 0) in bit 1, and the contents of the extended Program Counter in bits 2 through 17. At the beginning of a sequence break the overflow and indirect addres mode flip-flops are automatically set to zero. The indirect jump that terminates a sequence break requires the Sequence Break System to be on, temporarily places the computer in the extend mode, then restores the overflow, indirect address mode, and PC flip- flops to their previous stages (i.e., just prior to the beginning of the sequence break).

HIGH SPEED CHANNEL CONTROL (TYPE 19)

This control is used in conjunction with the High Speed Data Control (Type 131). A maximum of three such channels can be attached to the PDP-1 through this control. Automatic Magnetic Tape Control Type 52 includes the installation of a Type 19 control. A high speed channel is used to automatically transfer blocks of words between core memory and an in-out device. Each channel is automatically interrogated at the completion of each memory cycle on a priority basis. The priority is wired and fixed. The Sequence Break System has an overall priority just below that of the lowest priority high speed channel. When wired to this channel, a device communicates directly with memory through the Memory Buffer Register, by passing the IO Register. After proper initiation, data transfers proceed without disturbing the main program. If the channel has a word for or needs a word from the memory, the current program sequence pauses for on memory cycle (5 µsec) to serve that channel, then continues. The maximum rate of transfer is 200,000 (18-bit) words per second.

SEQUENCE BREAK SYSTEM (TYPE 120)

The purpose of the Sequence Break System (or program interrupt system) is to allow concurrent operation of several in-out devices and the main program sequence. This system has, nominally, sixteen automatic interrupt channels arranged in a priority chain. Four fixed and unique memory locations are assigned to each sequence break channel. Channel zero (highest priority) uses locations 0, 1, 2, and 3; channel one uses locations 4, 5, 6, and 7; etc. A break to a particular sequence can be initiated by the completion of an in-out device, the program or any external signal. If this sequence has priority, the C(AC) are automatically stored in the first of four assigned memory location, the C(PC) in the second,. and the C(IO) in the third. The time required to accomplish this is 15 microseconds (during which other interrupts cannot occur). The C(PC) as stored in the second location includes the state of the overflow flip-flop in bit zero. The Program Counter is reset to the addres of the fourth fixed location and the program begins operating in the new sequence. This new sequence may be broken by a higher priority sequence. A typical program for handling an in-out sequence would contain several instructions, including the appropriate IOT instruction. These are followed by load AC and load IO from their fixed locations and an indirect jump to the location of the previous C(PC). This last instruction also restores the previous state of the overflow flip-flop and terminates the sequence.



Sequence Break Indicator Panel

When the Type 120 Sequence Break System is installed in the PDP-1, the standard one-channel system is removed. The three instructions asociated with the one-channel system are retained and four additional instructions are provided:

Deactivate Sequence Break Channel
dsc 72kn50
: Turn off the channel specified by kn, where kn equals 00 for channel zero, 01 for channel one, etc., and 17 for channel fifteen.

Activate Sequence Break Channel
asc 72kn51
: Turn on the channel specified by kn.

Initiate Sequence Break
isb 72kn52
: Initiate a sequence break on the channel specified by kn regardless of whether the channel is on or off.

Clear All Channels
cac 720053
: Turns off all sixteen channels.

Sequence Break Systems with 32, 64, 128, and 256 channels are also available and operate in the same manner.

HIGH SPEED DATA CONTROL (TYPE 131)

The High Speed Data Control Type 131 automatically transfers data between the PDP-1 and an input-output device. After proper inititialization, data-transfers to and from the Data Control proceed concurrently with the main computer program. The maximum transfer rate is 200,000 18-bit words per second, based on the 5 µsec computer memory cycle.

A maximum of three Data Controls can be attached to a Type 19 High Speed Channel Control of the PDP-1. Each Data Control is asigned a priority to halt the program for data transfers with core memory. Each Data Control can operate three devices, one at a time. The Type 131 contains five major registers:

ONE BUFFER (1 Buf)

An 18-bit register acting as an intermediate storage buffer for Memory Buffer Register information received from the High Speed Channel Control or an external device. During incoming transfers it is an intermediate buffer between the Data Word Buffer (DWB) of the external device and the Two Buffer.

TWO BUFFER (2 Buf)

An 18-bit registed tha holds outgoing information to be transferred into the DWB of an external device or into the Memory Buffer Register of the computer during a high speed channel transfer.

DEVICE REGISTER (D Reg)

A 3-bit static register used to control the flow of information and connect the desired external device. The register is loaded from the Memory Buffer Register buss.

INITIAL LOCATION COUNTER (ILC)

A 16-bit register that contains the address of the next data word to be transferred and is advanced one each time a data word is transferred. This register is loaded from the IO Register.

WORD COUNTER (WC)

A 16-bit register containing the complement of the number of words remaining to be transferred in the data block. The counter is ad- vanced one each time a word is transferred to an external device DWB. Note that the Word Counter outputs are decoded and combined with logic levels to stop all further high speed channel requests at the proper time. This register is loaded from the IO Register.

The IOT instruction structure for the Type 131 Data Control is 72xxyy, where

72 specifies IOT

xx microprogramming

yy Data Control selection

Set Word Counter

swc Address x046

Transfers the contents of the IO Register into the Word Counter in the Data Control. the contents