## OMNIBUS MAGNETIC TAPE OPTIONS

The OMNIBUS Magnetic Tape Options include:

a. The TD8-EM Dual DECtape Transport Control and TU56 Dual DECtape Transport
b. The TM8-E DECmagtape Transport Control and TU10 DECmagtape transport

### DECtapes

The DECtape unit can interface directly with the OMNIBUS via the TD8-E or to the External Bus via the TC08. The configurations are defined in the following table. For information on the TC08 Controller, refer to section 4 of this chapter.

Four basic DECtape configurations are identified in the following table.

| SYSTEM DESIGNATION | DECtape | CONTROL | PREREQUISITE | REMARKS |
|---|---|---|---|---|
| None | TU56 (Dual Drive) | TC08 | KA8-E* KD8-E PDP-8/E | Up to 4 Dual TU56's per control. (8 drive units) |
| None | TU56H (Single Drive) | TC08 | KA8-E* KD8-E PDP-8/E | Up to 4 single DECtape drive units. |
| TD8-EM | TU56-M (Dual Drive) | TD8-E | PDP-8/E | Control plugs into OMNIBUS. |
| TD8-EH | TU56-MH (Single Drive) | TD8-E | PDP-8/E | Control plugs into OMNIBUS. |

### TD8-E DECtape Option

The DECtape system is a standard option for the PDP-8/E that serves as an auxiliary magnetic tape data storage facility. The DECtape system stores information at fixed positions on magnetic tape, as in magnetic disk or drum storage devices, rather than at unknown or variable positions, as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information has a number of features to improve its reliability and make it exceptionally useful for program updating and program editing applications. These features are: phase or polarity sensed recording on redundant tracks, bidirectional reading and writing, and a simple mechanical mechanism util-

* Magnetic tape options operated on the external bus of the PDP-8/E require the use of the KA8-E Positive I/O Bus Interface module and the KD8-E Data Break Interface module as prerequisites.

izing hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion).

**Specifications**

| | |
|---|---|
| Tape Characteristics | Capacity—260 feet of ¾ inch, 1 mil Mylar sandwich tape, coated both sides.<br>Reel diameter—3.9 inches<br>Tape Handling—direct drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers are used.<br>Speed—97 ± 14 ips<br>Density—350 ± 55 bpi<br>Information capacity—$2702_8$ Blocks with $201_8$ 12-bit words per block (188,672 12-bit words)<br>Tape Motion—bi-directional |
| Word Transfer Rate | 33,300 3-bit characters per second |
| Addressing | Mark and timing tracks allow searching for a particular block by number in a forward or backward direction. |
| Tape Motion Timing | Start Time—150 msec ± 15 msec<br>Stop time—100 msec ± 10 msec<br>Turn around time—200 msec ± 20 msec |
| Mounting | TU56 Drive mounts in a standard 19 inch equipment rack |
| Size | 10 ½ inches high<br>19 inches wide<br>9 ¾ inches deep } TU56 Drive<br>1 Quad Module } TD8-E Control plugs into OMNIBUS |
| Cooling | Internally mounted fan provided for TU56 |
| Environmental Conditions | Temperature—40°F to 90°F<br>Note: The magnetic tape manufacturer recommends 40-60% relative humidity and 60° to 80° as an acceptable operating environment for DECtape. |

**Tape Compatibility**

Tapes may be certified, programmed, read, modified, and rewritten interchangeably on either the larger automatic DECtape units (TC08/TC01) or on the TD8-E. *DEC provides all the necessary subroutines and* MAINDECs for the TD8-E; for example:

- Read/Write Subroutines
- Tape Certification Routine
- MAINDEC Maintenance Programs

- PS/8 Programming System (12K Minimum Configuration)
- A new 4K Keyboard Operating System with Program Directory, Line Editor, and PAL III* Assembler.
- A DECtape Copy Program

* (A Paper Tape Device is required; either ASR-33 or PC8-E, for input and output with PAL-III.)

**TD8-E DECTAPE CONTROL**

The TD8-E is a low cost interface for the TU56 DECtape units. A TD8-EM consists of a TD8-E and one TU56-M Dual DECtape drive. The TD8-EH consists of a TD8-E and one TU56-MH Single DECtape drive.

The TD8-E is contained on a single quad Flip-Chip module which plugs directly into the OMNIBUS of the PDP-8/E. It is connected to the TU56 by a special interface cable (P.N. 7008447). It uses a standard TU56 with no modifications. The Read/Write Amplifiers (G888) must be plugged into the TU56 drives.

When reading, writing, or searching, the PDP-8/E acts as a controller for the DECtape. That is, all data transfers to and from the 8/E are through the AC in non-interrupt, non-data break mode. The PDP-8/E is completely committed to the tape operation and cannot perform any other functions until the tape operations have been completed.

Up to four TD8-E interfaces can be used with a PDP-8/E. Each TD8-E can drive either a single or dual transport. It is therefore possible to have eight DECtape drives connected to the PDP-8/E through four TD8-E's. When a dual transport is used on the TD8-E's, the first TD8-E will control units 0 and 1; the second TD8-E will control units 2 and 3; the third, units 4 and 5; and the fourth, units 6 and 7.

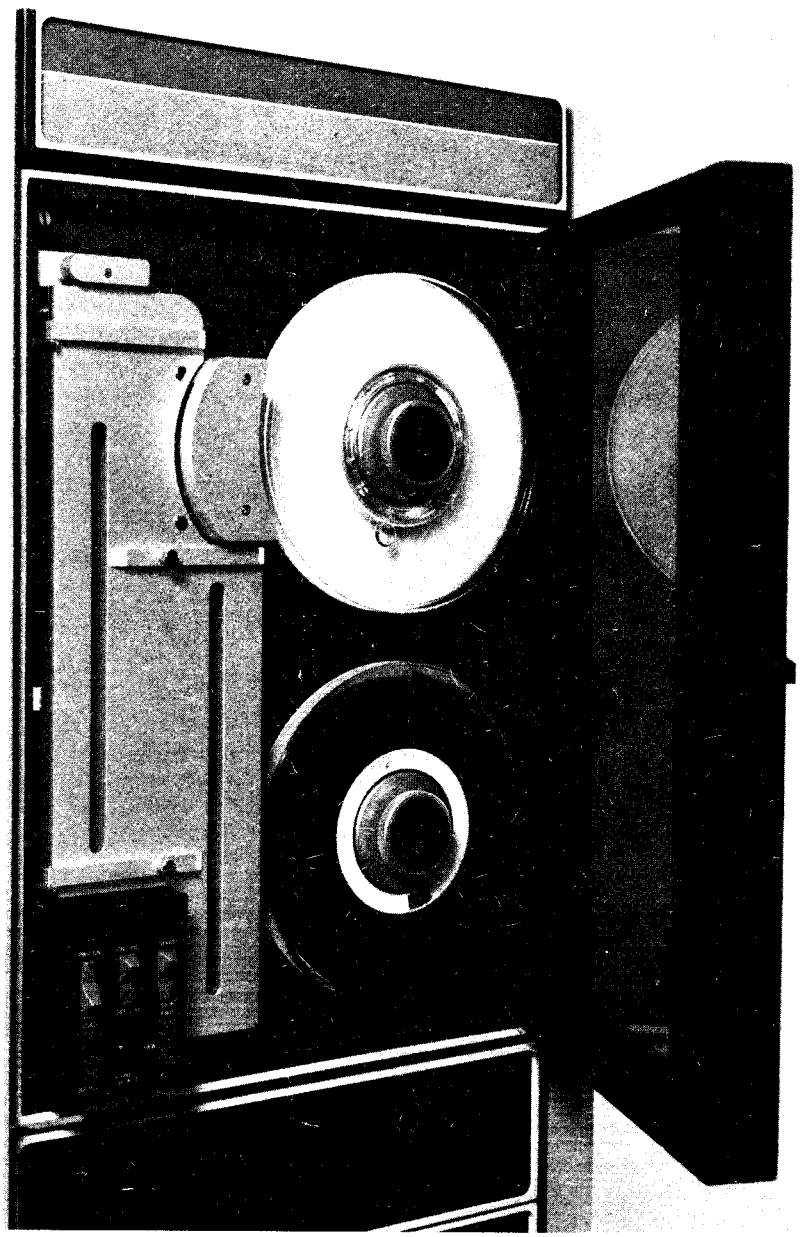
A comprehensive set of diagnostic routines is included with the TD8-E which checks all of its functions. The TD8-E is also supplied with subroutine software which search, read, and write PDP-8 compatible DECtapes. DECtapes written with the TC01 or TC08 control can be read with the TD8-E using this software and vice versa. Because of the close dependency of the hardware with the software, Digital Equipment Corporation will not guarantee operation of the TD8-E with any software other than that which is supplied by Digital Equipment Corporation.

The TD8-E was designed as a low-cost DECtape interface with limited functions. It is not a replacement for the TC08 which makes transfers of data direct to memory concurrent with CP operations. Its primary use is for library storage of programs and blocks of data. The TD8-E will, however, like the TC08, certify DECtapes by writing and verifying the mark and time tracks and block numbers.

Refer to Section 4 of this chapter for a detailed discussion of TU56.

**TU10 DECmagnetic Tapes**

The DECmagtape can interface directly with the OMNIBUS via the TM8-E, or to the EXTERNAL BUS via the TC58. The configurations of both categories are defined in the following table. For information on the TC58 controller, refer to section 4.



TU10 DECmagtape

**DECmagtape Configurations**

| SYSTEM OPTION | EQUIPMENT | NO. OF CHANNELS | DENSITIES (BPI) | TAPE SPEED (IPS) | OTHER INFORMATION |
|---|---|---|---|---|---|
| TM8-EA | TM8-E Control & TU10-EA(master) | 9 | 800 | 45 | Control plugs into OMNIBUS. TU10-EA contains a master and one slave. Up to 7 additional TU10 slaves may be added. 7 and 9 track TU10's can be mixed on the same system. For example, a 7 track master can be operated with a 9 track slave etc. The master consists of logic modules which plug into the TU10 electronics. |
| TM8-FA | TM8-E Control & TU10-FA(master) | 7 | 800/556/200 | 45 | Same as above. |
| TC58 * | TC58 Control(master) & TU10-EE(slave) | 9 | 800 | 45 | DW08A I/O conversion panel, KA8-E Positive I/O Bus and KD8-E Data Break Interface are prerequisites. The master is contained with the TC58 controller. Up to 7 additional TU10 slaves may be added. 7 and 9 track TU10's can be mixed on the same system. |
| TC58 * | TC58 Control(master) & TU10-FE(slave) | 7 | 800/556/200 | 45 | Same as above. |

* Refer to Section 4 for TC58 Description

## OMNIBUS DECmagtape Unit and Control Type TM8-E/F

**NOTE**

The following information is preliminary and is subject to change without notice. The reader should consult with the local DEC sales office.

The TM8E control provides the interface between the PDP-8/E and the TU10 master-slave magnetic tape transport system. The TU10 master can control 7 slaves; therefore the TM8-E is capable of controlling 8 transports.

The data transfer is via single cycle data break with a transfer rate of 36 KHZ. The transport operates at 45 ips and uses 7 channel formats at 200, 556 or 800 bpi or 9 channel format at 800 bpi.

The TM8-E contains six registers which are used to control the transports and report the status of the transports to the computer. The registers are loaded and read using IOT instructions which require no data break.

### PROGRAMMING

The following Instructions are used to program the TM8-E:

**Load Word Count Register (LWCR)**

Octal Code: 6701
Operation: Load Word Count Register and Clear the AC
AC → WC, 0 → AC

**Clear Word Count Register (CWCR)**

Octal Code: 6702
Operation: Clear Word Count Register

**Load Current Address Register (LCAR)**

Octal Code: 6703
Operation: Load Current Address Register and Clear the AC
AC → CA, 0 → AC

**Clear Current Address (CCAR)**

Octal Code: 6704
Operation: Clear Current Address

**Load Command Register (LCMR)**

Octal Code: 6705
Operation: Load Command Register and Clear the AC
AC → CM, 0 → AC

**Load Function Register (LFGR)**

Octal Code: 6706
Operation: Load Function Register (GO bit) and Clear AC
AC → Function Register 0 → AC

**Load Data Buffer Register (LDBR)**
Octal Code: 6707
Operation: Load Data Buffer Register and Clear AC
AC → DB, 0 → AC

**Read Word Count Register (RWCR)**

Octal Code: 6711
Operation: Clear AC and Read Word Count Register
0 → AC, WC → AC

**Clear Transport (CLT)**

Octal Code: 6712
Operation: Clear Transport

**Read Current Address Register (RCAR)**

Octal Code: 6713
Operation: Clear AC and Read Current Address Register
0 → AC, then CA → AC

**Read Main Status Register (RMSR)**

Octal Code: 6714
Operation: Clear AC and Read Main Status Register
0 → AC, then MS → AC

**Read Command Register (RCMR)**

Octal Code: 6715
Operation: Clear AC and Read Command Register
0 → AC, then CM → AC

**Read Function Register & Status (RFSR)**

Octal Code: 6716
Operation: Clear AC Read Function Register and Status 1
0 → AC, then Function and Status 1 → AC

**Read Data Buffer (RDBR)**

Octal Code: 6717
Operation: Clear AC and Read Data Buffer
0 → AC, then DB → AC

**Skip if Error Flag (SKEF)**

Octal Code: 6721
Operation: Skip if error flag is set.

**Skip if Control not Busy (SKCB)**

Octal Code: 6722
Operation: Skip if the control is not busy. The TM8-E becomes busy when a go is given to the transport and becomes not busy at MTTF.

**Skip When Job Done (SKJD)**

Octal Code: 6723
Operation: Skip if the job is done (MTTF is set). The job done flag (MTTF) sets at the end (LRCS) of a Read, Read/Compare, Write File Mark, or Write operation, and at the end of a record, if an EOT, EOF or BOT was encountered or the WC overflowed during a space operation.
MTTF sets when a transport begins to do a rewind and a new transport may be selected, when a transport goes off-line following an off-line operation, and when a rewinding transport has reached BOT and is ready.

**Skip When Tape Ready (SKTR)**

Octal Code: 6724
Operation: Skip if tape unit is ready (TUR is true).

**Clear Controller and Master (CLF)**

Octal Code: 6725
Operation: Clear the Controller and Transport Master if TUR, if not clear MTTF, EF and Status Registers.
0 → Control Registers

Octal Code: 6726
Reserved for Maintenance

Octal Code: 6727
Reserved for Maintenance

**Description of Registers**

6701 LWCR The 12 bit Word Count Register may be loaded from AC 0—11 any time the control is not busy. If the register is loaded during Control Busy, data reliability and tape compatibility cannot be assured. The Word Count must be loaded to the 2's complement of the number of words to be transferred or blocks to be spaced. The Word Count is incremented at TPI of the break cycle during Data Transfers and at LPCS during a space forward, and at the first word of a block during a Space Reverse.

Recommended block length is per USA Standards, Document USAS X3.22-1967. Recorded Magnetic Tape for information interchange (800 cpi, NRZ1).

6702 CWCR This IOT clears the Word Count Register and is essentially for maintenance use. It should not be used during Control Busy.

6703 LCAR The 12 bit Current Address Register may be *loaded from AC 0–11 any time the control is not* busy. It must be loaded to one less the Memory Address where the first data is taken or placed. If the Register is loaded during Control Busy, the following occurs:

1). In wrap around mode, function bit 6 = 0, location of the data transfer can not be assured within the selected memory field.

2). In EMA INC Enable mode, function bit 6 = 1, location of the data transfer can not be assured within the memory.

The Current Address Register is incremented at Break Request prior to the break cycle.

6704 CCAR — This IOT clears the Current Address Register and is essentially for maintenance use. It should not be used during Control Busy.

6705 LCMR — The Command Register can only be loaded from AC 0—11 during Control Not Busy. If the IOT is issued during Control Busy, an illegal function will be indicated and the current operation aborted. The transport may have to be rewound.

| Bits | |
|---|---|
| 0, 1, 2 | Unit selection: These determine which of the eight transports will be used. |
| 0 0 0 | Transport 0 |
| 0 0 1 | Transport 1 |
| 0 1 0 | Transport 2 |
| 0 1 1 | Transport 3 |
| 1 0 0 | Transport 4 |
| 1 0 1 | Transport 5 |
| 1 1 0 | Transport 6 |
| 1 1 1 | Transport 7 |
| Bit 3 | Parity: 0 = Even<br>1 = Odd |
| Bit 4 | Enable Interrupt on Error Flag |
| Bit 5 | Enable Interrupt on MTTF (job done flag) |
| Bits 6, 7, 8 | Extended Memory Address: These three bits determine which memory field the controller uses. The manner in which these bits are loaded depends upon the setting of the EMA Enable bit, Function Register bit 6. |

Bits

| 6 | 7 | 8 | |
|---|---|---|---|
| 0 | 0 | 0 | Field 0 |
| 0 | 0 | 1 | Field 1 |
| 0 | 1 | 0 | Field 2 |
| 0 | 1 | 1 | Field 3 |
| 1 | 0 | 0 | Field 4 |
| 1 | 0 | 1 | Field 5 |
| 1 | 1 | 0 | Field 6 |
| 1 | 1 | 1 | Field 7 |

Bit 9 — Reserved for Future Use

Bits 10, 11 — Density: These bits select the density for the transports operation.

| 10 | 11 | | |
|---|---|---|---|
| 0 | 0 | 200 bpi | 7 channel |
| 0 | 1 | 556 bpi | 7 channel |
| 1 | 0 | 800 bpi | 7 channel |

This also serves as a core dump mode. When issued to a 9 channel transport, data is written in 7 channel format and zero's are written in channels 0 and 1 on the tape.

| | | | |
|---|---|---|---|
| 1 | 1 | 800 bpi | 9 channel |

6706 LFGR — The function register must be the last register to be loaded, since this register contains the GO bit.

| Bit 0 | Bit 1 | Bit 2 | |
|---|---|---|---|
| 0 | 0 | 0 | Off Line: The selected transport is taken off-line and rewound to BOT. The MTTF is set when the transport responds to the function, the controller may then select and use another transport. The transport must be manually reset to the on-line state. The Word Count and Current Address Registers need not be loaded. |
| 0 | 0 | 1 | *Rewind: The transport rewinds at high* speed (150 ips) to BOT and stops. The MTTF is set when the transport responds to the function. The controller may then select and use another transport. Should the rewinding |

transport be reselected, another MTTF will occur when the tape has stopped at BOT. The word count and Current Address Registers need not be loaded.

| | | | |
|---|---|---|---|
| 0 | 1 | 0 | Read: Data may be transferred from the tape to memory in the forward direction only. All registers must be loaded. |
| 0 | 1 | 1 | Read/Compare: Tape data is compared to data in core memory. All registers must be loaded. If there is a comparison error, CA incrementation ceases, and the R/C error bit is set. Tape motion continues to the end of the record. The CA register contains the address of the word which failed. |
| 1 | 0 | 0 | Write: Data may be written on the tape in the forward direction only. All registers must be loaded. When the proper number of words have been written the transport writes the appropriate check characters to end the block. |
| 1 | 0 | 1 | Write End of File (File Mark): The transport writes the file mark which consists of a one word block. The CA and WC registers need not be loaded. |
| 1 | 1 | 0 | Space Forward: The transport moves forward at 45 ips the number of records specified by the WC register, or until a File Mark is read. If End of Tape is read space forward will stop at the first inter-record gap. The CA register need not be loaded. |
| 1 | 1 | 1 | Space Reverse: The transport moves in the reverse direction at 45 ips the number of blocks specified by the WC or until a file mark or BOT marker is read. The CA register need not be read. |

Bit 3 Extend Gap: This bit causes the transport to write with a minimum 3 inch gap between blocks.

Bit 4 Enable Check Characters: When this bit is set, it will allow the check characters to be read into the computer during a read function. When the word count overflows, this bit will allow at least one break during 7-track operation for the LPC or two breaks during 9-track operation for the CRC and LPCC. If a record length incorrect error occurs, the check character is considered bad and can not be used. This feature will be used primarily for 9-track error correction.

| | | |
|---|---|---|
| Bit 5 | | GO: This bit causes the controller to issue a GO command to the transport when the transport is capable of accepting it. The GO will not be issued if the specified function is illegal. |
| Bit 6 | | EMA INC Enable: If this bit is not set, the TM8-E will treat the extended memory the same way any other PDP-8 Family data break option would, i.e., each 4K block is used in a wrap around mode.<br><br>If this bit is set, the extended memory will be treated as a continuous memory rather than as 4K blocks. When the last location in a field is reached, the EMA bits are incremented and the transfer continues in the next field. I.e.: If a word is placed in field 2, location 7777, the following word will be placed in field 3, location 0000 if the EMA increment bit is set. If it is not, the word will be placed in field 2, location 0000.<br><br>In both modes of operation, the Current Address must be set to one less than the first location to be accessed. The 12 bit CA register and the 3 EMA bits are treated as one 15 bit register with the EMA bits most significant. I.e.: to access field 2, location 20, load EMA = 2, CA = 0017; to access field 2, location 0, load EMA = 1, CA = 7777 if in EMA increment mode; to access field 2, location 0, load EMA = 2, CA = 7777 if not in EMA increment mode.<br><br>If memory field 7 is selected, the EMA cannot increment, but will wrap around in field 7 and an EMA 7 increment error will occur. |
| 6707 | LDBR | Load Data Buffer Register and Clear the AC: This is primarily used for maintenance. |
| 6711 | RWCR | Clear the AC and Read The Word Count Register into the AC: This is primarily used for maintenance but also may be useful during Error Check routines. |
| 6712 | CLT | Clear Transport: This will clear the transport's master registers. |
| 6713 | RCAR | Clear the AC and Read Current Address Register: This is primarily used for maintenance but may also help during error check routines. |
| 6714 | RMSR | The 12 bit main status register is used to report the most important status of the transport and control to the computer. It may be read into AC 0–11 at any time. |

| Bit | |
|---|---|
| 0 | Error Flag: The Error Flag will interrupt the processor if the interrupt enable bit (CM04) is set. An illegal function or select error will set the Error flag immediately, halting data breaks and ending a Write operation. BOT, EOT, Read/Compare Error, Bad Tape, Lateral or Longitudinal parity errors, Record length incorrect, data late, or EMA 7 increment error will set the Error Flag after MTTF is set. |
| 1 | Rewind Status: The selected transport is rewinding. |
| 2 | Beginning of Tape (BOT): The BOT reflective strip is being sensed by the selected transport. |
| 3 | Select Remote: The selected transport is not on-line. |
| 4 | Parity Error: A longitudinal or lateral parity error has been detected. |
| 5 | File Mark (EOF): The selected transport detected a file mark during a space, read, or Read/Compare operation. |
| 6 | Record length incorrect: During a read or READ/Compare operation, the record length was different from the contents of the WC. The Word Count may be read to determine whether the record was long or short. |
| 7 | Data Request Late: The computer failed to service the break request before the next data transfer to or from the transport. |
| 8 | End of Tape (EOT): The EOT reflective strip has been sensed by the selected transport. |
| 9 | File Protect: The selected transport has a write lockout ring. No write functions will be accepted. |
| 10 | Read/Compare Error: A comparison failure occurred during the Read/Compare function. The CA contains the address of the bad word. |
| 11 | Illegal Function:<br>1. Issuance of LCMR, LFGR, or LDBR while the control is busy.<br>2. Specifying any density but 800 bpi for a 9-channel transport.<br>3. A space reverse function when the transport is at BOT. |

4. Read, Read/Compare or Space Forward after a Write or WEOF command.
5. Changing to transports which is not ready. (TUR is false)

| | | |
|---|---|---|
| 6716 | RFSR | Clears the AC and Read the Function and 2nd status register. |
| Bits 0-5 | | Function Register. |
| 6 | | Transport channel: The selected transport is 7-channel if the bit is 0, and 9-channel if it is 1. |
| 7 | | Bad Tape: Bad tape error indicates two or more consecutive characters missing, followed by data within the time of settling down. The CRC and LPCC will not cause bad tape errors. |
| 8 | | EMA 7 INC Error: This occurs if an attempt is made to increment the EMA from field 7 to field 0. The data will wrap around in field 7. |
| 9 | | Lateral Parity Error: A lateral parity error was detected. |
| 10 | | Reserved for Future Use. |
| 11 | | Longitudinal Parity Error: A longitudinal parity error was detected. |
| 6717 | RDBR | Clear the AC and Read data buffer into the AC. This is primarily used for maintenance. |

**TU10 MASTER**

The TU10 Master controls the function timing, write pulses, generation of all the check characters and checking of parity, and is capable of controlling 8 slaves on a common bus. The TU10 Master unit includes 1 TU10 slave.

**TU10 SLAVE**

The TU10 DECmagtape Transport is a solid-state, magnetic tape handling device that controls tape motion and reads or records digital information on magnetic tape in industry-compatible formats.

The TU10 uses vacuum columns and a servo-controlled single capstan to control tape motion. The only contact with the oxide surface is the magnetic head and a rolling contact on one low-friction, low-inertia bearing. Dancer arms and pinch rollers, which shorten tape life and can cause errors, are not used in the TU10.

Tape transport commands can be issued manually from the TU10 control panel or remotely from the processor by means of the Controller. Indicators on both the transport and the controller indicate transport status.

Each tape transport consists of the TU10 cabinet, reel and reel motor control, capstan drive, and read/write components. The circuitry which controls the motion of the transport, generates the write pulses, timing gaps, parity, and check characters, and checks the parity is located in the Controller. These logic circuits may be shared by up to 8 TU10's.

**SPECIFICATION**

**Power and Cabling**

| | |
|---|---|
| TU10 Power: | tape transport power (reel motors and fans) provided by internal power supply in each transport |

Cabling:

a) 2 BC08P-15 to connect TC58
   1 BC08N-15 to TU10
b) 3 BC08N-15 to Bus TU10's together
c) 2 BC08L-15 to connect TM8-E to TU10

**TU10 DECmagtape Transport**

| | |
|---|---|
| Mounting: | mounts in standard H960-CA cabinet |
| Size: | 26 inches high, 19 inches wide, 25 inches deep |
| Cooling: | internally mounted fans |
| Controls: | front panel mounted |

**Environmental Conditions**

| | |
|---|---|
| Temperature: | 40°F to 100°F for system<br>60°F to 80°F for magnetic tape |
| Humidity: | 20% to 95% (non-condensation) for system<br>40% to 60% (non-condensation) for tape |

**Power Input Requirements**

| | |
|---|---|
| TU10-EE, FE | 115 Vac, 60 Hz at 14A |
| TU10-EH, FH | 115 Vac, 50 Hz at 14A |
| TU10-EF, FF | 230 Vac, 60 Hz at 7A |
| TU10-EJ, FJ | 230 Vac, 50 Hz at 7A |

**Local Transport Controls**

| | |
|---|---|
| PWR ON/PWR OFF | power control switch |
| ON-LINE/OFF-LINE | local or programmed operation |
| START/STOP | tape motion control |
| LOAD/BR REL | releases brake for loading |
| UNIT SELECT | selects unit for program control |
| FWD/REW/REV | tape direction control |

**Tape Characteristics**

| | |
|---|---|
| Capacity: | 2400 feet of ½-inch, industry standard, 1-mil Mylar tape. |
| Reel Diameter: | 10-½ inch standard reels |
| Tape Handling: | direct-drive reel motors; servo-controlled single capstan; vacuum tape buffer chambers with constant tape winding tension |
| Tape Speed: | 45 inches per second, reading and writing |
| Rewind Speed: | 150 inches per second (approximately 3-minute rewind time for 2400-foot reel) |
| Packing Density: | **7-channel**—200, 556, and 800 BPI, selectable under program control |
| | **9-channel**—800 BPI |

**Data Recording and Transfer**

| | |
|---|---|
| Recording Mode: | NRZI, industry compatible |
| Magnetic Head: | Dual gap, read-after-write |
| Data Transfers: | Direct memory access (non-processor request) |
| Transfer Rate: | 36,000 characters per second, maximum |
| BOT, EOT Detection: | photoelectric sensing of reflective strip, industry compatible |
| Write Protection: | write protect ring sensing |
| Data Checking: | read-after-write parity checking; longitudinal redundancy check; cyclic redundancy check (9-channel only) |
| Interrecord Gap: | reads tape with gap of 0.48 inches or more; writes tape with gap of 0.52 inches or more (compatible with industry standard) |

**TU10 Models**

| No. of Channels | Type of Unit | 115 VAC 60 Hz | 115 VAC 50 Hz | 230 VAC 60 Hz | 230 VAC 50 Hz |
|---|---|---|---|---|---|
| 9-channel | Master | TU10-EA | TU10-EC | TU10-EB | TU10-ED |
| | Slave | TU10-EE | TU10-EH | TU10-EF | TU10-EJ |
| 7-channel | Master | TU10-FA | TU10-FC | TU10-FB | TU10-FD |
| | Slave | TU10-FE | TU10-FH | TU10-FF | TU10-FJ |

NOTE: DECmagtape units TU20 and TU30 are also compatible with the TM8-E and TC58 controllers.

## LABORATORY PERIPHERALS

### AD8-EA Analog-to-Digital Converter

The AD8-EA converter is a 10-bit successive-approximation type with sample and hold circuits, conversion circuits, an input buffer, and control logic contained on two PDP-8/E modules. The converter can be used singularly with one channel input having an input range from −5 to +5 volts or can be used with AM8-EA and AM8-EB Multiplexers to perform conversion for up to 16 channels having full-scale inputs from + 1 to − 1 volts. Analog inputs are connected to the module by H855 connectors from the multiplexer or by a shielded twisted pair from an external device.

Operation of the AD8-EA converter is controlled by IOT instructions. A conversion is initiated by an ADST instruction, or from the Real Time Clock DK8-EP. An input starts the conversion and clears the A/D Done Flag. When the conversion is complete, the converter sets its A/D Done Flag. This flag is sensed by an ADSK instruction. If it set, the next instruction is skipped so that the 10-bit digital word can be transferred to AC2-11 by an ADRB instruction. Since the 10-bit word is in two's complement form, AC00 and AC01 copy AC02 (sign-extended format). The converter contains an interrupt enable flip-flop that is controlled by program instructions. When enabled, this flip-flop permits the converter to generate interrupt requests to the program interrupt facility upon completion of conversion.

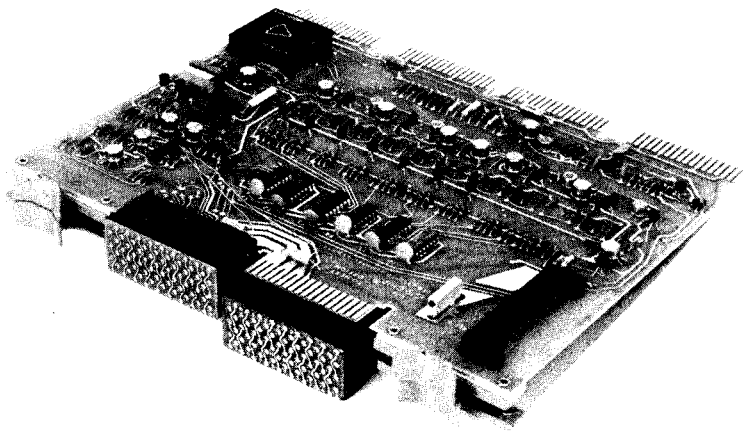
The converter also contains circuits for detection and sensing of a timing error. A timing error is defined as the receipt of a conversion request while a conversion is in progress. If this condition occurs, a Timing Error Flag is set. The Timing Error Flag is sensed by an ADSE instruction. An ADST or ADCL instruction clears this flag. This instruction also clears the A/D Done Flag so that another conversion can be implemented.

**Specifications**

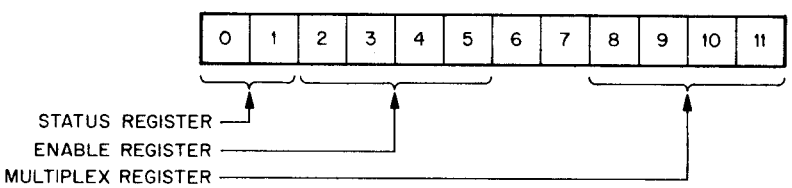
| | |
|---|---|
| Input Voltage Range: | −5.0 to +5.0 Volts |
| Input Impedance: | Signal<br>Return Input $\geq$ 10KΩ<br>Signal Input $>$ IMΩ |
| Output Format: | Parallel: 10 bits right-justified and sign extended, two's complement |
| Resolution: | ± ½ LSB at 20 degrees C greater |
| Conversion Rate: | than 50 kHz |
| Sample Acquisition Time: | Approx 3 μs |
| Aperture Time: | 200 ns |

## PROGRAMMING

The following instructions are used to program the operations involving the AD8-EA and AM8-E. Each instruction is completed in 1.2 μsec.



AD8-EA A/D Converter




| | |
|---|---|
| Status Register | 0—A/D Done Flag Status (Done = 1)<br>1—Timing Error Flag Status (Error = 1) |
| Enable Register | 2—Enable Interrupt on A/D Done = 1<br>3—Enable Interrupt on Timing Error = 1 (note 1)<br>4—Enable External (e.g. clock) A/D start<br>5—Auto-Increment Mode (note 2) |
| Multiplex Register | 8-11—Indicates current channel ($0 - 17_8$) to be sampled by A/D |

Note 1: The Timing Error Flag indicates that either an ADRB, and ADLM, ADST or external A/D start was attempted while a conversion was in progress. ADLM will be honored while an external A/D start or ADST will be ignored under this condition. ADLM or ADRB will cause an erroneous result to appear in A/D Buffer.

Note 2: When this bit is set, the occurrence of A/D Done = 1 will increment the Multiplex Register by 1. Incrementing past channel $17_8$ will cause the MUX register to reset to channel 0.

Eight instructions are used to program the A/D Converter and Multiplexer. Each instruction is completed in 1.2$\mu$s and is defined as follows:

**Clear All (ADCL)**

Octal Code: 6530
Operation: Clears the A/D Done Flag and Timing Error Flags to ready the converter for another conversion. This instruction also clears the MUX and Status Register.

**Load Multiplexer (ADLM)**

Octal Code: 6531
Operation: Load Multiplexer register from AC8-11 and Clear AC.

**Start Conversion (ADST)**

Octal Code: 6532
Operation: Clear A/D Done and Timing Error Flags and Start A/D Converter. Channel to be converted is determined by MUX register.

**Read A/D Buffer (ADRB)**

Octal Code: 6533
Operation: Clear A/D Done Flag and load the contents of the A/D Buffer into ACO-11.

**Skip On A/D Done (ADSK)**

Octal Code: 6534
Operation: Skip the next instruction if A/D Done = 1. Do not clear flag.

**Skip On Timing Error (ADSE)**

Octal Code: 6535
Operation: Skip the next instruction if Timing Error Flag = 1. Do not clear flag.

**Load Enable Register (ADLE)**

Octal Code: 6536
Operation: Load Enable Register from AC2-5 and clear AC Register.

**Read Status Register (ADRS)**

Octal Code: 6537
Operation: Read A/D Status, Enable Register, and MUX into ACO-11.

## PROGRAMMING EXAMPLES

**Normal Mode—**

The simplest method of programming the analog-to-digital converter is to have the program issue a start command, loop on the done flag until the conversion process is complete and the done flag is set to a "one", then the value of the converter's buffer is read into the PDP-8/E Accumulator. The program looks like this:

```
ADST        /Clear the ADC done flag and start conversion
ADSK        /Skip the next instruction when done
JMP .—1     /Jump back one instruction
ADRB        /Read ADC buffer into AC
```

If the Analog-to-Digital Converter had been enabled to accept start pulses from an external device, such as a clock, then a timing error could occur. To check for this the following code could be added after the ADST command:

```
•
•
•
ADSE        /Skip the next instruction on error
SKP         /unconditional skip
JMS ERROR   /Go to error routine
•
•
•
```

When the ADC is equipped with the multiplexer option, the channel to be sampled is selected prior to starting the conversion process. This is done using the ADLM command. For example a simple program to continuously "read" the value of one of the parameter knobs and display the digital value in the PDP-8/e accumulator look like this:

```
START,  CLA             /clear the PDP-8/E accumulator
        TAD CHN         /get the channel # (0-3 for knobs)
AGAIN,  ADLM            /load multiplexer from AC
        ADST            /start
        ADSK            /skip when finished
        JMP .-1         /
        ADRB            /Read ADC value
        JMP AGAIN       /repeat process
```

**Clock Mode—**

In this special mode, an external event, usually the clock overflow starts the conversion process. This mode sample is taken at regular intervals as defined by the clock rate. The following example takes $1000_{10}$ samples at the specified clock rate and stores them in memory.

```
        •
        •
        •
INITIALIZE CLOCK AND ADC ENABLE REGISTER
        •
        •
        •
START,  CLA
        TAD NUMBER
        DCA COUNTER
        TAD ADDRESS
        DCA POINTER     /POINTER IS AN AUTO-INDEX REGISTER

ADLOOP  ADSK
        JMP .-1
        ADRB
        DCA I POINTER
        ISZ COUNTER
        JMP ADLOOP
        •
        •
        •

NUMBER ,-1750₈          /# of samples (1000₁₀ in this case)
COUNTER , 0
ADDRESS , n-1           /Beginning of table
POINTER , 0
```

**Fast Sample Mode—**

In fast sample mode the PDP-8/E processor is allowed to proceed while the called for conversion is still in process. The conversion still requires its full time to complete but since the order of events has changed, the sample may be taken at the full speed of the Analog-to-Digital Converter. The following example demonstrates this:-

```
          •
ADLOOP ,  ADSK
          JMP .—1
ADSTART ,  ADRB
          ADST
          DCA I POINTER
          ISZ COUNTER
          JMP ADLOOP
```

To make use of this program it is necessary to enter the program at ADSTART.

**AM8-EA 8-Channel Analog Multiplexer**

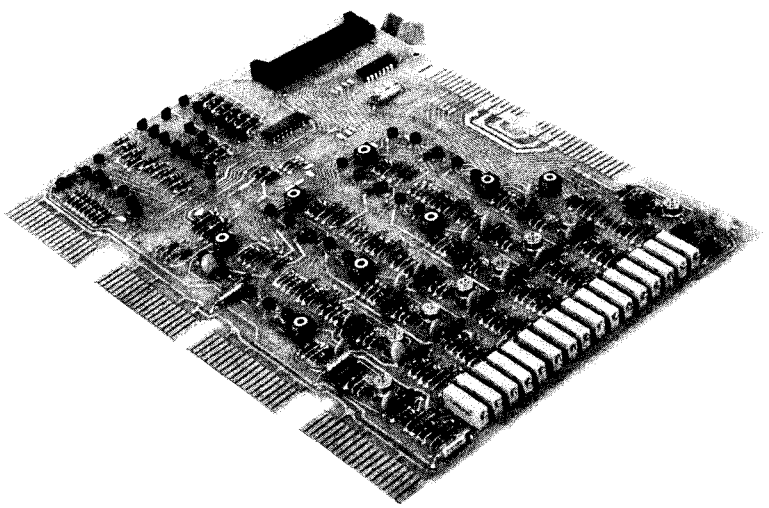
The AM8-EA is an 8-channel analog multiplexer designed for use with the AD8-EA A/D Converter. The multiplexer accepts bipolar analog input having a full-scale range of ±1v and converts these inputs into a full-scale ±5.0 volt output supplied to the AD8-EA Converter.

The AM8-EA consists of multiplexer switches and scaling amplifiers for 8 analog channels. The AD8-EA can be expanded to 16 channels in eight-channel groups by adding an AM8-EA 8-channel Multiplexer Module. Multiplexer operation is controlled by the AD8-EA IOT instructions. These instructions and the associated multiplexer control provide the capabilities for random or sequential selection of channels, combining the operation of the A/D converter with that of the multiplexer. Two programmable address modes are provided: autoincrement or non-autoincrement. The AM8-EA is set to nonautoincrement mode when INITIALIZE is generated.

In the autoincrement mode, channel addresses are incremented automatically at the completion of a conversion by an A/D Done Flag from the converter. The program specifies the first address of interest by issuing an ADLM instruction and then can issue an instruction to start an A/D conversion. Upon completion, the A/D Flag increments the multiplexer channel address for the next sample. This process can continue until the AUTO MODE flip-flop is reset.

**Specifications**

| | |
|---|---|
| Input Voltage | Bipolar, ±1V |
| Input Impedance | 70K ohms ± 2%, shunted by 300 pf |
| Output | Bipolar, ± 5V full scale |
| Common Mode Rejection | Greater than 25 dB, 35dB typical |



AM8-E 8-Channel Analog Multiplexer

| | |
|---|---|
| Overload Protection | ±67V from fault line (indefinitely) |
| Overload Recovery Time | 8 μs |
| Frequency Response | Flat from 0 to 30 KHz, —3dB 60 KHz |
| Leakage Current | Negligible at 70K ohms impedance |
| Long Term Stability (1 hour) | 1% for ± 30°C |

**DR8-EA 12-Channel Buffered Digital I/O**

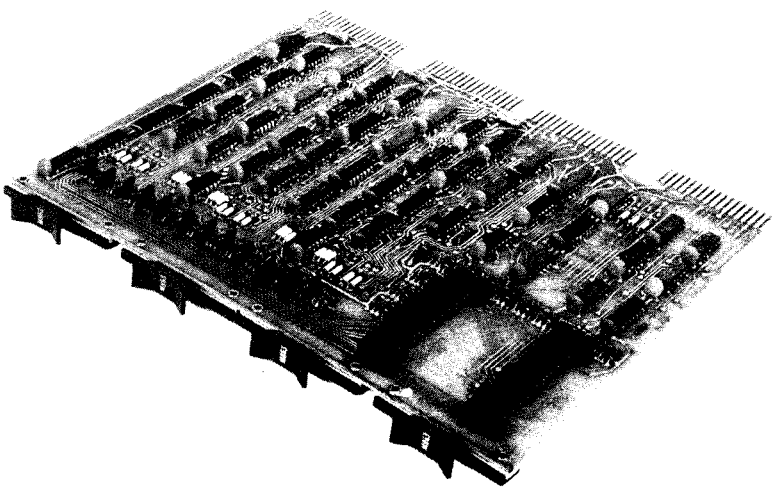
The DR8-EA Digital I/O can be used to control 12 discrete digital switching circuits located externally, and can be used to accept 12 discrete digital inputs from external sources. The unit consists of IOT control logic, a 12-bit input buffer, a 12-bit output buffer, and 3 multiplexer ICs that control the flow of data for input and output operations. All circuits are TTL logic and are mounted on a single PDP-8/E module which plugs into the OMNIBUS. The standard TTL outputs are connected to the external load via two H854 connectors on the module. Inputs from external sources are also connected to the DR8-EA using H854 connectors.

Data outputs are updated under program control. Standard output drivers have a TTL 30-unit load capability. For an output function the computer issues a DBRO, DBSO, or DBCO instruction. For DBSO instructions, only logical ones in the AC are loaded into the output register; AC bits containing logical ZEROS do not affect output register bits. For DBCO instructions, logical ONE's in AC result in logical ZEROS in corresponding bits of the output register. For DBRO instructions, the contents of the output register is transferred into the AC register.

Data inputs must be TTL compatible, have negative transition to .8V or less for a logical ONE, and have a pulse duration of greater than 50ns. Pulse rise and fall time should be less than 150ns for maximum noise immunity. In one mode of operation, the input register bits, once set by the data inputs, remain set until read by a DBRI instruction. In the second mode of operation, the input can be placed directly through gating on the bus, and will remain as long as the input remains. The DBRI instruction is also used to read the input data. When this IOT is issued, the content of the input register is gated to the AC via the OMNIBUS. A DBCI instruction, used with DBRI instruction, enables inputs that occurred too late to be read by the next DBRI instruction. Correct usage of this feature results in "zero dead time" for events. Any of the input lines can cause an interrupt if the proper jumpers are selected. The interrupt facility can be enabled by instruction DBEI and disabled by instruction DBDI.

A maximum of 8 DR8-EA options can be used. Each device selector code is determined by the user by means of jumpers. Device codes 50 to 57 are legal; however, the DR8-EA normally comes with device code 50 installed.

The DR8-EA is contained entirely on one PDP-8/E module.



DR8-EA 12 Channel Buffered Digital I/O

**Specifications**

| | |
|---|---|
| Input Format | Parallel, 12 bits. |
| Input Levels | Compatible TTL levels. Input circuitry switches at 0.8 to 2.4 Volts, and is protected to allow input swings as positive as +20 Volts and as negative as −15 Volts. |
| Input Connections and Pulse Width | Inputs to inverter buffers are normally held high by resistors. A negative transition of 0.8V or less will cause the input to become a logical ONE. Optional inputs bypass the flip-flop for direct interrogation of input line status. |
| Output Format | Parallel, 12 bits. |
| Output Levels | TTL-compatible levels capable of driving 30 unit loads.<br>Output lines are protected from short circuits to ground. |
| Environmental: | 0°C to 55°C<br>10% to 90% relative humidity (non-condensing) |
| Power Requirements: | +5.0 volts, 2.25 amps (worst case) |

**Programming**

The following instructions are used for DR8-EA operation. The X refers to a jumper selectable code. However, the DR8-EA normally comes with code 50 installed.

**Disable Interrupt (DBDI)**

Octal Code: 65X0
Operation: Disable all interrupts that are caused by a logical ONE on the input.

**Enable Interrupts (DBEI)**

Octal Code: 65X1
Operation: Set Interrupt Enable Flip-Flop. This tests the IN FLAG and causes an Interrupt Request if IN FLAG equals ONE.

**Skip on Flag (DBSK)**

Octal Code: 65X2
Operation: Tests the IN FLAG. If the Flag is a ONE, the next sequential memory location is skipped.

**Clear Selective Input Register (DBCI)**

Octal Code: 65X3
Operation: ONE's in the AC clear respective bits in the Input Register.

**Transfer Input to the AC(DBRI)**

Octal Code: 65X4
Operation: Transfers the complete 12-bit Input Register to the AC.

**Clear Selective Output Register (DBCO)**

Octal Code: 65X5
Operation: ONE's in the AC clear the respective bits in the Output Register.

**Set Selective Output Register (DBSO)**

Octal Code: 65X6
Operation: ONE's in the AC set the respective bits in the Output Register.

**Transfer Output to AC (DBRO)**

Octal Code: 65X7
Operation: Transfer the complete 12-bit Output Register to the AC.

**Programming examples**

To clear all registers

```
        CLA CMA   /Set AC to 7777
        DBCI      /set all input bits to zero
        DBCO      /set all output bits to zero
        DBDI      /disable interrupts
```

To service the occurrence of events

```
START,DBSK        /has event happened
        JMP-1     /no, check again
        DBRI      /yes, read register
        DBCI      /clear way for reoccurrence
        SPA       /was it event 0
        JMS SUB0  /yes, go service 0
        RAL       /no, shift left
        SPA       /was it event 1
        JMS SUB1  /yes, go service 1
        RAL       /no, shift left
        . . .
        RAL       /no, shift left
        SPA       /was it event 11
        JMS SUB11 /yes, go service 11
        JMP START /no, go wait for another event
        SUB0, 0   /return location
        DCA SAVE  /save for further checking
        . . .
        (Service event)
        . . .
        CLA
        TAD SAVE  /get for further checking
        JMP I S0  /go check further
S1,
        . . .
```

### Interface

The DR8-EA interfaces to the PDP-8/E OMNIBUS by plugging directly into the bus.

Interface to the outside world is by two (2) edge connectors on the M863 module. Signals leaving the board (12 bits parallel) are high (+3 volts) for a logical false and ground (0 volts) for a logical true. Each output line has approximately 20 milliamperes of drive (high level) and 20 milliamperes of sink (low level). Output levels remain fixed except when changed by the processor.

Signals entering from the "outside world" must be TTL in nature. The input represents approximately two (2) unit loads. When jumpered for "edge detection" a negative going edge (3 volts to 0 volts) is sensed. The signal must remain low (0 volts) for at least 50 NS. When sensing for an external level (jumpered so as to bypass the "flop") ground (0 volts) represents a logical true and a high (+3 volts) represents a logical false. With all bits jumpered this way the option represents a 12-bit parallel input register rather than an event detector.

An optional means of interfacing to the DR8-EA is available by using two (2) BC08J-X cables. Each cable (ribbon type) is terminated by a Berg type connector on one end (for interfacing to the DR8-EA module) and a standard DEC flip-chip on the other. One cable is used for the input and the other for output.

### Cable Descriptions

The 7008418 cable is used to jumper the input to the output for diagnostic purposes. It is part of the DR8-EA option. If the user desires interface cables, the following can be purchased:
The BC08J cable consisting of the 1210073-0 connector, cable and the M953 module, and is available in several standard lengths.

### Jumper Descriptions

The chart defined below will enable the user to change the IOT device code by changing the jumper across the specified split lug.

| device selector | | jumper | | |
|---|---|---|---|---|
| (normal conf) | 50 | 6H | 7H | 8H |
| | 51 | 6H | 7H | 8L |
| | 52 | 6H | 7L | 8H |
| | 53 | 6H | 7L | 8L |
| | 54 | 6L | 7H | 8H |
| | 55 | 6L | 7H | 8L |
| | 56 | 6L | 7L | 8H |
| | 57 | 6L | 7L | 8L |

*The normal configuration will be factory installed with device selector* code 50.

The input jumpers will be factory installed with A jumper, (edge triggered flip-flop). To change to level enables, use jumper B. The A,B, lugs are on all 12 bits.

Jumpers will also be provided to insulate the inputs from the interrupt and skip circuitry.

| J2 — Input | | J1 — Output | |
|---|---|---|---|
| D | — Bit 0 | D | — Bit 0 |
| F | — Bit 1 | F | — Bit 1 |
| J | — Bit 2 | J | — Bit 2 |
| L | — Bit 3 | L | — Bit 3 |
| N | — Bit 4 | N | — Bit 4 |
| R | — Bit 5 | R | — Bit 5 |
| T | — Bit 6 | T | — Bit 6 |
| V | — Bit 7 | V | — Bit 7 |
| X | — Bit 8 | X | — Bit 8 |
| Z | — Bit 9 | Z | — Bit 9 |
| BB | — Bit 10 | BB | — Bit 10 |
| DD | — Bit 11 | DP | — Bit 11 |

**Pin Connections**

The output and input pins corresponding the AC bit enabled on the DR8-EA are as follows:

**Input and Output End Pins (BC08J)**

| | |
|---|---|
| Bit 0 — B1 | Gnds A1, C1, F1, K1, |
| Bit 1 — D2 | N1, R1, T1, C2, |
| Bit 2 — D1 | F2, J2, L2, N2, |
| Bit 3 — E2 | R2, U2 |
| Bit 4 — E1 | |
| Bit 5 — H2 | |
| Bit 6 — H1 | |
| Bit 7 — K2 | |
| Bit 8 — J1 | |
| Bit 9 — M2 | |
| Bit 10 — L1 | |
| Bit 11 — P2 | |

## LABORATORY MOUNTING PANEL

The laboratory peripheral panel is designed for compact yet versatile packaging of modular accessory epuipment for laboratory environments. The panel is a 19-inch rack-mounted unit with H945 panel mounting frame and housing that accepts plug-in type modules or module panels. Modules can be single-width, double-width, or other multiples of single-width, and may contain a printed circuit card mounted on the vertical dimension. Controls and input/output connectors for peripheral equipment are mounted on the module front panel. Modules or module panels are attached to the panel frame using one fastener at the top and bottom of the module panel.

**The following options are available:**

H945 Housing (Rack Mountable Chassis) for mounting laboratory peripherals including space for mounting 11 panel units; 5 single panel units; 3 double panel units, and a single 1½ panel unit filler panels.

| | |
|---|---|
| H945-BA | 115V Table Top Version. |
| H945-BB | 230V Table Top Version. |
| H945-CA | 115V Rack Mount Version. |
| H945-CB | 230V Rack Mount Version. |
| DK8-EF | Optional panel for Real Time Clock type DK8-ES. Contains three 3-conductor phone jacks for event inputs and outputs; three one-turn potentiometers for voltage adjustments and three 4-pole double throw switches for line, or plus or minus voltage references. |
| AM8-EC | Analog input panel—16-channel A/D panel used for AM8-EA multiplexer inputs. Panel contains four 3-conductor phone jacks and four 10-turn vernier controls and 2 connectors. Panel repuires 3 single-panel-unit widths. |
| AM8-ED | Simple analog input panel 16-channel A/D panel used for AM8-EA multiplexer inputs. Panel contains two connectors and requires a single-panel-unit width. |
| VR03-A | Model 602 Tektronix Oscilloscope and VM03 Mounting Hardware. |
| VM03 | Model 602 Tektronix Oscilloscope Mounting Hardware. |

## DB8-E INTERPROCESSOR BUFFER

The DB8-E interprocessor buffer allows two PDP-8/E's to transfer data between themselves or it may be used single ended as a data path between a PDP-8/E and user designed logic.

Device codes are jumper selectable between 50 and 57 allowing up to 8 DB8-E's to be connected to one PDP-8/E. The PDP-8/E's may be interconnected at distances up to 100 feet apart by means of two (2) BC08-R type cables.

All logic is mounted on a single QUAD size board which plugs directly into the OMNIBUS. Two (2) 40 pin connectors type H854 mounted on the module receive cable type BC08-R or BC08-J. On the terminal end of the cable, connector type H856 is provided.

### SPECIFICATIONS

| | |
|---|---|
| Maximum Transfer Rate | One 12-bit word at a maximum rate of approximately 5K Hz. |
| Physical Characteristics | The entire option is contained on one 8½" PDP-8/E QUAD module. |
| Temperature Operating Range | 32°F to 131°F (0°C to 55°C) |
| Power Requirements | +5 volts at 600ma. |
| Data Format | 12 parallel bits in and 12 parallel bits out. |

### PROGRAMMING

The following instructions are used for the DB8-E operation:

**Skip on Receive Flag (DBRF)**
Octal Code: 65X1
Operation: Skip if the Receive Flag equals one.

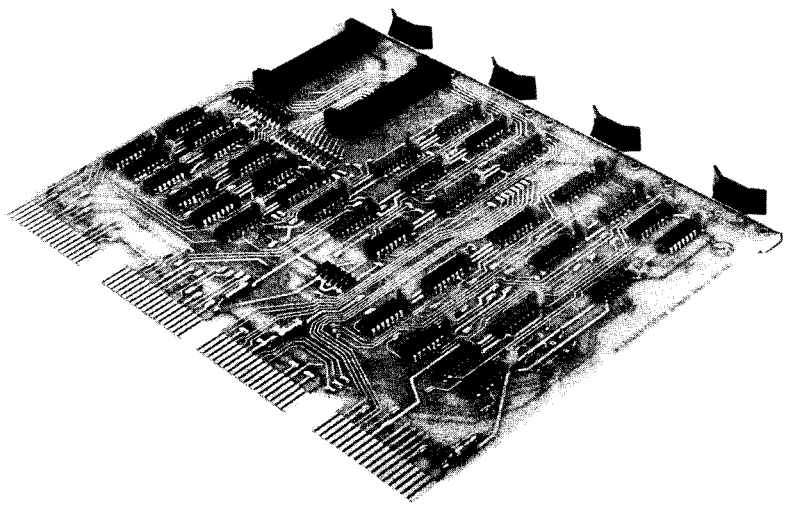
**Read Incoming Data (DBRD)**
Octal Code: 65X2
Operation: Read the Incoming Data into the AC and clear the Receive Flag.

**Skip on Transmit Flag (DBTF)**
Octal Code: 65X3
Operation: Skip if the Transmit Flag equals one.

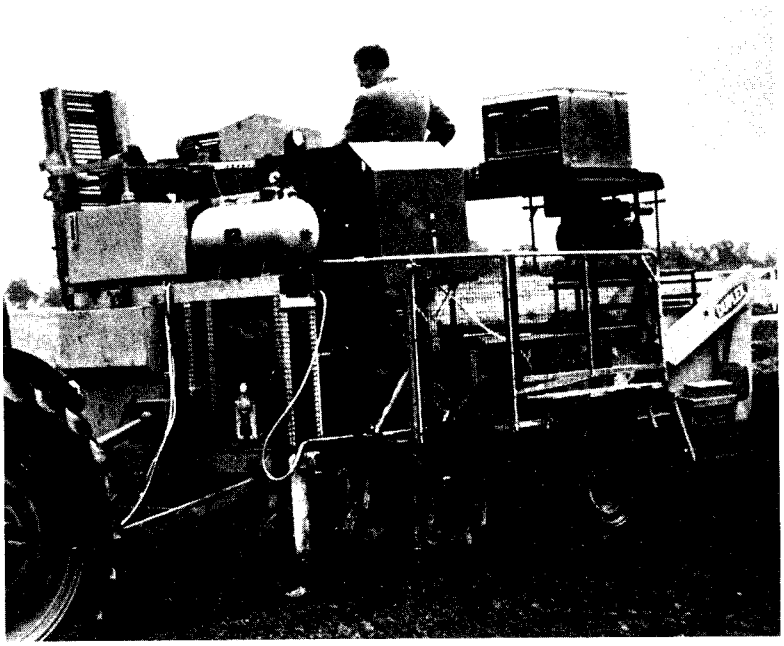
**Transmit Data (DBTD)**
Octal Code: 65X4
Operation: Transfer the contents of the AC Register to the Transmit Buffer. Transmit Data and set the Transmit Flag.

**Enable Interrupt (DBEI)**
Octal Code: 65X5
Operation: Enable the Interrupt Request Line.

**Disable Interrupt (DBDI)**
Octal Code: 65X6
Operation: Disable the Interrupt Request Line.



DB8-E interprocessor buffer



Instant evaluation of experimental farm machinery under test at the National Institute of Agricultural Engineering's Scottish Station near Edinburg, Scotland, is carried out by a PDP-8. The computer is mounted on a pre-production model of a potato picker (computer is in enclosure at technician's right). Picker is capable of rejecting all foreign matter from potato crop by X-ray techniques.

Besides the potato picker, the computer has been used to control various tractor-mounted farm equipment and a mechanical handling system. The PDP-8 gives the institute an instantly modifiable control and monitoring system, which may be connected without difficulty to any piece of equipment. When not controlling and evaluating farm equipment, it performs other functions.

## SECTION 4 EXTERNAL BUS INPUT/OUTPUT EQUIPMENT OPTIONS

The following equipment options are provided for the External Bus. Positive I/O Bus Interface (KA8-E) is a prerequisite for external I/O transfer and the Data Break Interface (KD8-E) is a prerequisite for any external data break peripheral. Refer to Chapter 10 for the External Bus Interface Discussion.

### EXTERNAL BUS INTERFACE CONTROL OPTIONS

The external bus interface options enable the PDP-8/E user to interface PDP-8/I and PDP-8/L type peripherals (such as mass storage devices, data acquisition, and control equipment) with the PDP-8/E. It also permits user-designed equipment to be interfaced with the 8/E external bus through the use of a general-purpose interface unit. A type KA8-E Positive I/O Bus Interface unit is required for any type of peripheral connected to the external bus. A type KD8-E Data Break Interface unit is required for each external peripheral that uses the data break facilities of the computer. These interface units and the BBO8-P General Purpose Interface are described below. The detailed relationships of programmed I/O transfers and data break transfers are described in Chapter 10.

#### KA8-E Positive I/O Bus Interface

The KA8-E option enables the PDP-8/E user to interface PDP-8/I and PDP-8/L type peripherals with a PDP-8/E. This option converts OMNIBUS signals into positive programmed I/O bus signals used by PDP-8/I and PDP-8/L type peripherals. For example, 8/I and 8/L type peripherals require IOP pulses to perform their operations. The OMNIBUS does not generate internal IOP pulses, but does provide signals (MD bits 9-11) that can be converted to IOP pulses. Other signals normally required for programmed I/O transfers are also available on the OMNIBUS. The KA8-E merely buffers these signals and makes them available to the external bus at the correct time. Similarly, the KA8-E buffers peripheral inputs and makes them available to the OMNIBUS. A detailed description of the external bus interface, including signals, levels, timing relationships, and other interface data, is provided in Chapter 10.

Only one KA8-E can be used per machine. This module is required both for programmed I/O transfers and for external bus data break transfers. The KA8-E is also required whenever the BB08-P General Purpose Interface option is used, and when user-designed or user-installed logic is to be connected to the external bus. The KA8-E Positive I/O Bus Interface is contained on one PDP-8/E module that plugs into the OMNIBUS.

See Chapter 10 for details of interfacing with the external bus.

#### BB08-P General Purpose Interface Unit

The BB08-P General-Purpose Bus Interface provides the PDP-8/E user with the capability of interfacing user-designed or user-installed logic with the PDP-8/E external bus. (The KA8-E Positive I/O Bus Interface module is a prerequisite for using the BB08-P.)

The BB08-P can interface one receive (input) and one transmit (output) device, or two receive, or two transmit devices, and control related

transfers from program instructions. In addition, the unit can supply operating power for the user's device.

The BB08-P logic is housed in one prewired DEC type H943 Mounting Panel with a self-contained Type H716 Power Supply. There are 34 module sockets not used by option modules; thus, these sockets are available for user logic modules. The spare sockets, located in two adjacent rows, can accommodate 34 single-height modules, or 17 double height modules or combinations.

The basic data format for transfers is 12-bit parallel. The organization of fields within this format is at the user's discretion; however, user logic must operate according to the following rules:

a. Data user logic to computer, via BB08, must take inverted positive-bus form:
   0V (L) = logic true (1);
   +3V (H) = logic false (0).
b. Data from computer to user logic, via BB08, must be accepted in true positive-bus form:
   +3V (H) = logic true (1);
   0V (L) = logic false (0).
c. User logic must provide pulses to the BB08 to set the Transmit and Receive flags as required. These pulses must take the form of 0V to +3V transitions of not less than 100 ns duration. Rise and fall times of these pulses should be 150 ns or less.

The user may, at his discretion, use any or all of the following spare logic gates on modules of the BB08 option:

a. Four C/D flip-flops on the M216 or M206 Module at panel location A06.
b. Two TTL logic inverters on the M111 Module at panel location A07.
c. Eight open-collector bus drivers on the M623 Module at panel location 805.
d. Eight TLL two-input NAND gates on the M113 Module at panel location B06.

The BB08-P receive section consists of 12 level-converter gates, a device selector, and Receive Flag circuits. For transfers to the computer, the user device sets the Receive Flag to initiate a program interrupt for servicing the device. The computer then interrogates the skip chain by issuing Skip-on-External-Flag instructions. When a skip instruction with 37 (octal) is detected by the BB08, this device returns a skip pulse that causes a conditional jump in the computer. The program then clears the Receive Flag by issuing an IOT 6372 (octal) and transfers the input word to the computer with a 6374 (octal) instruction.

The BB08-P transmit section consists of 12 level-converter gates, a device selector, and Transmit Flag circuits. The most important difference between transmit and receive logic is that transfer from the buffered accumulator bus to the user's device is enabled whenever the BB08 device selector decodes 636X (octal).

**Specifications**

| | |
|---|---|
| Data Format | 12-bit parallel. Can be discrete bits or any organization of fields. |
| Receive/Input | TTL compatible of the inverted positive bus form:<br>0V (L) = logic 1<br>+3V (H) = logic 0 |
| Transmit/Output | TTL compatible of the true positive bus form:<br>+3V (H) = logic 1<br>0V (L) = logic 0 |
| Power Supply Outputs (Available for User Logic) | 3A at +5V<br>1.3A at + 15V |
| Power | 115VAC, 60 Hz, 1A |

**Programming**
The following instructions are used for BB08-P operation:

**Skip On Transmit Flag (GTSF)**

Octal Code: 6361
Execution Time: 2.6 μs
Operation: Skips the next instruction if the Transmit Flag is set.

**Clear Transmit Flag (GCTF)**

Octal Code: 6362
Execution Time: 2.6 μs
Operation: Resets the Transmit Flag.

(User Designated)

Octal Code: 6364
Execution Time: 2.6 μs
Operation: This instruction is not used by BB08-P; however, the BB08-P decodes this IOT to make IOP4 available to user. User can use the IOP4 pulse to strobe data into his device.

**Skip On Receive Flag (GRSF)**

Octal Code: 6371
Execution Time: 2.6 μs
Operation: Skips the next instruction if Receive Flag is set.

**Clear Receive Flag (GCRF)**

Octal Code: 6372
Execution Time: 2.6 μs
Operation: Resets the Receive Flag.

**Read Device Buffer (GRDB)**

Octal Code: 6374
Execution Time: 2.6 $\mu$s
Operation: Transfers data from receive device to AC0-11.

**KD8-E Data Break Interface**

The KD8-E Data Break Interface option provides the PDP-8/E user with the one- and three-cycle data break facilities of the computer. Each KD8-E implements one of the 12 available data break channels of the PDP-8/E.

Each KD8-E contains the hardware to implement one standard data break channel and logic for establishing multiplexing priority between break devices. The KD8-E option is contained on one PDP-8/E module that plugs into the OMNIBUS.

Data break operations and the relationships of the KD8-E for these operations are described in detail in Chapter 10. Transfer time is 1.4 microseconds (715 kHz) for the single-cycle data break devices and 4.2 microseconds for 3-cycle data break devices.

## RANDOM ACCESS DISK DEVICES

### RK8 Disk System

The RK8 Disk System provides the PDP-8/E user with a modular, random-access, mass-storage device that utilizes removable disk cartridges as a storage medium. A basic system consists of one RK01 Disk Drive and Control and one RK08-P Disk Interface Control housed in a DEC H950 cabinet with self-contained power supplies, control, and indicator panel. The basic system provides the capability of storing 831,488 12-bit words and is readily expandable to over 3.3 million words in increments of 831,488 words. The RK08-P controls up to four RK01 units; thus, the expansion requires the addition of up to three RK01s.

Complete write protection is provided either on a sector basis, under manual/program control, or on whole disk basis, under manual control. This feature allows the programmer complete flexibility. Sectors of the disk containing system programs can be write-protected, while other sectors, containing data or new programs under development, can be write-permitted.

Sector numbers can be sequentially located on the disk, or scattered throughout a track. This feature allows for maximum throughput. Staggering of sector numbers throughout the track allows for computation time between data block transfers and enables the most efficient use of the system.

Complete transfer rate optimization is available. Consecutive data blocks can be transferred every 5 ms without specifying continuation. This feature eliminates the need to wait one disk revolution between blocks. A complete 4K of data can be transferred in just 80 ms.

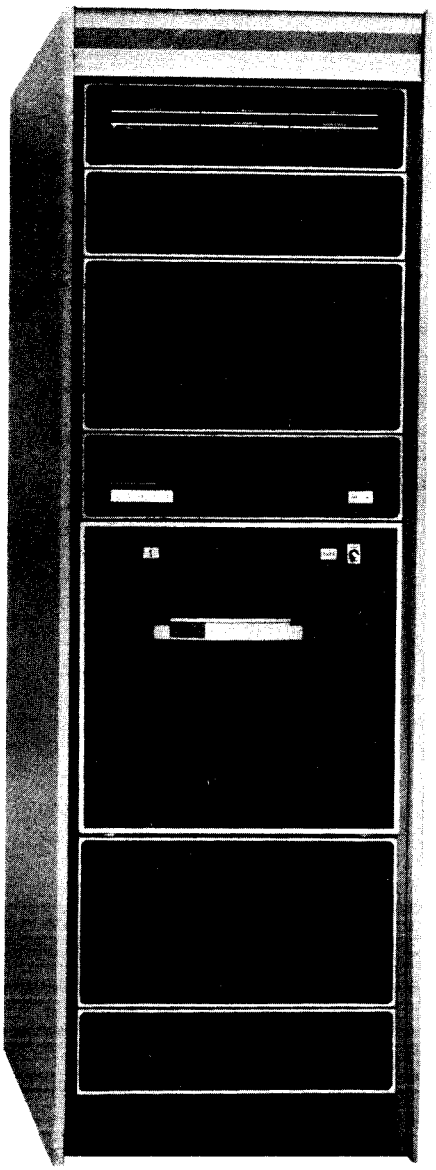
Complete track verification is performed with a preformatted cartridge. A separate leader containing track, surface, and sector address is written and verified by the format program, and checked on each transfer. This feature ensures positive track identification before a transfer is enabled.

Complete self-checking maintenance features are built in. These features permit fast and easy diagnosis of any errors.

Data transfers are performed using the single-cycle data break facilities of the PDP-8/E; thus, the KA8-E External Bus Interface and KD8-E Data Break Interface are prerequisites for using the RK8 on the PDP-8/E external bus.

#### Specifications

| | |
|---|---|
| Disk Capacity: | |
| Storage Capacity: | Each RK01 Disk Cartridge stores 831,488 (includes three spare tracks) 12-bit words. |
| Expansion: | Four RK01 drives can be controlled by one RK08 control for a total of 3,325,952 words. |
| Data Tracks: | 200 (plus three tracks) |
| Words per Track: | 4096 (2048 words on 0 and 1 surfaces) |
| Sectors: | 16 |



RK8 Disk System

| | |
|---|---|
| Words per Sector: | 256 |
| Minimum Block Size: | 256 |
| Maximum Block Size: | 4096 |

Read/Write Heads
Type = Tunnel erase
Number = Two (one per disk surface)

Recording Parameters

| | |
|---|---|
| Recording Method: | Double Frequency—Time plus data |
| Density: | 704 bits/inch (outer track) to 1026 bits/inch (inner track) |
| Speed: | 1500 + or − 30 rpm |
| Transfer Path: | Single cycle Data Break |
| Transfer Rate: | 16.7 μs per word |
| Minimum Access Time: | 2 ms step plus 37 ms settle time (Adjacent Tracks) |
| Average Access: | 134 ms (includes settle time) |
| Maximum Access: | 441 ms (includes settle time) |
| Latency Maximum: | 40 ms (one revolution) |
| Latency Average: | 20 ms (½ revolution) |
| Program Interrupt: | Transfer Done Flag<br>Track Found Flag (Enabled Separately)<br>Error Flag (Enabled Separately) |
| Write Lock: | The two words at the beginning of each track contain the status information that is automatically checked for write lock of sectors. |

**RK01 Disk Drive and Control**
The RK01 Disk Drive and Control contains the drive electronics and mechanism for accepting and releasing the disk, positioning the read/write heads, and controlling reading and writing of data from RK08-P commands.

The recording medium is a removable disk cartridge mounted in a protective case. The disk is an aluminum platter coated on both sides with magnetic oxide. When the cartridge is inserted into the drive mechanism, a read/write access door is automatically opened to permit positioning of the read/write heads over the disk surfaces. The disk is retained on its drive spindle by a magnet, and is driven counterclockwise at a uniform rate of 1500 rpm by a hysteresis synchronous drive motor. Information is recorded on or retrieved from both surfaces of the disk by the upper and lower read/write heads. These heads are cushioned from the disk surface by a film of forced air which keeps them between 125 and 160 microinches from the disk surface.

The upper surface of a disk mounted on the drive spindle is normally designated surface 0; the lower surface 1. Each disk surface is divided into 203 tracks (200 data tracks and 3 spares), with track 000 on the outer periphery and track 202 on the innermost portion of the recording area. Thus, for 203 combinations, eight bits must be allotted to address a track. The interval required for moving the read/write heads from one track to an adjacent track is approximately 2 ms; this means that, for a

move between the two possible extremes (track 000 and track 203), approximately 443 ms (including settling time) is required.

Each track is divided into 16 sectors with sectors 0 (octal) through 7 (octal) on the upper or 0 surface and sectors 10 (octal) through 17 (octal) on the lower or 1 surface. Sector assignments can be staggered as desired for the most efficient operation. Four bits (three for sector and one for surface) must be allotted for selection of a sector. A sector provides storage capabilities for two 12-bit header words, 256 12-bit data words and a 12-bit parity word. The first header word defines the track and sector address and the second word stores sector protect and status bits. The 12-bit parity word defines the longitudinal parity of the data words.

Information is recorded on the disk using the double-frequency or self-clocking method, in which a composite signal (generated from clock and data signals) is supplied to the read/write electronics. The clock frequency (720 kHz) determines the basic recording rate and cell width. For the recording of a logical zero, only the clock frequency is present in the composite signal and the results in a single change of direction in the magnetic flux pattern. However, for the recording of a logical one, a data pulse, occurring at twice the clock rate, is combined with the clock signal. This composite signal produces two changes in direction of the flux pattern. Thus, a component of the clock frequency is always present for timing purposes.

**RK08-P Disk Interface Control**

The RK08-P interfaces up to four RK01 Disk Drive and Control units with the external bus of the PDP-8/E. As part of this function, the RP08-P:

a. Decodes programmed IOT instructions.
b. Accepts and stores word count, current address, and command and address words.
c. Selects the program-designated RK01 and starts the program-designated operation.
d. Jointly (with the selected RK01) locates the disk address (track sector and surface).
e. Generates interrupt and break requests to initiate a single-cycle data break.
f. Buffers the input/output data and performs related conversion (serial-to-parallel and parallel-to-serial).
g. Performs housekeeping chores for single-cycle data break transfers (incrementing of word count and current address and providing address for transfer).
h. Generates and checks longitudinal parity for the sectors.
i. Provides flags for denoting current conditions and error status.
j. Provides logic for aiding in maintenance of an RK8 system.

Data transfers between the disk and core memory are implemented using the single-cycle data break facilities of the computer. (Refer to Chapter 10 for a detailed description of single-cycle data break.) For this operation, the computer specifies the number of words to be transferred (word count), and loads this information into the RK08-P word count

register by issuing a DLWC instruction. The first core memory address involved in the transfer is then loaded into the current address register by issuing a DLCA instruction. Next the computer loads a command word defining the selected disk, extended memory address (if this option is used), the interrupts it will accept, and the type of operation to be performed. This information is loaded into the command register of the RK08 by a DLDC instruction. Next the program loads the disk address (track, sector, and surface address) into corresponding registers in the RK08. This information defines disk starting location. If a read operation is to be performed, a DLDR instruction is issued to load the disk address and start the operation. Similarly, for a write operation, a DLDW instruction is issued. When the correct data track is located, a data break request is generated and the data break interface logic assumes control of the transfers. For this phase, the data break logic controls the loading and conversion of disk data words by asserting a B BREAK line to the RK08-P. Information read from the disk is converted from serial form for parallel transfer to the core memory.

This information is routed via external bus lines DATA00-11, gated by the Data Break Interface, and supplied to the MB via OMNIBUS lines DATA0-11. For write operations, information is accessed at the memory location specified by the current address. Data is provided to the RK08-P via the MD00-11 OMNIBUS lines and the Positive I/O Bus Interface (where it is buffered), and supplied to the RK08-P via the BMB00-11 external bus lines. The data is loaded into an RK08-P buffer under data break control and is shifted out to the disk read/write electronics. For each word transfer, the core memory address is specified by the current address register, and then the current address and word count registers are incremented. When the proper number of words have been transferred, as denoted by word count overflow, the RK08 generates an interrupt request. When the computer honors this request, it senses the transfer done flag of the RK08 with a DSKD instruction. If this flag is set, the computer senses the peripheral error flag with a DSKE instruction to determine if any errors were recorded during the transfers. If not, the transfer is assumed to be valid.

**Programming**

The following instructions are associated with the RK08-P control and the RK01 disk drive and control:

**Load Disk Address (DLDA)—(Maintenance Only)**

| | |
|---|---|
| Octal Code: | 6731 |
| Execution Time: | 2.6 $\mu$s |
| Operation: | Loads the Disk address for maintenance or diagnostic functions. |

**Load Command Register (DLDC)**

| | |
|---|---|
| *Octal Code:* | *6732* |
| Execution Time: | 2.6 $\mu$s |
| Operation: | Loads the contents of AC0-11 into the Command Register and clears AC. The Command Register bit usage is shown in Figure 7-6. |

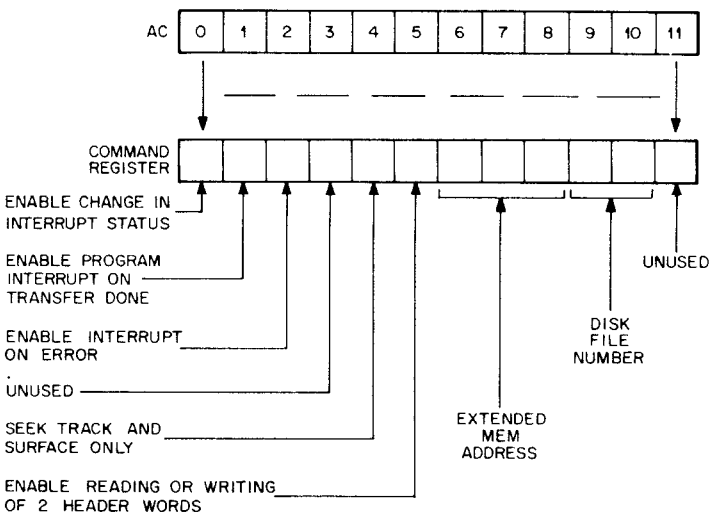



Figure 7-6 Command Word

**Load Disk Address and Read (DLDR)**

Octal Code: 6733
Execution Time: 3.6 $\mu$s
Operation: Loads track, surface, and sector address from AC, then clears AC. Starts read from disk if Command Register bit 4 is zero. If bit 4 is a one, instruction is executed only to seek track and surface. The relationship of bits in the AC transfer is shown in Figure 7-7.

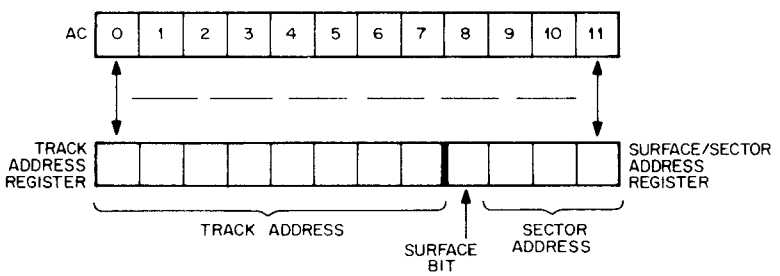



Figure 7-7 Address Word (Read)

**Read Disk Address (DRDA)**

Octal Code: 6734
Execution Time: 2.6 $\mu$s
Operation: Clears AC and reads content of Track Address Counter and Surface/Sector counters into AC0-11.

**Load Disk Address and Write (DLDW)**

Octal Code: 6735
Execution Time: 3.6 $\mu$s
Operation: Loads track, surface, and sector address from AC, then clears AC. Also starts a write operation if Command Register bit 4 is zero. If bit 4 is a one, instruction is executed only to seek track and surface.

**Read Disk Command Register (DRDC)**

Octal Code: 6736
Execution Time: 3.6 $\mu$s
Operation: Clears AC, then reads content of Command Register to AC0-11.

**Load Disk Address and Check Parity (DCHP)**

Octal Code: 6737
Execution Time: 4.6 $\mu$s
Operation: Loads track, surface, and sector address from AC, then clears AC. If bit 4 of Command Register is zero, reads data at specified address and checks parity. If bit 4 is one, instruction is executed to seek track and surface.

**Read Disk Status Register (DRDS)**

Octal Code: 6741
Execution Time: 2.6 $\mu$s
Operation: Clears AC, then reads content of Status Register into AC. Status bits are defined in Figure 7-8.

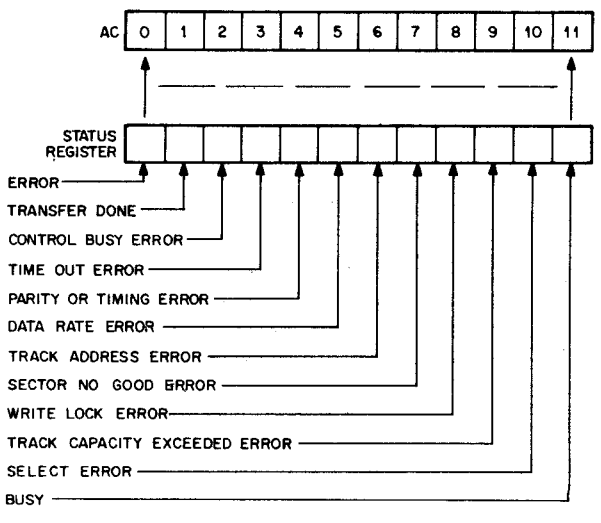



Figure 7-8 Status Word

**Clear Status Register (DCLS)**

Octal Code: 6742
Execution Time: 2.6 $\mu$s
Operation: Clears Status Register.

**Load Maintenance Register (DMNT)**

Octal Code: 6743
Execution Time: 3.6 $\mu$s
Operation: Loads the content of AC into Maintenance Register and performs specified operation. Bits remain in Maintenance Register until DMNT is issued with AC bits = 0, Maintenance functions are defined in Figure 7-9.

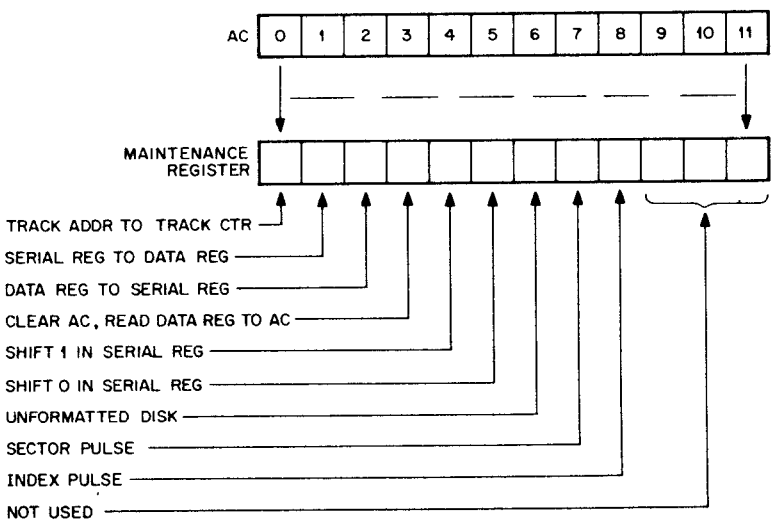



Figure 7-9 Maintenance Word

**Skip on Disk Done (DSKD)**

Octal Code: 6745
Execution Time: 3.6 $\mu$s
Operation: The Disk Transfer Done Flag is sensed; if it is set, the next instruction is skipped.

**Skip on Disk Error (DSKE)**

Octal Code: 6747
Execution Time: 4.6 $\mu$s
Operation: The Error Flag is sensed; if it is set, the next instruction is skipped.

**Clear All (DCLA)**

Octal Code: 6751
Execution Time: 2.6 $\mu$s
Operation: Clears selected disk to track 000, and clears all control registers and flags except Disk Selection. Transfer Done is set when disk is positioned to track 000.

**Read Word Count Register (DRWC)**

Octal Code: 6752
Execution Time: 2.6 $\mu$s
Operation: Clears the AC, then reads contents of WC register to AC0-11.

**Load Word Count Register (DLWC)**

Octal Code: 6753
Execution Time: 3.6 $\mu$s
Operation: Loads the contents of AC into WC register, then clears AC.

**Load Current Address Register (DLCA)**

Octal Code: 6755
Execution Time: 3.6 $\mu$s
Operation: Loads the contents of AC into CA register, then clears AC.

**Read Current Address Register (DRCA)**

Octal Code: 6757
Execution Time: 4.6 $\mu$s
Operation: Clears the AC, then reads contents of the CA register to AC0-11.

**Example Subroutine**

```
DISKIO,  0              /SUBROUTINE ENTRY POINT
         TAD CNT        /FETCH # OF WORDS TO BE READ
         DLWC           /LOAD WORD COUNT REGISTER
         TAD CUR        /FETCH ADD OF MEMORY BUFFER
         DLCA           /LOAD CUR ADDR REGISTER
         TAD 0000       /PUT COMMAND IN ACCUMULATOR
         DLDC           /LOAD COMMAND REGISTER
         TAD ADR        /FETCH TRACK, SURFACE, & SECTOR
         DLDR           /LOAD DISK ADR AND READ DATA
                        /DLDW WOULD HAVE WRITTEN
         DSKD           /DONE WITH TRANSFER?
         JMP.—1         /NO—GO BACK 1
         DSKE           /YES—IS THERE AN ERROR?
         JMP I DISKIO   /NO ERROR—RETURN
         JMP ERR        /GO TO ERROR SUBROUTINE
CNT,     XXX            /# WORDS TO BE READ
CUR,     YYY            /BEG ADDR OF MEMORY BUFFER
ADR,     ZZZ            /DISK ADDRESS
```

**DF32-D DEC Disk File & Control & DS32-D DEC Disk File Expander**
The DF32-D Disk File is a fast, low-cost, random-access, bulk-storage device and control for use with the PDP-8/E computer. [When the DF32-D is used with the PDP-8/E, the KD8-E Data Break interface and the KA8-E Positive I/O Bus interface are also required.] Operating through the three-cycle Data Break Facility, the DF32-D provides 32,768 13-bit words (12 bits plus parity) of storage, and is economically expandable to 131,072 words when using the DS32-D Expander Disk.

Transfer rate of the DF32-D is 32 or 64 $\mu$s per word (optional when timing track is written); average access time is 16.67 ms for 60 Hz power (20 ms with 50 Hz power).

Two basic assemblies make up the DF32-D; the storage unit with read/write electronics and computer interface logic. The storage unit contains a nickel-cobalt-plated disk, driven by a hysteresis synchronous motor. Data is recorded on a single disk surface by 16 fixed-position read/write heads.

Disk motor and shaft, read/write data heads, and timing and address heads are mounted on a 19-inch relay rack assembly, which permits easy access to the unit by sliding the unit in and out of a standard Digital Equipment Corporation cabinet.

The DS32-D Extender Disk File is also a slide-mounted assembly with a storage element and read/write electronics. Information transfers are made via the DF32-D logic, and are controlled by the DF32-D.

**Specifications**

| | | |
|---|---|---|
| Storage Capacity | 32,768 13-bit words; expandble to 131,072 words in increments of 32,768 words, using DS32-D. | |
| Data transfer rate | 60 Hz power | 50 Hz power |
| | 32 (64) $\mu$s per word | 39 (78) $\mu$s per word |
| Average access time | 16.67 ms | 20.0 ms |
| Write lock switches | Inhibit writing on lower and/or upper 16K or any 32K disk surface; may be used to inhibit one or more 32K disks in an expanded configuration. | |
| Addressing Scheme | Random or absolute addressing from 0 to 32K words with variable block sizes from 1 word to 4096 words. | |
| Data assembly | Read/write on disk is serial, with external transfer parallel by word. | |
| Data Availability | 16 $\mu$s (48 $\mu$s with alternate timing track) from the time word is assembled until new word starts to shift into assembly register. (A similar timing condition exists during the write operation.) | |
| Data tracks | 16 per disk, 2048 words per track | |
| Recording method | NRZI | |
| Density (max) | 1100 · BPI | |
| Timing tracks | 2 plus 2 spare | |

| | | |
|---|---|---|
| Size | 10-½ in. high and 23-⅝ in. deep in a standard 10-in. rack. | |
| Heat Dissipation | 1700 Btu/hr. | |
| Data Transfer Path | 3-cycle Break | Address Locations<br>7750 Word Count<br>7751 Memory Address |
| Program Interrupt | Data Transfer-completion flag and/or non-existent disk. | |
| Write lock Switches | Inhibit write only on lower or upper 16K or both on one or more discs. | |
| Select Switches | Rotary Switches to select disk unit number. | |

**Programming**
The following instructions operate the disk system:

**Clear Disk Memory Address Register (DCMA)**

| | |
|---|---|
| Octal Code: | 6601 |
| Execution Time: | 2.6 μs |
| Operation: | Clears disk memory address register, parity error, and completion flags. This instruction also clears the disk memory request flag and interrupt flags. |

**Load Disk Memory Address Register and Read (DMAR)**

| | |
|---|---|
| Octal Code: | 6603 |
| Execution Time: | 3.6 μs |
| Operation: | Loads the content of the AC into the disk memory address register an clears the AC. This IOT initiates readings of information from the disk into the specified core location. Clears parity error and completion flags. |

**Load Disk Memory Address Register and Write (DMAW)**

| | |
|---|---|
| Octal Code: | 6605 |
| Execution Time: | 3.6 μs |
| Operation: | Loads the content of the AC into the disk memory address register and clears the AC. This disk then begins to write information into the disk from the specified core location. Clears parity error and completion flags. Data break must be allowed to occur within 33 μs (66 μs) after issuing this instruction |

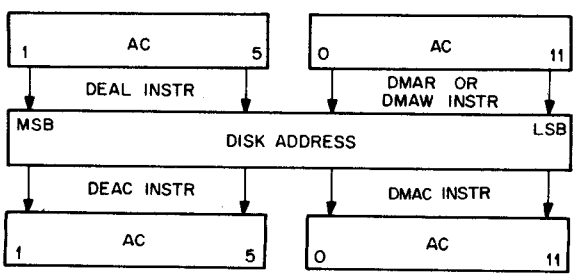


Figure 7-10 Address Words

**Clear Disk Extended Address Register (DCEA)**

Octal Code: 6611
Execution Time: 2.6 $\mu$s
Operation: Clears the disk extended address and memory address extension register.

**Skip on Address Confirmed Flag (DSAC)**

Octal Code: 6612
Execution Time: 2.6 $\mu$s
Operation: Skips next instruction if address confirmed flag is a one. Flag is set for 16 $\mu$s whenever the address on the disk equals the contents of the disk address registers. Clears the AC.

**Load Disk Extended Address (DEAL)**

Octal Code: 6615
Execution Time: 3.6 $\mu$s
Operation: Clears the disk extended address and memory address extension registers and loads them with the track address data held in the AC. ORs the contents of these registers, plus the photocell mark and three error flags, into the AC. (See DEAC instruction.)

**Read Disk Extended Address Register (DEAC)**

Octal Code: 6616
Execution Time: 3.6 $\mu$s
Operation: Clears the AC, then loads the contents of the disk extended address register into the AC to allow program evaluation. Skips the next instruction if address confirmed flag is a one.

**NOTE**

Write lock switch status is true only when disk unit contains a write command. The nonexistent disk condition will appear following the completion of a data transfer during read, where the address acknowledged was the last address of a disk and the next word to be addressed falls within a nonexistent disk. The completion flag for this data transfer is set by the nonexistent disk condition 16 $\mu$s after the data transfer.

**Skip On Zero Error Flag (DFSE)**

Octal Code: 6621
Execution Time: 2.6 $\mu$s
Operation: Skips the next instruction if parity error, data request late, and write lock switch flag are all zero. Indicates no errors.

**Skip on Data Completion Flag (DFSC)**

Octal Code: 6622
Execution Time: 2.6 $\mu$s
Operation: Skips the next instruction if the completion flag is a one, indicating data transfer is complete.

**Read Disk Memory Address Register (DMAC)**

Octal Code: 6626
Execution Time: 3.6 $\mu$s
Operation: Clears the AC, then loads the contents of the disk memory address dress register into the AC to allow program evaluation. During read, the final address will be the last one transferred.

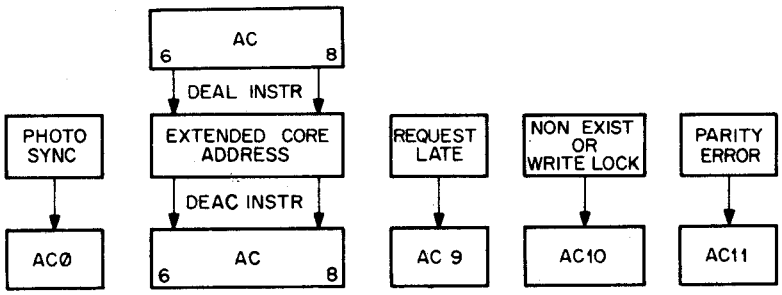



Figure 7-11

Three-cycle data break locations: Work Count address is 7750 (field 0). Current Address is 7751 (field 0).

Three maintenance IOTs are also used by the DF32-D. These IOTs are used to simulate certain pulses within the disk control for static logic tests. Since they all use device code 63, this code should not be used by other peripheral devices when a DF32-D is part of the system.

**NOTE**

For the DEAL and DEAC instructions, refer to the diagrams shown below:

| | | | |
|---|---|---|---|
| Bits 1-5 (DEAL, DEAC Inst.) | Accumulator + (Low Order 12 Bits) 0-11 of DMAW or DMAR | → | Disk Address (17 Bit) |
| Field Bits 6-8 (DEAL, DEAC Inst.) | + Cell 7751 (Current Address) | → | Current Address (Memory) Address (15 Bit) |

The computer can handle 12 bits; therefore, the high order bits for disk and memory address are manipulated by the DEAL and DEAC instructions. Low order bits are manipulated in the AC.

## TYPE RF08 DISK FILE AND CONTROL AND TYPE RS08 EXPANDER DISK FILE

The RF08 control and the RS08 disk combine to provide fast, low-cost, random access, bulk storage for the computer. One RF08/RS08 provides 262,144 13-bit words of storage. Up to four RS08 disks can be added to the RF08 control for a total of 1,048,576 words of storage. Data is recorded on a single disk surface by 128 fixed read/write heads.

Data transfer is accomplished through the three-cycle break system of the computer and its associated required options, which are the same as for the DF32/DS32 system. Fast track-switching time permits spiral read or write. Data may be read or written in blocks of from 1 to 4096 words. Transfers accross disks are handled automatically by the control unit.

### RF08/RS08 Specifications

| | | |
|---|---|---|
| Disks | Four RS08s may be controlled by one RF08 for 1,048,576 words. | |
| Storage Capacity | Each RS08 stores 262,144 13-bit words (12 plus one even parity bit) | |
| Data Transfer Path | 3-Cycle Break | Address Locations<br>7750 Word Count<br>7751 Current Address |
| Data Transfer Rate | 60 Hz Power<br>16.0 $\mu$s per word | 50 Hz Power<br>19.2 $\mu$s per word |
| Minimum Access Time | 258 $\mu$s | 320 $\mu$s |
| Average Access Time | 16.9 ms | 20.3 ms |
| Maximum Access Time | 33.6 ms | 40.3 ms |
| Program Interrupt | 33 ms Clock Flag<br>Data Transmission Complete Flag<br>Error Flag | |
| Write Lock Switches | Eight switches per disk capable of locking out any combination of eight 16,384 word blocks in addresses 0 to 131,071. | |
| Data Tracks | 128 | |
| Words Per Track | 2048 | |
| Recording Method | NRZ1 | |
| Density | 1100 bpl Maximum | |
| Timing Tracks | 3 plus 3 spare (spares can be used to recover data on disk) | |

**RF08/RS08 Specifications (Cont)**

| | |
|---|---|
| Operating Environment | Recommended temperature 65° to 90°F. |
| Vibration/Shock | Good isolation is provided. To prevent data errors, extreme vibrations should be avoided while the RS08 is transferring information. |
| Heat Dissipation | RF08: 150W<br>RS08: 300W |
| AC Power Requirements | 115/230 ± 10% Vac, single phase, 50 ± 2 or 60 ± 2 Hz, 5A (maximum) for logic power.<br>(Logic power for one RF08 and up to four RS08s is provided by one DEC Type 705B Power Supply) Additional line current is required for RS08 disk motor as shown below. |
| RS08 Motor Power Requirements | Motor start, 5.5A for 20 ± 3s. Motor run, 4.0A continuous @ 115 Vac. (A stepdown autotransformer is provided for 230 Vac operation). |
| Line Frequency Stability | Maximum line frequency drift 0.1 Hz/s. A constant frequency motor-generator set or static ac/ac inverter should be provided for installation with unstable power sources. |
| Motor Bearing Life | Expected operating life of at least 20,000 hours, under standard computer operating environment. |
| Reliability | Six recoverable errors and one nonrecoverable error in 2 x $10^9$ bits transferred. A recoverable error is defined as an error that occurs only once in four successive reads. All other errors are nonrecoverable. On-off cycling of the RS08 is not recommended. For this reason, the RS08 motor control operates independently of the computer power control. |
| Cabinet | A dedicated cabinet is designed to accommodate one RF08, up to two RS08s and power supply. Two additional RS08s can be mounted in a second cabinet. Other equipment should not be mounted in disk cabinets. |
| Shipping Information | Weight of RF08, one RS08, power supply and cabinet:<br>590 lb (crated)<br>500 lb (uncrated)<br>Weight of RF08, two RS08, power supply and cabinet: |

**Programming Instructions**

The programming instructions for the RFO8/RSO8 differ slightly from those provided in the DF32/DS32 description. The extended address capability and associated instructions (DCEA, DEAL, and DEAC) are replaced, in sequence, by interrupt enable and memory address extension register instructions (DCIM, DIML, and DIMA).

**Clear Disk Interrupt Enable and Core Memory Address Extension Register (DCIM)**

Octal Code: 6611
Event Time: 1
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the disk interrupt enable (DIE) and core memory address extension (MAE) registers.
Symbol: 0 → DIE, 0 → MAE

**Load Interrupt Enable and Memory Address Extension Register (DIML)**

Octal Code: 6615
Event Time: 1, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the interrupt enable (IE) and MAE, then load the interrupt enable and 'memory address extension registers with data held in the AC. Then clear AC.

NOTE

Transfers cannot occur across memory fields. Attempts to do so will cause the transfer to "wrap around" within the specified memory field.

Symbol: 0 → IE, 0 → MAE
AC 3-15 → IE, AC 6-8 → MAE
0 → AC

AC TO DISK STATUS REGISTER

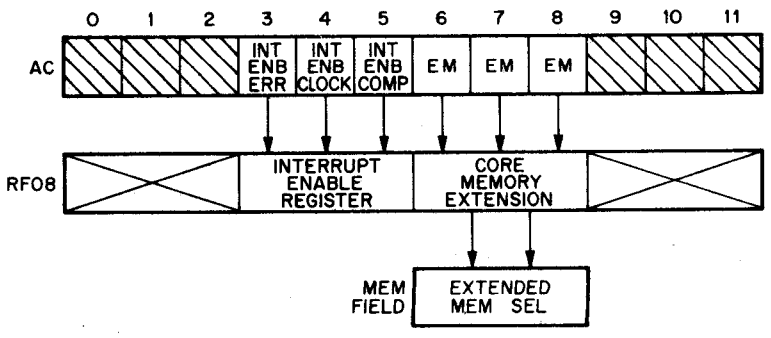



Figure 7-12 AC TO DISK STATUS REGISTER

**Load Interrupt and Extended Memory Address (DIMA)**
Octal Code: 6616
Event Time: 2, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the AC. Then load the contents of the status register (STR), into the AC to allow program evaluation.

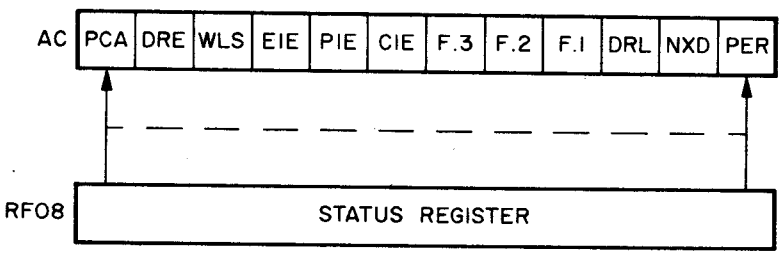



Figure 7-13 DISK TO AC STATUS REGISTER

| AC Bit | Abbr. | Description |
|---|---|---|
| 0 | PCA | Photocell Sync Mark (available 100 $\mu$s status) |
| 1 | DRE | Data Request Enable (maintenance only status) |
| 2 | WLS | Write Lock Status |
| 3 | EIE | Error Interrupt Enable |
| 4 | PIE | Photocell Interrupt Enable |
| 5 | CIE | Completion Interrupt Enable |
| 6-8 | F | (FIELD) Core Memory Extension Fields |
| 9 | DRL | Data Request Late |
| 10 | NXD | Nonexistent Disk |
| 11 | PER | Parity Error |
| *Symbol:* | *0 → AC* | |
| | STR → AC | |

In addition to these changes in instructions, the RF08/RS08 utilizes six additional instructions: DFSE, DISK, DCXA, DXAL, DXAC, and DMMT.

**Skip on Disk Error (DFSE)**
Octal Code: 6621
Event Time: 1
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Skip next instruction if there is parity error, data request late, write lock status, or nonexistent disk flag set.
Symbol: Parity error, data request late, write lock status, or nonexistent disk flags are set, PC + 1 → PC.

**Skip Error or Completion Flag (DISK)**
Octal Code: 6623
Event Time: 2
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: If either the error or data completion flag (or both) is set, the next instruction is skipped.
Symbol: If PER or Data Complete, PC + 1 → PC.

**Clear High Order Address Register (DCXA)**
Octal Code: 6641
Event Time: 1
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the high order 8-bit disk address register (DAR).
Symbol: 0 → DAR

**Clear and Load High Order Address Register (DXAL)**
Octal Code: 6643
Event Time: 1, 2
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the high order 8 bits of the DAR. Then load the DAR from data stored in the AC. Then clear AC.
Symbol: 0 → DAR high order 8 bits,
AC → DAR,
0 → AC

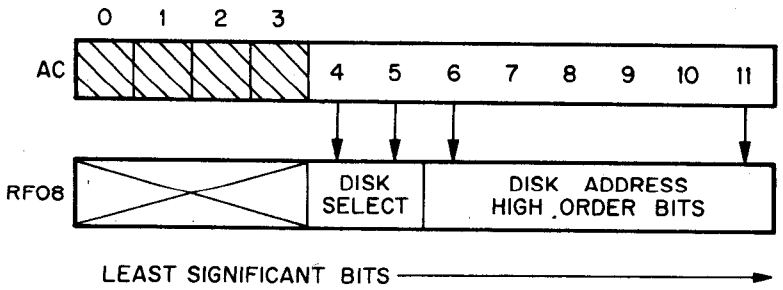



Figure 7-14 Higher Order Address Word Transfer

**Clear Accumulator and Load DAR Into AC (DXAC)**
Octal Code: 6645
Event Time: 1, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: Clear the AC; then load the contents of the high order 8-bit DAR into the AC.
Symbol: 0 → AC,
DAR high order 8 bits → AC

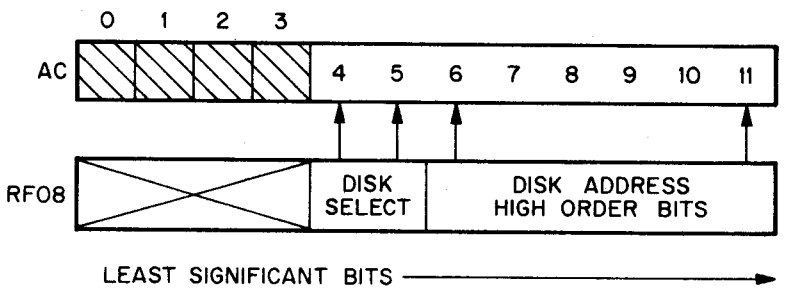



Figure 7-15 Disk Address Transfer to AC

**Initiate Maintenance Register (maintenance purposes only) (DMMT)**

Octal Code: 6646
Event Time: 2, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 $\mu$s
Operation: For maintenance purposes only with the appropriate maintenance cable connections and the disk disconnected from the RS08 logic, the following standard signals may be generated by IOT 66-46 and associated AC bits. AC is cleared and the maintenance register (MAIR) is initiated by issuing an IOT 6601 command.

AC (1) Track A Pulse
AC (1) Track B Pulse
AC (1) Track C Pulse
AC (1) DATA PULSE (DATA HEAD #0)
AC (1) Photocell
AC (1) DBR
Setting DBR to a 1 causes data break request in computer.

Symbol: AC → MAIR

Three-cycle data break locations: word count address is 7550 (field 0), current address is 7751 (field 0).

DF32 Programming Compatibility

The IOT instructions 660X and 6622 are identical in every respect to the DF32 instruction; i.e., the same operations are performed. The 661X and 662X instructions differ only in the following:

a. OIT 6615 does not transmit the extended disk address bits for addressing over 32K; instead, AC 3-5 are assigned to enable or disable conditions on the program interrupt line. The AC is cleared upon execution of this instruction.

b. IOT 6616 no longer reads back the extended address bits by 1 through 5 into the AC. These bits are assigned to examine the status of interrupt enable. In addition, AC2 indicates the status of write lock and AC10 shows only nonexistent disk conditions. AC1 shows the condition of data request enable used for maintenance purposes.

c. IOT 6621 has been changed to skip on error rather than no-error. Non-existent disk has been included as an error skip condition.

d. IOT 6623 (DISK) is a new skip instruction that will skip on either error or completion flags or both.

The DF32 maintenance instruction IOT 663X is not assigned to the RF08 system.

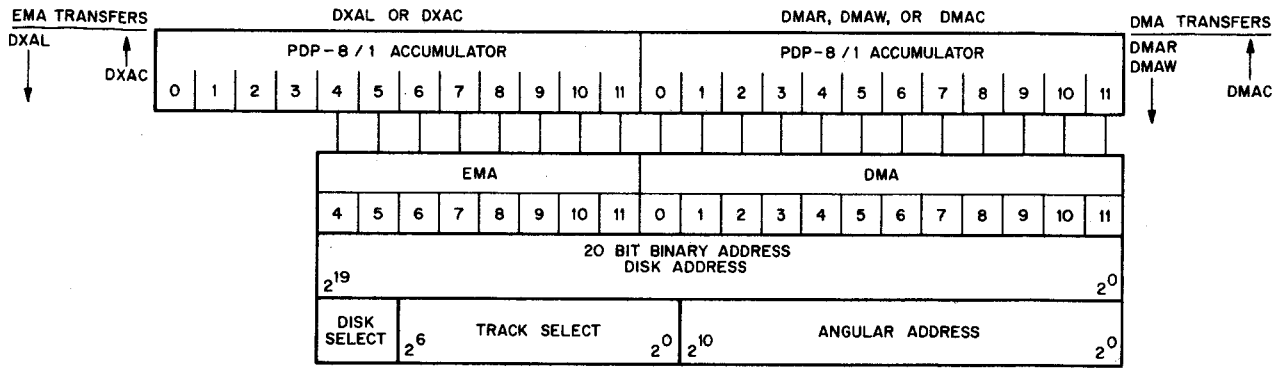



Figure 7-16 RF08 Addressing Format

## Programming Example

### Software

A sample of a typical I/O routine for the RF08/RS08 is as follows:

```
0200  4777            JMS I    (DISKIO)
0201  0000  FUNCT,    0                /X0=READ, X1=WRITE (X=0=7 MEMORY FIELD)
0202  0000  WDCT,     0                /+ WORD COUNT
0203  0000  CORE,     0                /CORE LOCATION
0204  0000  DSKHI,    0                /HIGH ORDER 8 BITS
0205  0000  DSKLOW,   0                /LOW ORDER 12 BITS
0206  5020            JMP ERROR                /ERROR RETURN (AC=ERROR CONDITION)
                                       /NORMAL RETURN (AC=0)

0207  0000  DISKIO,   0
0210  7300            CLL CLA
0211  1607            TAD I DISKIO
0212  6615            DIML             /LOAD EXTENDED MEMORY BITS
0213  1607            TAD I DISKIO
0214  0376            AND (7
0215  7640            SZA CLA

0216  7126            STL RTL          /+2
0217  1375            TAD (3
0220  1374            TAD (6600
0221  3236            DCA RORW                 /6603=READ, 6605=WRITE
0222  2207            ISZ DISKIO
0223  1607            TAD I DISKIO
0224  7041            CIA
0225  3773            DCA I (7750      /STORE=WORD COUNT
0226  2207            ISZ DISKIO
0227  1607            TAD I DISKIO
0230  3772            DCA I (7751)     /LOAD CORE ADDRESS
0231  2207            ISZ DISKIO
0232  1607            TAD I DISKIO
0233  6643            DXAL             /LOAD HIGH ORDER 9
                                       /BITS OF DISK ADDRESS,

0234  1607            TAD I DISKIO
0235  2207            ISZ DISKIO

0236  0000  RORW, .   0                /READ OR WRITE

0237  6623            DISK             /DONE?
0240  5237            JMP .-1          /NO
0241  6621            DFSE             /YES, ERROR?
0242  2207            ISZ DISKIO       /SKIP TO NORMAL RETURN
0243  5607            JMP I DISKIO     /RETURN

      6615  DIML = 6615
      6623  DISK = 6623
      6643  DXAL = 6643
      6621  DFSE = 6621
      0020  ERROR = 20

0372  7751
0373  7750
0374  6600
0375  0003
0376  0007
0377  0207

CORE     0203
DFSE     6621
DIML     6615
DISK     6623
DISKIO   0207
DSKHI    0204
DSKLOW   0205
DXAL     6643
ERROR    0020
FUNCT    0201
RORW     0236
WDCT     0202
```

## MAGNETIC TAPE OPTIONS

The External Bus Magnetic Tape Options include:

a. The TU56 Dual DECtape Transport and TC08 DECtape control,
b. The TU10 DECMAGtape Transport and TC58 Automatic Magnetic Tape Control.

### DECtape

The DECtape system is a standard option for the PDP-8/E that serves as an auxiliary magnetic tape data storage facility. The DECtape system stores information at fixed positions on magnetic tape, as in magnetic disk or drum storage devices, rather than at unknown or variable positions, as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information has a number of features to improve its reliability and make it exceptionally useful for program updating and program editing applications. These features are: phase or polarity sensed recording on redundant tracks, bidirectional reading and writing, and a simple mechanical mechanism utilizing hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion).
Four basic DECtape configurations are identified in the following table.

| SYSTEM DESIGNATION | DECtape | CONTROL | PREREQUISITE | REMARKS |
|---|---|---|---|---|
| None | TU56 (Dual Drive) | TC08 | KA8-E<br>KD8-E<br>PDP-8/E | Up to 4 Dual TU56's per control. (8 drive units) |
| None | TU56 (Single Drive) | TC08 | KA8-E<br>KD8-E<br>PDP-8/E | Up to 4 single DECtape drive units. |
| TD8-EM | TU56 (Dual Drive) | TD8-E | PDP-8/E | Up to 4 Dual Drive TU56's per control.<br>(8 drive units)<br>Control plugs into OMNIBUS. |
| TD8-EA | TU56H (Single Drive) | TD8-E | PDP-8/E | Up to 4 single drive units. Control plugs into OMNIBUS. |

Magnetic tape options operated on the external bus of the PDP-8/E require the use of the KA8-E Positive I/O Bus Interface module and the KD8-E Data Break Interface module as prerequisites.

**DECtape Format**

DECtape utilizes a 10-track read/write head. Tracks are arranged in five nonadjacent redundant channels: a timing channel, a mark channel, and three information channels. Redundant recording of each character bit on nonadjacent tracks materially reduces bit dropouts and minimizes the effect of skew. The series-connection of corresponding track heads within a channel and the use of Manchester phase recording techniques, rather than amplitude sensing techniques, virtually eliminate dropouts.

The timing and mark channels control the timing of operations within the control unit and establish the format of data contained on the information channels. The timing and mark channels are recorded prior to all normal data reading and writing on the information channels. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing channel. Therefore, wide variations in the speed of tape motion do not affect system performance. Information read from the mark channel is used during reading and writing data to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control mode. During normal data reading, the control assembles 12-bit computer-length words from four successive lines read from the information channels of the tape. During normal data writing, the control disassembles 12-bit words and distributes the bits so they are recorded on four successive lines on the information channels. A mark-channel error-check circuit ensures that one of the permissible marks is read in every six lines on the tape. This 6-line mark-channel sensing requires that data be recorded in 12-line segments (12 being the lowest common multiple of 6-line marks and 4-line data words) which correspond to three 12-bit words.

A tape contains a series of data blocks that can be of any length which is a multiple of three 12-bit words. Block length is determined by information on the mark channel. A uniform block length is usually established over the entire length of a reel of tape by a program that writes mark and timing information at specific locations. The ability to write variable-length blocks is useful for certain data formats. For example, small blocks containing index or tag information can be alternated with large blocks of data. (Software supplied with DECtape allows writing for fixed block lengths only.)

Between the blocks of data are areas called interblock zones. The interblock zones consist of 30 lines on tape before and after a block of data. Each of these 30 lines is divided into five 6-line control words. These 6-line control words allow compatibility between DECtape written on any of DEC's 12-, 18-, or 36-bit computers. As used on the PDP-8/E, only the last four lines of each control word are used.

Block numbers normally occur in sequence from 1 to n. There is one block numbered 0 and one block n + 1. Programs are entered with a statement of the first block number to be used and the total number of blocks to be read or written. The total length of the tape is equivalent to 849,036 lines, which can be divided into any number of blocks up to 4096 by prerecording of the mark track. The maximum number of blocks is determined by the following equation in which n(b) equals number of

blocks and n(w) equals number of words per block (n(w) must be divisible by 3).

$$n(b) = \frac{212112}{n(w) + 15} - 2$$

DECtape format is illustrated in Figures 7-17 through 7-20.

Figure 7-17 DECtape Track Allocations

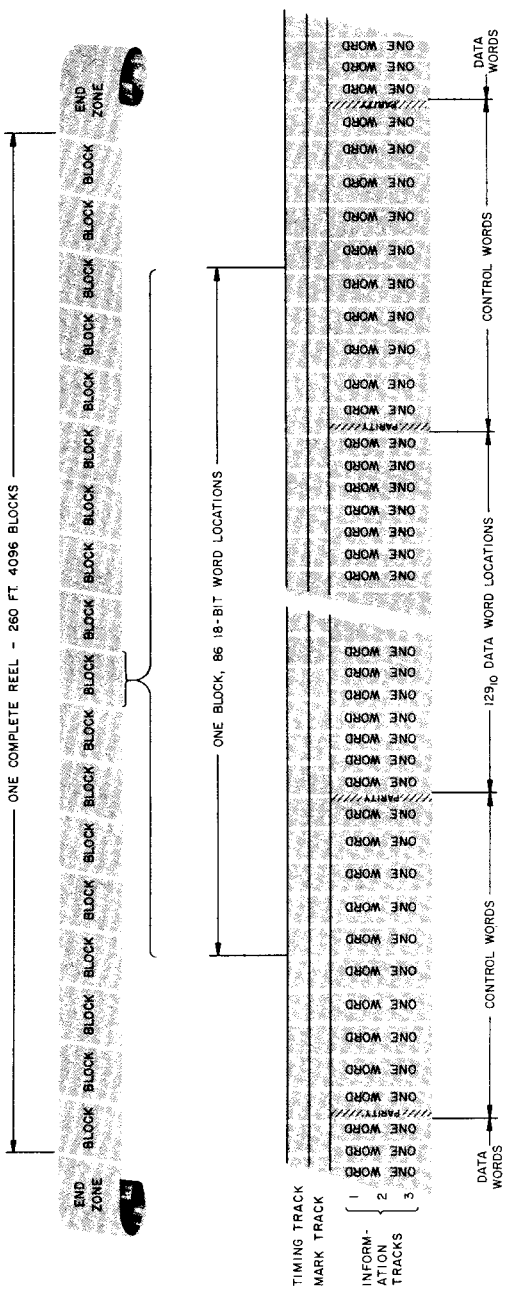



Figure 7-18 DECtape Mark Channel Format

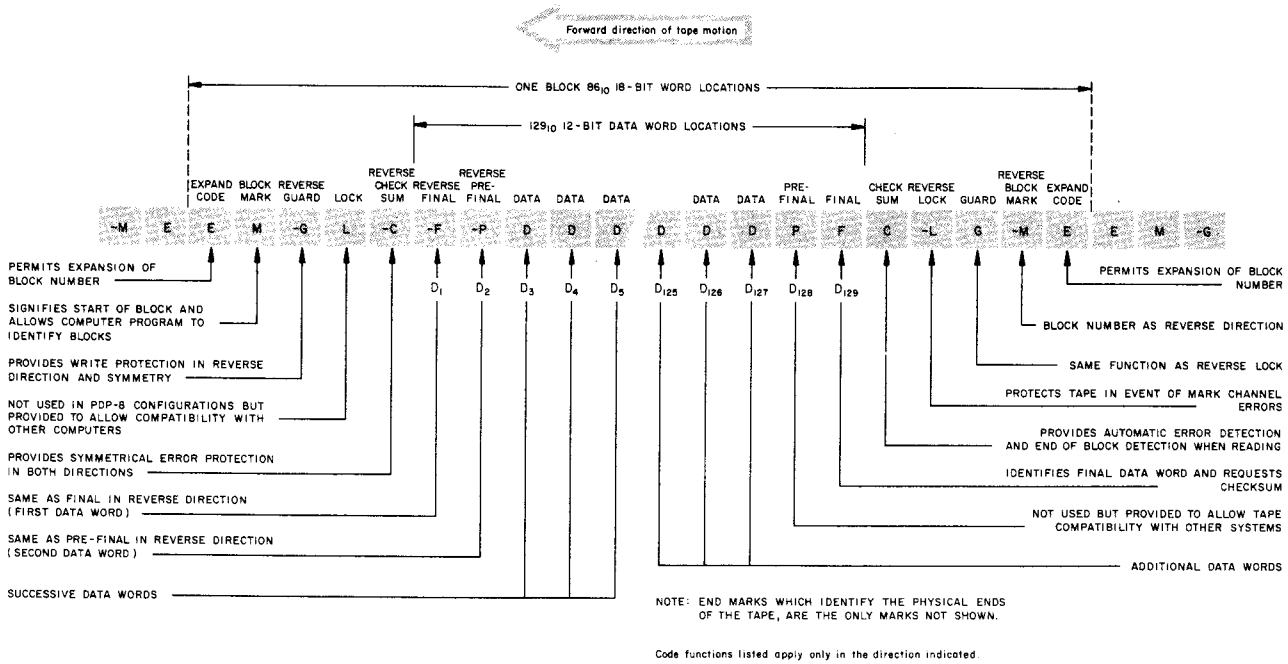



Figure 7-19 DECtape Control Word and Data Word Assignments

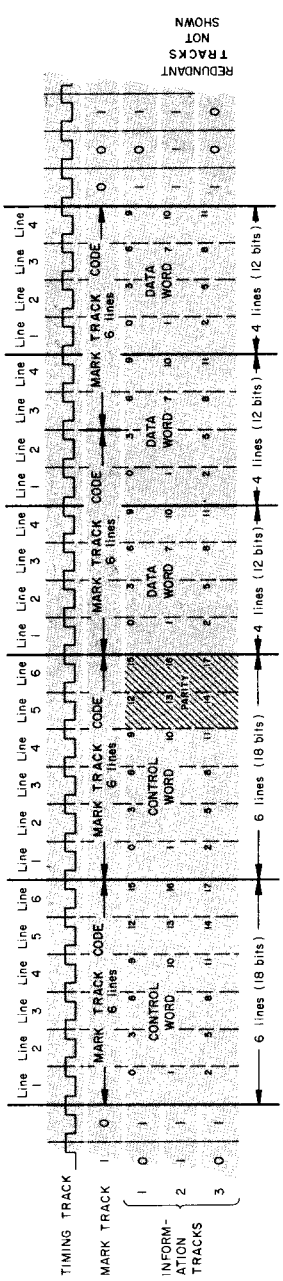



Figure 7-20 DECtape Format Details

**TU56 Dual DECtape Transport and TC08-P DECtape Control**
A DECtape system on the external bus can contain up to four TU56 Dual DECtape transports (the equivalent of up to eight single tape transports) controlled from one TC08-P unit. Data transfers between the computer and tape are implemented using the three-cycle data break facilities of the computer (refer to Chapter 10 for three-cycle data break description). Thus, the KA8-E Positive I/O Bus Interface and KD8-E Data Break Interface units are prerequisites.

Data is stored on tape in the form of three-bit words (refer to tape format) and is transferred between the tape and computer in the form of 12-bit words. A 12-bit read/write buffer in the TC08 assembles and disassembles the information for transfer. For transfers to the computer, data is read from four consecutive lines of tape and assembled into a 12-bit word. When transferred to the computer, the 12-bit word is supplied via external bus lines DATA00-11 to the KD8-E Data Break Interface. This unit, in turn, provides the word to OMNIBUS lines DATA0-11 under data break control. For transfers to tape, the KA8-E unit buffers the 12-bit words and provides them to the TC08 via external bus lines BMB00-11. The TC08 disassembles these words and supplies them to the tape transport for the writing of four tape lines. Transfer of command and control signals is effected by IOT instructions. These instructions are provided to the TC08 via the BMB00-11 external bus lines.

The TC08 contains registers and control flip-flops that form two status registers (designated A and B) for transfer of information to and from the computer accumulator.

**TU56 Dual DECtape Transport**
The TU56 provides the PDP-8/E user with a compact, high-reliability dual-reel tape transport in just 10½ inches of rack space. When used with the TC08-P control, the TU56 provides two fixed -address, magnetic tape facilities for high-speed loading, readout, and updating of programs and data. The TU56 transport contains the tape read/write heads, drive mechanisms, and switching circuits for tape drive and direction. All transport operations (except local) are controlled by the TC08 from program instructions. The TC08 selects the transport, controls tape motion and direction, selects a read or write operation and buffers data transferred. Information is stored in the form of three-bit words on a one-mil Mylar tape with ten tracks. This tape, ¾ inches in width and 260 feet in length, is contained on a reel that is less than four inches in diameter. Information can be recorded or read for either direction of tape motion.

Redundant recording (each bit of data and timing is recorded on two tracks) ensures high reliability and eliminates the need for parity checking. Data words are recorded on six of the ten tracks and four tracks are allotted for mark and timing channels. Other features include TTL logic, dynamic braking for shorter turnaround time, and DC motor drive to eliminate line frequency dependency. Connections from the read/write head are made directly to the external control, which contains the read and write amplifiers.

The logic circuits of the TU56 transport control tape movement in either direction over the read/write head. Tape drive motor control is com-

pletely through the use of solid-state switching circuits to provide fast, reliable operation. These circuits control the torque of the two motors that transport the tape across the head according to the established function of the device: i.e., go, stop, forward, or reverse. In normal tape movement, full torque is applied to the forward or leading motor and a reduced torque is applied to the reverse or trailing motor to keep proper tension on the tape. Since tape motion is bidirectional, each motor serves as either the leading or trailing drive for the tape, depending upon the forward or reverse control status of the TU56.

Tape movement can be controlled by commands originating in the computer or by manual operation of switches on the front panel of the transport. Manual control is used to mount new reels of tape on the transport, or as a quick maintenance check for proper operation of the control logic in moving the tape.

Since DECtape is a fixed address system, the programmer need not know accurately where the tape has stopped. To locate a specific point on tape he must only start the tape motion in the search mode. The address of the block currently passing over the head will be automatically transferred to core where it can be compared with the desired block address and tape motion continued or reversed accordingly. TU56 typical time characteristics are provided below, but are not accurately controlled.

| | |
|---|---|
| Start Time | 150 ms* |
| Stop Time | 100 ms* |
| Turnaround Time | 200 ms* |

*Also, see control specifications. These times are frequently lengthened by the particular control.

**Specifications**

| | |
|---|---|
| Transfer rate | 33,300 three-bit characters per second |
| Information capacity | 2.7 million bits per reel |
| Density | 350 + or − 55 bits per inch |
| Tape speed | 93 + or − 12 inches per second |
| Tape motion | Bidirectional |
| Start time | 150 + or − 15 ms |
| Stop time | 100 + or − 10 ms |
| Turn around time | 200 + or − 50 ms |
| Reel capacity | 250 ft. of ¾ inch, 1 mil Mylar tape |
| Reel size | 3.9 inches in diameter |
| Mounting | Mounts in a standard 19-inch equipment rack |
| Size | 10½ in. high, 19 in. wide, 9¾ in. deep |
| Cooling | Internally mounted fans provided |
| Power requirements | a. + 10V @ 0.53 amps or + 5V @ 0.55 amps<br>b. − 15V @ 0.45 amps<br>c. 115/220 VAC + or − 10% @ 2.85/1.43 amps 47-63 Hz |
| Environmental | Temperature: 40 degrees F to 90 degrees F<br>Humidity: 15% to 80% Relative Humidity<br>Internal Temp Rise: 10% F above ambient |
| Reliability | Recoverable Error Rate-less than 1 part in 2.5 x 10 ↑ 10 transfers |

**TC08 DECtape Control**

The TC08 control buffers and controls information transfers between one to eight TU56 transports (one to four TU56 Dual DECtape transports) interfacing with the external bus of the PDP-8/E. Transfers are implemented using the three-cycle data break facilities of the computer; thus, the KA8-E Positive I/O Bus Interface and the KD8-E Data Break Interface modules are prerequisites.

During both input and output operations, the TC08 receives data and control information from the processor and generates the appropriate signals to the selected transport to execute the programmed commands. Binary information is transferred between the tape transport and the computer as one 12-bit computer word every 133⅓ μs. When writing, the TC08-P disassembles the 12-bit word into four successive three-bit words to be written on tape. During read operations, the TC08 assembles the four successive three-bit words into one 12-bit word for transfer to the computer. Transfers between the computer and the control always occur in parallel for a 12-bit word. Data transfers use the three-cycle data-break (high speed channel) facility of the computer. (Refer to Chapter 10 for details of 3-cycle data-break transfers.)

The TC08 contains the following primary control and data processing circuits:

a. Device selector and IOT decoding logic to command a transport from program instructions.
b. A 12-bit buffer register for assembling tape inputs and disassembling computer data.
c. A command and status register (designated Status Register A) for defining: (1) the active transport, (2) direction of tape, (3) tape motion, (4) operating mode, (5) function (read/write, search, etc.), (6) interrupt enable, and (7) clearing of flags.
d. A status register (designated Status Register B) for indicating error status and other status.
e. Flag circuits that provide the program with conditional indications and requests.
f. Tape motion and direction control circuits.
g. Mark track generation and detection circuits with error detectors.
h. Longitudinal parity generation and checking circuits.
i. Data break request circuits.

Programmed IOT instructions are generated to clear, read, or load Status Register A and to read or load Status Register B. An IOT skip instruction is also provided to test the status of flag circuits. These instructions are provided to the TC08-P control via the KA8-E Positive I/O Bus Interface and external bus lines BMB-00-11.

A control and indicator panel is also provided with the TC08. A single control, NORMAL/WRTM, places the TC08 in the write timing and mark track mode (WRTM), or else in the NORMAL mode. The indicators denote the current status of the control including the tape transport selected, motion, function, interrupt status, error flags, and other status indications.

Three program flags in the TC08-P control serve as condition indicators and request originators.

a. DECtape Flag (DT): This flag indicates the active/done status of the current function.
b. Data Flag (DF): This flag requests a data break to transfer a block number into the computer during a search function, or when a data word transfer is required during a read or write function.
c. Error Flag (EF): Detection of any nonoperative condition by the control sets this flag in status register B and stops (except for parity errors) the selected transport. The error conditions indicated by this flag are:
   (1) Mark Track Error: This error occurs any time the information read from the mark channel is erroneously decoded.
   (2) End of Tape: The end zone on either end of the tape is over the read head.
   (3) Select Error: This error occurs 5 $\mu$s after loading status register A to indicate any one of the following conditions:
   (a) Specifying a unit select code which does not correspond to any transport select number, or which is set to multiple transports.
   (b) Specifying a write function with the WRITE ENABLED/WRITE LOCK switch in the WRITE LOCK position on the selected transport.
   (c) Specifying an unused function code (i.e., AC6-8 = 111).
   (d) Specifying any function except write timing and mark track with the NORMAL/WRTM switch in the WRTM position.
   (e) Specifying the write timing and mark track function with the NORMAL/WRTM switch in the NORMAL position.
   (4) Parity Error: This error occurs during a read data function if the longitudinal parity or check sum over the entire data word, the reverse check character, and the check character is not equal to 1.
   (5) Timing Error: This error indicates a program fault caused by one of the following conditions:
   (a) A data break did not occur within 17 $\mu$s (+ or − 30%) of the data break request.
   (b) The DT flag was not cleared by the program before the control attempt to set it.
   (c) The read data or write data function was specified while a data block was passing the read head.

Three-cycle data break locations: The TC08-P uses location 7754 of field 0 for word count and 7755 of field 0 for current address.

**Control Modes**—The DECtape system operates in either the normal or continuous mode, as determined by bit 5 of status register A during a DTXA command. *Operation in each mode is as follows:*

a. Normal (NM): Data transfers and flag settings are controlled by the format of information on the tape.

b. Continuous (CM): Data transfers and flag settings are controlled by a word count read from core memory during the first cycle of each three-cycle data break, and by tape format.

**Functions**—The DECtape system performs one of seven functions, as determined by the octal digit loaded into status register A during a DTXA command. These functions are:

a. Move: Initiates movement of the selected transport tape in either direction. Mark channel decoding is inhibited in this mode except for end of tape.
b. Search: As the tape is moved in either direction, sensing of a block mark causes a data transfer of the block number. If the word count overflows in either NM or CM, the DT flag is set and causes a program interrupt. After finding the first block number, the CM can be used to avoid all intermediate interrupts between the current and the desired block number. This makes a virtually automatic search possible.
c. Read Data: This function is used to transfer blocks of data into core memory with the transfer controlled by the tape format. In NM, the DT flag is set at the end of a block and causes a program interrupt. In CM, transfers stop when the word count overflows, the remainder of the block is read for parity checking, and then the DT flag is set.
d. Read All: Read all is used to read tape in an unusual format, since it causes all lines to be read. In NM, the DT flag is set at each data transfer. In CM, the DT flag is set when WCO occurs. In either case, the DT flag causes a program interrupt.
e. Write Data: This function is used to write blocks of data with the transfer controlled by the standard tape format. After word count overflow occurs, zeros are written in all lines of the tape to the end of the current block. Then the parity checksum for the block is written. The DT flag rises as in the read function.
f. Write All: The write all function is used to write an unusual tape format (e.g., block numbers). The DT flag assertions are similar to the read all function.
g. Write Timing and Mark Track: This function is used to write on the timing and mark tracks, permitting blocks to be established or block lengths to be changed. The DT flag assertions are also similar to the read all function. This function is illegal unless a manual switch in the control is positioned to WRTM.

**Programmed Operation**—Prerecording of a reel of DECtape, prior to its use for data storage, is accomplished in two passes. During the first pass, the timing and mark channels are placed on the tape. During the second pass, forward and reverse block mark numbers, the standard data pattern, and the automatic parity checks are written. These functions are performed by the DECTOG program. Prerecording utilizes the write timing and mark channel function, and a manual switch on the control, which permits writing on the timing and mark channels, activates a clock, which produces the timing channel recording pattern and enables flags for program control. Unless this control function and switch are used simultaneously, it is physically impossible to write on the

mark or timing channels. An indicator lamp on the control panel lights when the manual NORMAL/WRTM switch is in the WRTM position. Under these conditions only, the write register and write amplifier, used to write on information channel 1 (bits 0, 3, 6, and 9), are used to write on the mark channel. This prerecording operation need only be performed once for each reel of DECtape.

There are two registers in the TC08 DECtape Control that govern tape operation and provide status information to the operating program. Status register A contains three unit selection bits, two motion bits, the continuous mode/normal mode bit, three function bits, and three bits that control the flags. Status register B contains the three memory field bits and the error status bits. PDP-8/E IOT microinstructions are used to clear, read, and load these registers. In addition, there is an IOT skip instruction to test control status.

Since all data transfers between DECtape and the computer memory are controlled by the data break facility, the program must set the WC and CA registers (locations 7754 and 7755, respectively) before a data break. After init ating a DECtape operation, the program should always check for error conditions (a program interrupt would be initiated if the error flag is enabled and if the program interrupt system is enabled). The DECtape system should be started in the search function to locate the block number selected for transfer; when the correct block is found, the transfer is accomplished by programmed setting of the WC, CA, and status register A.

When searching, the DECtape control reads block numbers only. These are used by the operating program to locate the correct block number. In NM, the DECtape flag is raised at each block number. In CM, the DECtape flag is raised only after the word count reaches zero. The current address is not incremented during searching and the block number is placed in core memory at the location specified by the content of the CA. Data is transferred to or from the computer core memory from locations specified by the CA register which is incremented by one before each transfer.

Each time the DECtape system is ready to transfer a 12-bit word, and when the start of the data position of the block is detected, the data flag is raised to initiate a data break request to the data break facility. Therefore, the main computer program continues running, but is interrupted approximately every 133⅓ $\mu$s for a data break to transfer a word. Transfers occur between DECtape and successive core memory locations specified by the CA. The initial transfer address minus one is stored in the CA by an initializing routine. The number of words transferred is determined by the tape format in NM, or by tape format and the word count in CM. At the conclusion of the data transfer, the DT flag is raised and a program interrupt occurs. The interrupt subroutine checks the DECtape error bits to determine the validity of the transfer, and either initiates a search for the next information to be transferred or returns to the main program.

During all normal writing transfers, a check character (the six-bit logical equivalent of the words in the data block) is computed automatically by

the control and is recorded automatically as one of the control words immediately following the data portion of the block. This same character is used during reading to determine that the data playback and recognition take place without error.

Any one of the eight tape transports may be selected for use by the program. After using a particular transport, the program can stop the transport currently being used and select another transport, or can select another transport while permitting the original selection to continue running. This is a particularly useful feature when rapid searching is desired, since several transports may be used simultaneously. Caution must be exercised, however; although the original transport continues to run, no tape-end detection or other sensing takes place. Automatic tape-end sensing that stops tape motion occurs in all functions, but only in the selected tape transport.

The following is a list of timing considerations for programmed operations. (These times are based on 129 12-bit data words per block.)

n(s) = the number of block numbers to be read in the search function and CM, counting through the one causing the word count overflow. Only the block number causing the word count overflow requests a program interrupt.

n(d) = number of words transferred divided by the number of words per block. If the remainder does not equal 0, use the next larger whole number.

n(A) = number of words transferred.

| OPERATION | TIMING |
|---|---|
| Answer a data break request | Up to 17 μs + or − 30% |
| Word transfer rate | One 12-bit word every 133 μs + or − 30% |
| Block transfer rate | One 129-word block every 18.2 ms + or − 30% |
| Change funtcion from search to read data for the current block after DT flag from block number | 400 μs + or − 30% |
| Change function from search to write data for current block after DT flag from block number | 400 μs + or − 30% |
| Change function from read data to search for the next block after DT flag from transfer completion | 1000 μs + or − 30% |
| Change function from write data to search for next block after DT flag from transfer completion | 1000 μs + or − 30% |
| DECtape flag rises in continuous mode | |
| Move function | Never |
| Search function | (n(s) ) x (18.2 ms + or − 30%) |
| Read data function | (n(D) ) x (18.2 ms + or − 30%) |
| Read all function | (n(A) ) x (133 μs + or − 30%) |

| OPERATION | TIMING |
|---|---|
| Write data function | (n(D) ) x (18.2 ms + or − 30%) |
| Write all function | (n(A) ) x (133 μs + or − 30%) |
| Write T & M function | (n(A) ) x (133 μs + or − 30%) |
| In normal mode | |
| Move function | Never |
| Search function | Every 18.2 ms + or − 30% |
| Read data function | Every 18.2 ms + or − 30% |
| Read all function | Every 133 μs + or − 30% |
| Write data function | Every 18.2 ms + or − 30% |
| Write all function | Every 133 μs + or − 30% |
| Write T & M function | Every 133 μs + or − 30% |

**Programming**

The following instructions are associated with TC08-P operation:

**Read Status Register A (DTRA)**

Octal Code: 6761
Execution Time: 2.6 μs
Operation: Transfers content of Status Register A to the AC. ORs AC0-9 with Status Register with the result appearing in AC. The AC is not cleared before the transfer. AC bit assignments are defined in Figure 7-21.

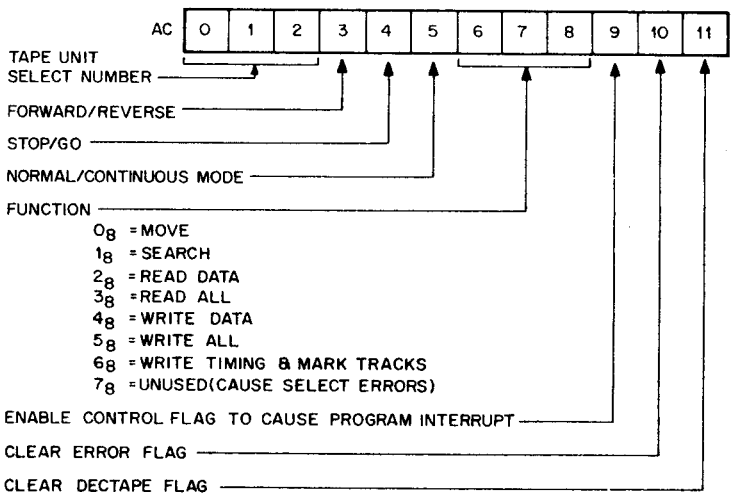



Figure 7-21 Status Register A Bit Assignments

**Clear Status Register A (DTCA)**

Octal Code: 6762
Execution Time: 2.6 μs
Operation: Clears Status Register A; DECtape and Error flag are undisturbed.

**Clear and Load Status Register A (DTLA)**

Octal Code: 6766
Execution Time: 3.6 μs
Operation: Clears Status Register A, then EXCLUSIVE ORs content of AC0-9 into Status Register A. Samples AC10 and 11 to control clearing of DECtape and error flags, then clears AC.

**Load Status Register A (DTXA)**

Octal Code: 6764
Execution Time: 2.6 μs
Operation: EXCLUSIVE ORs content of AC0-9 into Status Register A. Samples AC bits 10 and 11 to control clearing of Error and DECtape flags, then clears the AC.

**Skip On Flag (DTSF)**

Octal Code: 6771
Execution Time: 2.6 μs
Operation: If either DECtape or Error flags is set, skips the next instruction.

**Read Status Register B**

Octal Code: 6772
Execution Time: 2.6 μs
Operation: ORs content of Status Register B into AC. The AC is not cleared before transfer; AC bit assignments are defined in Figure 7-22.

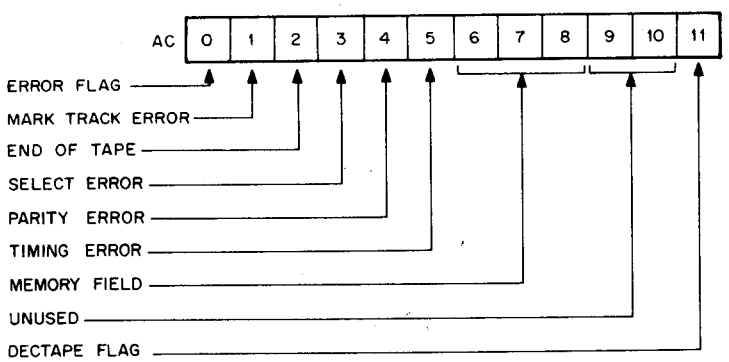



Figure 7-22 Status Register B Bit Assignments

**Load Status Register B**

Octal Code: 6774
Execution Time: 2.6 μs
Operation: Loads memory field portion of Status Register B with content of AC6-8, then clears the AC.

An elementary subroutine for reading or writing DECtape is given below. This routine does not use the interrupt, and exits with the DECtape drive halted.

The format for calling the subroutine is:

```
JMS (IDTAPE)    Effective JMS to IDTAPE, i.e., indirect JMS if IDTAPE
                  is not on same page as calling sequence.
WORD 1,         Bits 0-2, unit number
                Bit 3, start search (0=forward 1=reverse)
                Bits 6-8, memory field for transfer
                Bit 10, error return (0=JMP WORD 5)
                                     (1=JMP I WORD 5)
                Bit 11, function (0=READ 1=WRITE)
WORD 2,         Block number for start of transfer
WORD 3,         2's complement of the number of words to transfer
WORD 4,         Memory address of first transfer minus 1
WORD 5,         Error return or address for error return (to correspond
                  to Bit 10 of Word 1)
RETURN,         Transfer completed, return with AC cleared
```

```
ID7400,  7400
                                /AND MASK (MUST BE FIRST CELL IN
                                /PAGE)
IDTAPE,  0                      /ENTRY TO SUBROUTINE
         CLA
         TAD     I IDTAPE       /SAVE WORD 1
         DCA     IDCODE
         ISZ     IDTAPE         /ADVANCE TO BLOCK NUMBER (WORD
                                /2)
         TAD     IDCODE
ID0200,  AND     ID7400         /UNIT NUMBER AND DIRECTION BIT
         TAD     ID0010         /PUT INTO SEARCH MODE
         DTCA    DTXA
         DTLB                   /CLEAR FIELD BITS
         TAD     IDWC
         DCA     I IDCA         /SET UP CURRENT ADDRESS (7755)

/ERROR WHILE SEARCHING . . . NORMALLY ENTERED WITH B
/STATUS REGISTER IN THE AC, PERFORMS TURN AROUND IF END
/ZONE ERROR, AND FORCES THE STOP-GO BIT TO GO

IDSERR,  RTL
         RAL                    /MOVE END ZONE FLAG TO LINK
         CLA     CML
         TAD     ID0200         /GET DECTAPE GO FLAG

/CHANGE DIRECTION IF AND ONLY IF THE LINK IS ZERO,

IDCONT,  SNL                    /CHECK DIRECTION AND SIGN
         TAD     ID0400         /REVERSE DIRECTION
         DTXA                   /ENTER AND GO IN SEARCH MODE
         DTSF    DTRB           /IDLE . . AND LOAD ERROR FLAG
         JMP     .-1            /WAIT UNTIL FLAG COMES UP
         SPA                    /TEST ERROR FLAG
         JMP     IDSERR
```

```
        DTRA            /GET DIRECTION BIT
        RTL
        RTL             /DIRECTION BIT GOES TO LINK
        SZL     CLA
        TAD     ID0002  /REVERSE . . . GET "BLOCK TO FIND"
                        /-2
        TAD     I IDWC  /ADD IN LAST BLOCK SEEN
        CMA             /COMPLEMENT
        TAD     I IDTAPE /ADD IN "BLOCK TO FIND"
        CMA
        SZA     CLA     /BLOCK NUMBERS MATCH?
        JMP     IDCONT  /REENTER SEARCH LOOP
        SZL             /CHECK DIRECTION BIT
        JMP     IDCONT+1 /TURN AROUND IF REVERSE

/END OF SEARCH LOOP, TAPE IS NOW AT DESIRED BLOCK
/TRAVELING IN A FORWARD DIRECTION,

        ISZ     IDTAPE
        TAD     I IDTAPE /GET WORD COUNT
        DCA     I IDWC
        ISZ     IDTAPE
        TAD     I IDTAPE /GET TRANSFER ADDRESS
        DCA     I IDCA
        TAD     IDCODE
        DTLB            /LOAD FIELD BITS
        IAC             /GET READ-WRITE FLAG
        AND     IDCODE
        RTL     CLL     /MULTIPLY BY 20 (OCTAL)
        RTL
        TAD     ID0130  /BUILD INSTRUCTION
        DTXA            /START UP READ OR WRITE
        DTSF    DTRB    /WAIT . . AND LOAD ERROR FLAG
        JMP     .-1
        ISZ     IDTAPE  /ADVANCE TO WORD 5
        SMA             /SKIP IF ERROR FLAG SET
        ISZ     IDTAPE  /ADVANCE TO WORD 6 . . . NORMAL
                        /EXIT
        SPA     CLA     /SKIP FOR NORMAL EXIT
        TAD     IDCODE  /GET INDIRECT RETURN BIT
        RTR             /MOVE TO LINK
        SNL     CLA     /SKIP IF JMP I <WORD 5>
        JMP     .+3
        TAD     I IDTAPE /MAKE DOUBLE INDIRECT RETURN
        DCA     IDTAPE
        DTRA
        AND     ID0200  /GET STOP-GO BIT
        TAD     ID0002  /PRESERVE DECTAPE ERROR FLAGS
        DTXA            /STOP TAPE
        JMP     I IDTAPE /EXIT
IDWC,   7754            /WORD COUNT FOR DATA BREAK
IDCA,   7755            /CURRENT ADDRESS FOR DATA BREAK
ID0010, 10              /SEARCH FUNCTION BIT
```

```
ID0400,  400              /FORWARD-REVERSE BIT
ID0130,  130              /USED TO BUILD READ AND WRITE
                          /CODE
ID0002,  2
IDCODE,  0
```

**Software**

Four types of programs have been developed as DECtape software for the PDP-8/E:

a. Subroutines which the programmer may easily incorporate into a program for data storage, logging, data acquisition, data buffering (queuing), etc.
b. A library calling system for storing named programs on DECtape and a means of calling them with a minimal size loader.
c. System software which provides for storing, assembling, and editing of programs on DECtape, thereby greatly increasing the versatility and flexibility of the PDP-8/E.
d. Programs for preformatting tapes controlled by the content of the switch register to write the timing and mark channels, to write block formats, to exercise the tape and check for errors, and to provide each of maintenance.

Program development has resulted in a series of subroutines which read or write any number of DECtape blocks, read any number of 129-word blocks as 128 words (one memory page), or search for any block (used by read and write, or to position the tape). These programs are assembled with the user's program and are called by a JMS instruction. The program interrupt is used to detect the setting of the DECtape flag, thus allowing the main program to proceed while the DECtape operation is being completed. A program flag is set when the operation has been completed. Thus, the program effectively allows concurrent operation of several input/output devices along with operation of the DECtape system. These programs occupy two memory pages (400 (octal) = 256 (decimal) words).

The library system has the following features: First, the computer state remains unchanged when it exits. Second, the library calls programs by name from the keyboard and allows for expansion of the program file stored on the tape. Finally, the library conforms to existing system conventions, namely, that all of memory except for the last memory page (7600 (octal)—7777 (octal)) is available to the programmer. The PDP-8/E DECtape library system is loaded by a 17 (decimal)—instruction bootstrap routine that starts at address 7600 (octal). This loader calls a larger program into the last memory page, whose function is to preserve on the tape the content of memory from 6000 (octal) through 7577 (octal), and then load the INDEX program and the directory into those same locations. Since the information in this area of memory has been preserved, it can be restored when operations have been completed. The basic system tape contains the following programs:

a. INDEX: Typing this word causes the names of all programs currently on file to be typed out.

b. UPDATE: Allows the user to add a new program to the files. UPDATE queries the operator about the program's name, its starting address, and its location in core memory.

c. GETSYS: Generates a skeleton library tape on a specified DECtape unit.

d. DELETE: Causes a named file to be deleted from the tape.

Starting with the basic library tape, the user can build a complete file of his active programs and continuously update it. One of the uses of the library tape may be illustrated as follows:

The programmer may call the PDP-8/E FORTRAN compiler from the library tape and with it compile the program, obtaining the object program. The FORTRAN operating system may then be called from the library tape and used to load the object program. At this time the library program UPDATE is called, the operator defines a new program file (consisting of the FORTRAN operating system and the object program), adn adds it to the library tape. As a result, the entire operating program and the object program are now available on the DECtape library tape.

The DECtape system software is permanently stored on DECtape, from which it can be rapidly loaded. Any systems programs such as the assemblers (XPAL and XMACRO), the Symbolic Editor (XEDIT), or the Binary Loader (XLOAD), can be loaded in less than one minute.

The system software uses a standard DECtape format. There are 128 (200 (octal)) words per block and 1464 (2701(octal)) blocks, so the user has the remaining 1336 blocks for rapid access storage of his own programs.

The primary advantage for users are:

a. Efficient use of high-speed transfer rates between DECtape and core memory.

b. Symbolic programs may now be stored, edited, and assembled on DECtape, greatly increasing the versatility and flexibility of the PDP-8/E.

c. The computational workload can be more than doubled, compared to high-speed paper tape systems.

User's programs are written exactly as before for assembly by the PAL or MACRO-8 Assemblers. Using the Symbolic Editor, source programs are typed directly onto DECtape. After assembly, fast symbolic debugging can be done with DDT-8—after loading the program symbol table into DDT with the symbolic loader, XSYM.

The Binary Loader (XLOAD) can load the assembled binary program directly from the DECtape for program execution. Source files, symbol table, and program listings can be stored on DECtape and listed later, if desired. A duplicating program, XDUP, is available for copying programs.

This DECtape system also includes system calls to load any program from DECtape, to update or delete source files, and to restore the system for use by another programmer.

Although the system operates with one DECtape, a two DECtape configuration is strongly recommended as it will permit duplication of programs and saving of back-up master tapes. In a single DECtape system, if the system library is accidentally destroyed, the stored data cannot be replaced immediately because there is no means of recovery.

The last group of programs, called DECTOG, is a collection of short routines controlled by the content of the switch register. It provides for the recording of timing and mark channels and permits block formats to be recorded for any block length. Patterns may be written in these blocks and then read and checked. Writing and reading is done in both directions and checked. Specified areas of tape may be "rocked" for specified periods of time. A given reel of tape may thus be thoroughly checked before it is used for data storage. These programs may also be used for maintenance and checkout purposes.

**EXTERNAL BUS DECmagnetic Tape Options**

The DECmagtape unit can interface directly with the OMNIBUS via the TM8-E or to the External Bus via the TC58. The configurations of both categories are defined in the following table. For information on the TM8-E, refer to section 3.

**DECmagtape Configurations**

| SYSTEM OPTION | EQUIPMENT | NO. OF CHANNELS | DENSITIES (BPI) | TAPE SPEED (IPS) | OTHER INFORMATION |
|---|---|---|---|---|---|
| TM8-EA* | TM8-E Control & TU10-EA(master) | 9 | 800 | 45 | Control plugs into OMNIBUS. TU10-EA contains a master and one slave. Up to 7 additional TU10 slaves may be added. 7 and 9 track TU10's can be mixed on the same system. For example, a 7 track master can be operated with a 9 track slave etc. The master consists of logic modules which plug into the TU-10 electronics. |
| TM8-FA* | TM8-E Control & TU10-FA(master) | 7 | 800/556/200 | 45 | Same as above. |
| TC58 | TC58 Control(master) & TU10-EE(slave) | 9 | 800 | 45 | DW08A I/O conversion panel, KA8-E Positive I/O Bus and KD8-E Data Break Interface are prerequisites. The master is contained with the TC58 controller. Up to 7 additional TU10 slaves may be added. 7 and 9 track TU10's can be mixed on the same system. |
| TC58 | TC58 Control(master) & TU10-FE(slave) | 7 | 800/556/200 | 45 | Same as above. |

* Refer to Section 3 for TM8 options.

### TC58 DECmagtape System

The TC58 will control the operation of a maximum of eight digital magnetic tape transports, Types TU10, TU20 and TU30. The TC58 interfaces to and uses the KA8-E Positive I/O Bus and the KD8-E Data Break Interface.

The TC58 performs similar functions as the TM8-E. However, no master unit is required. The DECmagtape system configurations are illustrated in the following table. Refer to section 3 for a description of the TU10 DECmagtape unit.

### Operation

Transfers are governed by the in-memory WC and CA register associated with the assigned data channel (memory locations $7752_8$ and $7753_8$). Since the CA is incremented before each data transfer, its initial contents should be set to the desired initial address minus one. The WC is also incremented before each transfer and must be set to the two's complement of the desired number of data words to be transferred. In this way, the word transfer which causes the word count to overflow (WC becomes zero) is the last transfer to take place. The number of IOT instructions required for the TC58 is minimized by transferring all necessary control data (i.e., unit number, function, mode, direction, etc.) from the AC to the control using OIT instructions. Similarly, all status information (i.e., status bits, error flags, etc.) can be read into the AC from the control unit by IOT instructions.

During normal data reading, the control assembles 12-bit computer words from successive frames read from the information channels of the tape. During normal data writing, the control disassembles 12-bit words and distributes the bits so they are recorded on successive frames of the information channels.

### Programming

The commands for the magnetic tape control system are as follows:

**Skip on Error Flag or Magnetic Tape Flag (MTSF)**

| | |
|---|---|
| Octal Code: | 6701 |
| Operation: | The status of the error flag (EF) and the magnetic tape flag (MTF) are sampled. If either or both are set to 1, the content of the PC is incremented by one to skip the next sequential instruction. |
| Symbol: | If MTF or EF = 1, PC + 1 → PC |

**Skip on Tape Control Ready (MTCR)**

| | |
|---|---|
| Octal Code: | 6711 |
| Operation: | If the tape control is ready to receive a command, the PC is incremented by one to skip the next sequential instruction. |
| Symbol: | If Tape Control Ready, PC + 1 → PC |

**Skip on Tape Transport Ready (MTTR)**

| | |
|---|---|
| Octal Code: | 6721 |
| Event Time: | 1 |
| Indicators: | Iot, Fetch, Pause [IR = 6, F] |

Execution Time: 4.25 μs
Operation: The next sequential instruction is skipped if the selected tape transport is ready.
Symbol: If tape unit ready, PC + 1 → PC

**Clear Registers, Error Flag and Magnetic Tape Flag (MTAF)**

Octal Code: 6712
Event Time: 2
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Clears the status and command registers, and the EF and MTF if tape control is ready. If tape control is not ready, clears MTF and EF flags only.
Symbol: If tape control is ready, 0 → MTF, 0 → EF, 0 → command register
If tape control is not ready, 0 → MTF, 0 → EF

**Inclusive OR Contents of Command Register (MTRC)**

Octal Code: 6724
Event Time: 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Inclusively OR the contents of the command register into AC0-11.
Symbol: AC V command register → AC

**Inclusive OR Contents of Accumulator (MTCM)**

Octal Code: 6714
Event Time: 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Inclusively OR the contents of AC0-5, AC9-11 into the command register; jam transfer AC6-8 (command function).
Symbol: AC05, AC09-11 V command register → command register
AC6-8 → command register bits 6-8

**Load Command Register (MTLC)**

Octal Code: 6716
Event Time: 2, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Load the contents of AC0-11 into the command register
Symbol: AC0-11 → command register

**Inclusive OR Contents of Status Register (None)**

Octal Code: 6704
Event Time: 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs

Operation: Inclusively OR the contents of the status register into AC0-11.
Symbol: Status Register V AC → AC0-11

**Read Status Register (MTRS)**

Octal Code: 6706
Event Time: 2, 3
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Read the contents of the status register into AC0-11.
Symbol: Status Register → AC0-11

**Mag Tape "GO" (MTGO)**

Octal Code: 6722
Event Time: 2
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Set "GO" bit to execute command in the command register if command is legal.
Symbol: None

**Clear the AC (None)**

Octal Code: 6702
Event Time: 2
Indicators: Iot, Fetch, Pause [IR = 6, F]
Execution Time: 4.25 μs
Operation: Clear the accumulator.
Symbol: 0 → AC

Although any number of tapes may be simultaneously rewinding, data transfer may take place to or from only one transport at any given time. In this context, data transfer includes these functions: read or write data, write EOF (end-of-file), read/compare, and space. When any of these functions are in process, the tape control is in the not-ready condition. A transport is said to be not ready when the tape is in motion, when transport power is off, or when it is off-line.

Data transmission may take place in either parity mode; add for binary, even for BCD. When reading a record in which the number of characters is not a multiple of the number of characters per word, the final characters come into memory left-justified.

Ten bits in the magnetic tape status register retain error and tape status information. Some error types are combinations, such as lateral and longitudinal parity errors (parity checks occur after both reading and writing of data), or have a combined meaning, such as illegal command, to allow for the maximum use of the available bits.

The magnetic tape status register reflects the state of the currently selected tape unit. Interrupts may occur only for the selected unit. Therefore, other units which may be rewinding, for example, will not interrupt when done.

**Magnetic Tape Functions**

For all functions listed below, upon completion of the data operation

(after the end-of-record character passes the read head), the MTF (magnetic tape flag) is set, an interrupt occurs (if enabled), and errors are checked.

**No Operation**—NO OP command defines no function in the command register. A MTGO instruction with NO OP will cause an illegal command error (set EF).

**Space**—There are two commands for spacing records, SPACE FORWARD and SPACE REVERSE. The number of records to be spaced (two's complement) is loaded into the WC. The CA need not be set. The MTF (magnetic tape flag) is set, and an interrupt occurs at WC overflow, EOF (end of file), or EOT (end of tape), whichever occurs first. When issuing a space command, both the density and parity bits must be set to the density and parity in which the records where originally written.

Load Point or Beginning of Tape (BOT) detection during a backspace terminates the function with the BOT bit set. If a SPACE REVERSE command is given when a transport is set at BOT, the command is ignored, the illegal command error and BOT bits are set, and an interrupt occurs.

**Read Data**—Records may be read into memory only in the forward mode. Both CA and WC must be initialized CA, to the initial core address minus one; WC, to the two's complement of the number of words to be read. Both identify and parity bits must be set.

If WC is set to less than the actual record length, only the desired number of words are transferred into memory. If WC is greater than or equal to the actual record length, the entire record is read into memory. In either case, both parity checks are performed, the MTF is set, and an interrupt occurs when the end-of-record (EOR) mark passes the read head. If either lateral or longitudinal parity errors or bad tape have been detected, or an incorrect record length error occurs (WC not equal to the number of words in the record), the appropriate status bits are set. An interrupt occurs only when the MTF is set.

To continue reading without stopping tape motion, MTAF (clear MTF) and MTGO instructions must be executed. If the MTGO command is not given before the shut down delay terminates, the transport will stop.

**Write Data**—Data may be written on magnetic tape in the forward direction only. For the WRITE DATA function, the CA and WC and density and parity bits must be initialized. WRITE DATA is controlled by the WC, such that when the WC overflows, data transfer stops, and the EOR character and IRG (interrecord gap) are written. The MTF is set after the EOR has passed the read head. To continue writing, a MTGO command must be issued before the shut down delay terminates. If any errors occur, the EF will be set when the MTF is set.

A special feature of this control is the write extended interrecord gap capability. This occurs on a write operation when command register bit 5 is set. The effect is to cause a 3-inch interrecord gap to be produced before the record is written. The bit is automatically cleared when the wriitng begins. This is very useful for creating a 3-inch gap of blank tape over areas where tape performance is marginal.

**Write EOF**—The WRITE EOF command transfers a single character ($17_8$) record to magnetic tape and follows it with an EOR character. Ca and WC are ignored for WRITE EOF. The density bits must be set, and the command register parity bit should be set to even (BCD) parity. If it is set to odd parity, the control will automatically change it to even.

When the EOF marker is written, the MTF is set and an interrupt occurs. The tape transport stops, and the EOF status bit is set, confirming the writing of EOF. If odd parity is required after a WRITE EOF, it must be specifically requested through the MTLC command.

**Read/Compare**—The READ/COMPARE function compares tape data with core memory data. It can be useful for searching and positioning a magnetic tape to a specific record, such as a label or leader, whose content is known in core memory, or to check a record just written. READ/COMPARE occurs in the forward direction only; CA and WC must be set. If there is a comparison failure, incrementing of the CA ceases, and the READ/COMPARE error bit is set in the status register. Tape motion continues to the end of the record; the MTF is then set and an interrupt occurs. If there has been a READ/COMPARE error, examination of the CA reveals the word that failed to compare.

**Rewind**—The high-speed REWIND command does not require setting of the CA or WC. Density and parity settings are also ignored. The REWIND command rewinds the tape to loadpoint (BOT) and stops. Another unit may be selected after the command is issued and the rewind is in process. MTF is set, and an interrupt occurs (if the unit is selected) when the unit is ready to accept a new command. The selected unit's status can be read to determine or verify that REWIND is in progress.

**Continued Operation**

To continue operating in the same mode, the MTGO instruction is given before tape motion stops. The order of commands required for continued operation is as follows:

a. MTCM, if the command is to be changed.
b. MTAF, will only clear MTF and EF flags since tape control will be in a not ready state.
c. MTGO, if MTCM requested an illegal condition, the EF will be set at this time.

To change modes of operation, either in the same or opposite direction, the MTCM command is given to change the mode and an MTGO command is given to request the continued operation of the drive. If a change in direction is ordered, the transport will stop, pause, and automatically start up again.

*If the WRITE function is being performed, the only forward change in* command that can be given is WRITE EOF.

If no MTGO instruction is given, the transport will shut down in the interrecord gap.

**NOTE**

No flags will be set when the control becomes ready or the transport becomes ready, except if the REWIND command is present in the command register and the selected drive reaches BOT and is ready for a new command.

If a WRITE (odd parity) command is changed to WRITE EOF, the parity is automatically changed to even.

**NOTE**

Even parity will remain in the command register unless changed by a new command instruction, MTLC, which clears and loads the entire command register.

**Status or Error Conditions**

Twelve bits in the magnetic tape status register indicate status or error conditions. They are set by the control and cleared by the program.

The magnetic tape status register (STR) bits are:

| BIT* | FUNCTION (WHEN SET) |
|---|---|
| 0 | Error Flag (EF) |
| 1 | Tape rewinding |
| 2 | Beginning of tape (BOT) |
| 3 | Illegal command |
| 4 | Parity error (Lateral or Longitudinal) |
| 5 | End of file (EOF) |
| 6 | End of tape (EOT) |
| 7 | Read/compare error |
| 8 | Record length incorrect<br>WC = 0 (long)<br>WC = (short) |
| 9 | Data request late |
| 10 | Bad tape |
| 11 | Magnetic tape flag (MTF) or job done |

**MTF (STR11)**—The MTF flag is set under the following conditions:

a. Whenever the tape control has completed an operation (after the EOR mark passes the read head).

b. When the selected transport becomes ready following a normal REWIND function.

These functions will also set the EF if any errors are present.

**EOF (STR5)**—EOF is sensed and may be encountered for those functions which come under the heading of READ STATUS FUNCTION; i.e., SPACE, READ DATA, or READ/COMPARE and WRITE EOF. When EOF is

* The register bits are equivalent in position to the AC bits (i.e., STR 0 = AC 0, etc.).

encountered, the tape control sets EOF = 1. MTF is also set; hence, an interrupt* occurs and the EOF status bit may be checked.

**EOT (STR6) and BOT (STR2)**—EOT detection occurs during any forward command when the EOT reflective strip is sensed. When EOT is sensed, the EOT bit is set, but the function continues to completion. At this time the MTF is set (and EF is set), and an interrupt occurs.

BOT detection status bit occurs only when the BOT reflective strip is read on the transport that is selected.

When BOT detection occurs and the unit is in reverse, the function terminates. If a tape unit is at load point when a REVERSE command is given, an illegal command error bit is set causing an EF with BOT set. An interrupt then occurs.

**Illegal Command Error (STR3)**—The illegal command error bit is set under the following conditions:

a. A command is issued to the tape control with the control not ready.

b. A MTGO command is issued to a tape unit which is not ready, and the tape control is ready.

c. Any command (see figure 7-23) which the tape control, although ready, cannot perform; for example:

   (1) WRITE with WRITE LOCK condition

   (2) 9-channel tape and incorrect density

   (3) BOT and SPACE REVERSE

**Parity (STR4)**—Longitudinal and lateral parity checks will occur in both reading and writing. The parity bit is set for either lateral or longitudinal parity failure. A function is not interrupted, however, until MTF is set. Maintenance panel indicators are available to determine which type of parity error occurred.

**Read/Compare Error (STR7)**—When READ/COMMAND function is underway, STR7 is set to 1 for a READ/COMPARE error (see earlier portion of this section on READ/COMPARE for further details.

**Bad Tape (STR10)**—A BAD TAPE error indicates detection of a bad spot on the tape. Bad tape is defined as three or more consecutive missing characters followed by data, within the period defined by the shutdown delay. The error bit is set by the tape control when this occurs. MTF and interrupt do not occur until the end of the record in which the error was detected.

**Tape Rewinding (STR1)**—When a REWIND command has been issued to a tape unit and the function is underway, the tape rewinding bit is set in the control. This is a transport status bit, and any selected transport which is in a high-speed rewind will cause this bit to be set.

* All references to the interrupts assume the tape flags have been enables to the interrupt (command register bit 9 = 1) and that the unit is selected.

**Record Length Incorrect (STR8)**—During a READ or READ/COMPARE, this bit is set when the WC overflow differs from the number of words in the record. The EF flag is set.

**Data Request Late (STR9)**—This bit can be set whenever data transmission is in progress. When the data flag causes a data break cycle, the data must be transmitted before a write pulse or a read pulse occurs. If it does not, this error will occur, and data transmission will cease. The EF flag and bit 9 of the status register are set when the MTF is set.

**Error Flag (STR0)**—EF is set whenever any error status bit is present at the time that MTF is set. However, when an illegal command is given, the EF is set and the MTF is not set.

## Command Register Contents

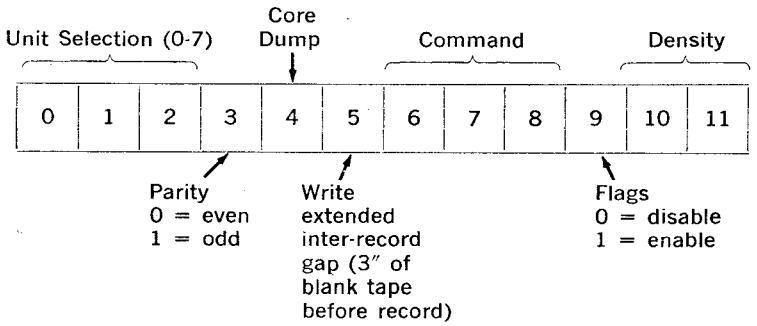



Figure 7-23

**Unit Selection**

| Unit | Unit Selection Bits 0 | 1 | 2 | Density |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 200 bpi |
| 1 | 0 | 0 | 1 | |
| 2 | 0 | 1 | 0 | 556 bpi |
| 3 | 0 | 1 | 1 | |
| 4 | 1 | 0 | 0 | 800 bpi |
| 5 | 1 | 0 | 1 | |
| 6 | 1 | 1 | 0 | 800 bpi |
| 7 | 1 | 1 | 1 | 9 channel |

| Density Selection Density | Bits |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

**Command Selection**

| COMMAND | BITS 6 | 7 | 8 |
|---|---|---|---|
| NO OP | 0 | 0 | 0 |
| Rewind | 0 | 0 | 1 |
| Read | 0 | 1 | 0 |
| Read/Compare | 0 | 1 | 1 |
| Write | 1 | 0 | 0 |
| Write EOF | 1 | 0 | 1 |
| Space Forward | 1 | 1 | 1 |
| Space Reverse | 1 | 1 | 1 |

**Magnetic Tape Function Summary**

Legend: CA = Current Address Register = 7752₈
WC = Word Count Register = 7753₈
F = Forward
R = Reverse
DS = Density Setting
PR = Parity Setting
EN = Enable Interrupt

| Function | Characteristics | Status of Error Types |
|---|---|---|
| NO-OP | CA: Ignored<br>WC: Ignored<br>DS: Ignored<br>PR: Ignored<br>EN: Ignored | Illegal<br>BOT<br>Tape Rewinding |
| SPACE FORWARD | CA: Ignored<br>WC: two's complement of number of records to skip<br>DS: Must be set<br>PR: Must be set<br>EN: Must be set | Illegal<br>EOF<br><br><br>Bad Tape<br>MTF, BOT, EOT |
| SPACE REVERSE | Same as Space Forward | Illegal<br>EOF<br>Bad Tape<br>BOT<br>MTF |

| | | |
|---|---|---|
| READ DATA | CA: Core Address —1<br>WC: two's complement of number of words to be transferred<br>DS: Must be set<br>PR: Must be set<br>EN: Must be set | Illegal<br>EOF<br>Parity<br>Bad Tape<br>MTF<br>EOT<br>Data Request Late<br>Record Length Incorrect |
| WRITE DATA | Same as READ DATA | Illegal<br>EOT<br>Parity<br>MTF<br>Bad Tape |
| WRITE EOF | CA: Ignored<br>WC: Ignored<br>DS: Must be set<br>PR: Must be set<br>EN: Must be set | Data Request Late<br>Same as WRITE DATA plus EOF |
| READ/COMPARE | Same as READ DATA | Illegal<br>EOF<br>Read/Compare Error<br>Bad Tape<br>MTF<br>EOT<br>Data Late<br>Record Length Incorrect |
| REWIND | CA: Ignored<br>WC: Ignored<br>DS: Ignored<br>PR: Ignored<br>EN: Must be set | Illegal<br>Tape Rewinding<br>MTF<br>BOT |

## DATA ACQUISITION PERIPHERALS

Digital Equipment Corporation manufactures a number of data acquisition and control subsystems designed for use with the PDP-8/E. In subsystem can be purchased initially and expanded as required. Three major analog multiplexer subsystems are available, covering analog input ranges from 10 mv to 100 V and having channel capabilities from 4 to 1024 channels. In addition, two types of Digital-to-Analog Converter subsystems are provided as options. A Universal Digital Controller subsystem is also offered as an option. This subsystem provides capabilities for controlling or interrogating up to 3072 discrete digital loads or sources.

### AD01-A 10 (or 11)-Bit Analog-to-Digital Converter

The AD01-A is a flexible, low cost, multichannel analog acquisition option for the PDP-8/E computer. The standard AD01-A consists of an expandable solid-state multiplexer, channel selection circuits for up to 32 channels, a programmable input range selector, a 10-bit A/D converter, control, and interface, and power supply. Module additions can be used to expand the multiplexer in four-channel groups up to 32 channels. (Optional 32 channel expander available).

The AD01-A interfaces with the external bus of the PDP-8/E computer to provide ten-bit digitization of unipolar analog signals having a full-scale range of 0V to +1.25V, +2.5V, +5V or +10V. An optional sign-bit addition permits eleven-bit bipolar operation. A programmable input range selection extends the dynamic range of the AD01-A (at moderate sampling rates) to an equivalent of 13 bits for unipolar inputs or to 14 bits for bipolar inputs. An optional sample and hold amplifier is also available to reduce the conversion aperture to 100 ns. Each multiplexer channel switch utilizes an enhancement mode MOSFET that is normally open when unselected, or when power is off. These switches provide overload protection for up to + or − 20V, and signal protection against short circuits.

Operation of the AD01-A is controlled by program instructions from the computer. An ADSC instruction selects the multiplexer channel, system gain, and the interrupt or noninterrupt mode as defined by an AC word.

The selected channel input is connected to the programmable-gain amplifier, which scales the analog input for a 0 to +10V output that is provided to the A/D converter summation junction, either directly or via the sample-and-hold. The ADSC instruction also clears the A/D Done Flag and initiates a conversion cycle. The conversion is performed by successive approximation. For standard unipolar AD01-A, the analog input results in a 10-bit binary output code. The sign-bit option permits conversion of bipolar inputs (0 to + or − 1.25V, + or − 2.5V, + or − 5V, or + or − 10V) to an eleven-bit, two's complement code with an extended sign format. For this format, AC bits 0 and1 are connected to the same source and denote polarity of the analog input (1 = −V, 0 = +V).

When the conversion is complete, the A/D converter sets its A/D Done Flag. This flag is sensed by an ADSF instruction and, if set, causes the next program instruction to be skipped so that the converter word can be transferred to the AC, using an ADRB instruction. The ADRB instruction also clears the A/D Done flag to ready the AD01-A for another cycle.

The above operations can also be implemented using microprogrammed IOT instructions for "best sampling" operation.

**Specifications**

| | |
|---|---|
| Resolution | Unipolar<br>10 bits, or 1 part in 1024<br>Bipolar (option)<br>sign + 10 bits |
| Converter Accuracy | ± 0.1% of 10V full-scale input<br>± 0.125% of full-scale with sample & hold |
| Quantizing Error | ± ½ least significant bit |
| Thruput Rate | 22μs including channel & gain selection unipolar; 29μs bipolar. |
| S & H Aperture | 100 ns |
| | 0.1μs with sample and hold |
| Sample & Hold Acquisition | 5μs to .01% of full-scale step change |
| No. of Analog Inputs | 4 minimum, expandable to 32 in groups of 4 Channels (64 channels available) |
| Input Impedance | 1000 megohms in parallel with 20 pf. |
| Input Isolation | Enhancement mode MOSFET switches, "off" when unselected or power off. |
| Channel Selection (program selectable) | 5-bit address |
| Input Voltage Range (program selectable) | Unipolar:<br>0 to + 1.25, +2.5, + 5.0, +10.0V full-scale<br>Bipolar (option):<br>0 to ± 1.25, ± 2.5V, ± 5.0, ± 10.0V<br>CRC and VRC (compute): 1.4 μs full-scale |
| Overload Capability | ± 20V on all ranges without damage |
| Cross Channel Attenuation | 78 db, DC-80Hz for 20 volts p-p signals, 100 ohm source impedance |
| Input Gain | Program selectable |

**Accuracy Specifications**

| Program Selected Gain | ×1 | ×2 | ×4 | ×8 | Comments |
|---|---|---|---|---|---|
| Full Scale Input | +10V | +5.0V | +2.5V | +1.25V | Selectable |
| Gain Accuracy | 0.05% | 0.05% | 0.05% | 0.05% | Unipolar<br>% of full-scale for 30 days |
| Resolution | 9.8mv | 4.9mv | 2.45mv | 1.22mv | per bit |
| Zero Drift | 550 | 300 | 175 | 110 | uv/degreeC RTI |

| | | | | | |
|---|---|---|---|---|---|
| Zero drift w/sample & hold | 750 | 400 | 225 | 140 | uv/degreeC RTI |
| | 2mv | 1mv | 1mv | 1mv | 0-0 RTI |
| Noise | | | | | |
| w/sample & hold | +−.05% | 1.2mv | 1.2mv | 1.2mv | 0-0 |
| Repeatability | 2.4mv | +−.05% | +−.05% | +−.1% | 25 degree C and 3 sigma confidence |

| | |
|---|---|
| Sign Bit | Adds one bit |
| Word Length | Control word 12 bits<br>Output word 12 bits |
| Modes of Operation | Interrupting/noninterrupting (program-selectable) |
| Environmental | 0 to + 55 degrees C operating<br>−25 degrees to + 85 degrees C storage to 90% without condensation |
| Power | 115/230V + or − 10%<br>47 to 470 Hz, single phase less than 50W |

**Programming**
The following instructions are associated with AD01A operation:

**Skip on A/D Done Flag (ADSF)**

| | |
|---|---|
| Octal Code: | 6531 |
| Execution Time: | 2.6 μs |
| Operation: | Skips the next program instruction if the A/D Done Flag is set. |

**Read A/D Buffer (ADRB)**

| | |
|---|---|
| Octal Code: | 6532 |
| Execution Time: | 2.6 μs |
| Operation: | Transfers the content of the A/D buffer to AC0 through AC11 and clears the A/D Done Flag. |

**Convert Analog Input (ADCV)**

| | |
|---|---|
| Octal Code: | 6534 |
| Execution Time: | 2.6 μs |
| Operation: | Clears the A/D Done Flag and initiates a conversion operation. |

**Select Multiplexer Channel and Gain (ADSC)**

| | |
|---|---|
| Octal Code: | 6535 |
| Execution Time: | 3.6μs |
| Operation: | Loads the content of AC into multiplexer input register and implements channel and gain selection. Also clears the A/D Done Flag and initiates a conversion. |

**Read A/D Buffer, Clear Flag and Start Conversion (ADRC)**

Octal Code: 6536
Execution Time: 3.6$\mu$s
Operation: Jam transfers content of A/D buffer to AC0-AC11, clears flag, and starts a new conversion.

**Select Channel and Gain and Read A/D Buffer (ADSR)**

Octal Code: 6537
Execution Time: 4.6$\mu$s
Operation: Transfers the content of the AC to the multiplexer input register, clears the AC, and transfers the content of the A/D buffer to the AC. The A/D Done Flag is then cleared, and another conversion is initiated.

**NOTE**

The ACRC (6536) and ADSR (6537) instructions are used for "burst sampling" conversions in the noninterrupt mode.

A program service routine for the AD01-A can be written as follows:

```
ADSC    /SELECT CHANNEL, GAIN AND MODE AND START
        /CONVERSION
ADSF    /SKIP ON A/D DONE FLAG
JMP.—1  /JUMP BACK AND TEST FLAG AGAIN
EXIT    /READ A/D BUFFER
```

**AFC8 Low-Level Analog Input Subsystem**

The AFC8 is a computer-based unit that multiplexes up to 1024 analog inputs, selects gain, and performs a 12-bit analog-to-digital conversion. Analog inputs can be provided by thermocouples or strain-gain sources having a source impedance of 0 to 500 Ω. Both channel selection and gain of the multiplexer are under control of the computer; thus, the multiplexer can handle combinations of low-level and high-level analog inputs having a range from 10 mV dc full scale to 100V full scale. Channel sampling is performed at a maximum rate of 200 channels per second. Field wiring terminates on screw terminal connectors, and requires only simple 2-wire twisted pair inputs.

Analog inputs are converted to 12-bit digital words (11 bits plus sign) for transfer to the PDP-8/E computer. Sampling of analog inputs is initiated by the computer issuing IOT instructions. Two IOT instructions are normally required for each channel sample. The first instruction defines the multiplexer gain for the channel and loads a three-bit gain

word from the AC into a multiplexer register. The second instruction defines one of 1024 possible channels for the sample and loads an 11-bit address from the AC into a register. This instruction also starts a multiplexer timing cycle, in which system gain is established, the channel is selected, and the analog output is made available to the A/D converter. When the A/D converter completes the conversion, it loads the 12-bit word into a buffer register, terminates multiplexer sampling, and sets its device flag. The computer senses the state of the device flag by issuing ADSF instructions. When the flag is set, the A/D converter returns a skip request and the computer issues an ADRB instruction to transfer the digital word to AC00 through AC11. This instruction also clears the A/D flag to ready the device for another conversion.

The subsystem is housed in 19-inch industrial type (H964) cabinets that have their own cooling and low-voltage power supplied. Four of these cabinets are required for the maximum channel capability of 1024 channels. The multiplexer is connected to the PDP-8/E computer using a Positive I/O Bus Interface module.

**Specifications**

| | |
|---|---|
| Analog Input Voltage Ranges | ± 10 mV full scale<br>± 50 mV full scale<br>±100 mV full scale<br>±200 mV full scale<br>−200 mV to + 500 mV full scale<br>−200 mV to +1 V full scale<br>−200 mV to +5 V full scale<br>−200 mV to + 10 V full scale<br>−200 mV to +100 V full scale |
| Analog Input Current Ranges | ± 1 mA full scale<br>± 5 mA full scale<br>±10 mA full scale<br>±50 mA full scale |
| A/D Converter Output Word | Parallel, 12 bits (11 bits plus sign) |
| Resolution | 5μV |
| Accuracy | ± 25μV or ±0.05% of f.s., whichever is greater |
| Common Mode Rejection | 120 dB or greater above 60 Hz |
| Common Mode Voltage | 200V |
| Normal Mode Rejection | 50 dB or greater at 60 Hz |
| System Sampling Rate | 200 channels per second (max.) |
| Single Channel Sampling Rate | 20 samples per second max. at stated accuracy |
| Expansion Capabilities | System can be expanded in groups of 8 channels up to a maximum of 1024 channels. |

| | |
|---|---|
| Internal A/D Conversion Time | 50 μs |
| Resolution | Sign + 11 bits |

**Programming**
Instructions for multiplexer operation are listed below.

**Set Multiplexer Gain (ADSG)**

| | |
|---|---|
| Octal Code: | 6542 |
| Execution Time: | 2.6 μs |
| Operation: | Loads a three-bit gain word from AC09 through 11 into a multiplexer register for selection of system gain for channel. |

**Set Multiplexer Address (ADSA)**

| | |
|---|---|
| Octal Code: | 6544 |
| Execution Time: | 2.6 μs |
| Operation: | Loads an eleven-bit address from AC01 through 11 into a multiplexer register for selection of a channel. Also starts multiplexer timing to select gain and channel and provide analog sample to A/D converter. |

**Skip on A/D Flag (ADSF)**

| | |
|---|---|
| Octal Code: | 6531 |
| Execution Time: | 2.6 μs |
| Operation: | Senses A/D converter flag. If flag is a one, increments the PC, and skips the next sequential instruction so the A/D converter can be serviced. |

**Read A/D Converter Buffer (ADRB)**

| | |
|---|---|
| Octal Code: | 6534 |
| Execution Time: | 2.6 μs |
| Operation: | Transfers twelve-bit word in A/D buffer to AC00 through AC11, and resets A/D converter flag. |

A program for selecting multiplexer gain and channel and transfer of digital word to the computer can be written as follows:

```
TAD XX
ADSG      /LOAD MULTIPLEXER GAIN WORD
CLA
TAD YY
ADSC      /LOAD MULTIPLEXER ADDRESS WORD
ADSF      /SKIP IF A/D CONVERTER FLAG IS 1
JMP .—1   /JUMP BACK AND SENSE FLAG AGAIN
```

ADRB /READ A/D BUFFER AND TRANSFER CONTENTS TO /AC00-11. CLEAR A/D CONVERTER FLAG.

**Type AF04A Guarded Scanning Integrating Digital Voltmeter**

The Type AF04A is a Guarded Scanning Integrating Digital Voltmeter system, with wide dynamic range and high common-mode rejection, and is capable of expansion to 1000 channels. The AF04A is used with the PDP-8/E to multiplex up to 1000 three-wire analog channels into a six-decimal digit integrating digital voltmeter (IDVM). Each digit is BCD-coded for input and display by the IDVM. Full scale ranges are from + or − 10 mV to + or − 300V, with automatic ranging, 300 percent overranging, and a usable 5 μs resolution. Guarded input construction and active integration assist in attaining an effective common-mode rejection of greater than 140 dB at all frequencies. (Normal mode rejection is infinite at multiples of power line-frequency.)

This system is ideally suited for data acquisition of process monitoring where a wide range of signals requires large dynamic range. The 10mV range has 0.001 percent resolution, and, coupled with a common-mode noise rejection greater than 140 dB at all frequencies, allows accurate direct measurement of thermocouples, strain gauges, load cells, and other low-level transducers without additional amplification.

The AF04A IDVM, operated under program control, is capable of either random channel selection or sequential channel selection. The computer selects either program-controlled ranging (for fastest speed) or auto-ranging, as well as the integration time of the integrating digital voltmeter.

The digitized data, as well as the current channel address, is read by the computer in either two or three bytes.

A decimal display of the digitized value, including sign and decimal location, is continuously displayed on the front panel. The current channel number is also displayed. Front-panel controls on the IDVM allow for manual setting of all the programmed functions. A front-panel control allows continuous display of the internal secondary standard, which can be prewired to a particular channel for reference checking during normal operation. The AF04A may be manually controlled, completely independent of the computer.

**Specifications**

| | |
|---|---|
| Full scale + or − | 10mV, 100mV, 1V, 10V, 100V, 300V and automatic ranging |
| Over-ranging | 300% on all but highest range |
| Maximum Input Voltage | 300V |
| Resolution | 5μV (usable), 0.1μV (LSB) |
| Accuracy (overall worst case with daily calibration) | + or − 0.004% of reading or + or − 0.01% of full scale |
| Temperature Stability (RMS full scale and zero drift) | + or − 0.006%/day |

| | |
|---|---|
| Temperature coefficient | + or − 0.003% of reading/degrees C |
| Full scale | + or − 0.002% of full scale/degrees C |
| Zero | (+ or − 0.006% of full scale/degrees C on 10mV and 1V range) |
| Line voltage stability | + or − 0.005%/10% change |
| Maximum common-mode voltage | + or − 300V from power line ground |
| Common-mode rejection (166.6ms integration period and 1000-ohm source unbalance) | >140 dB at all frequencies |
| Normal-mode rejection | Infinite at multiples of line frequency |
| Input impedance | |
| 10, 100, 1000 mV ranges | 1000 megohms/V |
| 10, 100, 300V ranges | 10 megohms |
| Internal secondary standard | |
| Value | + or − 1.000V |
| Accuracy | + or − 0.002% traceable to National Bureau of Standards |
| Stability | + or − 0.005%/month |
| Temperature coefficient | negligible |

Selected Resolution

| DC Voltage Range | 0.001% Maximum Reading | 0.001% Resolution | 0.01% Maximum Reading | 0.01% Resolution | 0.1% Maximum Reading | 0.1% Resolution |
|---|---|---|---|---|---|---|
| 10mV | 30.0000mV | 0.1μV | 030.00mV | 1μV | 0030.00mV | 10μV |
| 100mV | 300.000mV | 1μV | 0300.00mV | 10μV | 00300.0mV | 100μV |
| 1000mV | 3000.00mV | 10μV | 03000.0mV | 100μV | 003000.mV | 1mV |
| 10V | 30.0000V | 100μV | 030.000V | 1mV | 0030.00V | 10mV |
| 100V | 0300.000V | 1mV | 0300.00V | 10mV | 00300.0V | 100mV |
| 1000V* | 0300.00V | 10mV | 00300.0V | 100mV | 000300.V | 1V |

*1000V range is scanner-limited to 300V peak maximum.

Scanning Speed
(Programmed Range)

| Resolution | Integration Time | Total Time | Speed Scanning |
|---|---|---|---|
| 0.1% | 1.6 ms | 20 ms | 50 ch/s |
| 0.01% | 16.6 ms | 40 ms | 25 ch/s |
| 0.001% | 166.6 ms | 188 ms | 5 ch/s |

Scanning Speed (Auto-Range)—Add 6-36 ms, depending on per-channel voltage span.

**Programming**

The IOT instructions associated with the scanning IDVM are designed to minimize the computer overhead associated with this option, while retaining maximum program controlled flexibility. The IOT instructions are:

**Select Range and Gate (VSEL)**

Octal Code: 6542
Execution Time: 2.6 μs
Operation: Transfers the contents of the accumulator to the AF04A control register. Control Word 1 is used only if a range change is required (see Figure 7-17).

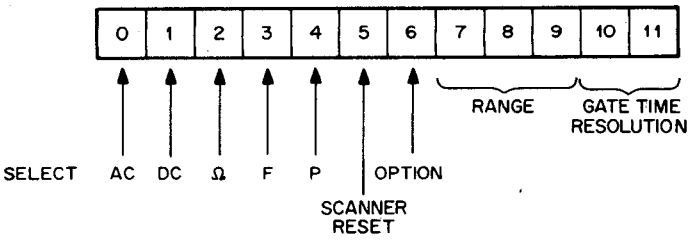



Figure 7-24 Control Word 1 (from Computer)

**Select Channel and Convert (VCNV)**

Octal Code: 6541
Execution Time: 2.6 μs
Operation: Transfers the contents of the accumulator to the AF04A channel address register. Automatically digitizes the analog signal on the selected channel (see Figure 7-18).

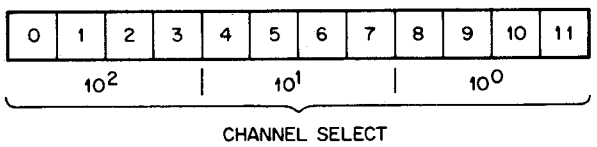



Figure 7-25 Control Word 2 (from Computer)

**Index Channel and Convert (VINX)**

Octal Code: 6544
*Execution Time:* 2.6 μs
Operation: Increments the last channel address by one and automatically digitizes the analog signal on the selected channel. The contents of the control register are unchanged.