Design in common for the R4200 (VRX), R4600 (Orion), R4000PC and R4400PC

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This document is intended to guide system designers who wish to do a single system design which can be used with either the R4200 or R4600 processor.

This would allow a system manufacturer to produce two different systems at different price/performance points from a single design.

This is possible designing for either the 208-pin QFP package of R4200 and R4600, or the 179-pin PGA package of each. In the case of choosing the 179-pin package, the R4000PC and R4400PC processors will expand the choice and range of systems manufacturable from the single design even further.

It is not intended that R4200 / R4600 CPU's would be interchangeable by the user in such a design.

This document addresses the following differences which may be significant to system designers:

1/ R4200 and R4600 pin-out (208-pin QFP package)
2/ R4200, R4600, R4000PC and R4400PC pin-out (179-pin PGA package)
3/ Primary cache differences (R4000PC, R4200, R4600 and R4400PC)
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11/ System Interface parameters ""

1/ 208-pin QFP package

R4200 and R4600 signals are the same where I/O is concerned but different in the areas of processor configuration and initialization.

The majority of pins have an identical function. Those that have a difference are marked with a note. Where possible, conflicting functions were overlapped with NoConnects on the other processor. There are 16 such cases marked Note 1 & 2.

In a few cases, functionally different pins were aligned such that inputs overlap inputs and outputs overlap outputs. Most of these cases can be dealt with trivially, ignoring optional or unused functionality. For the remaining 2 or 3 pins (depends on settings of configuration pins on R4200), it may be necessary either to have jumpers which can be set, or dual traces, one of which would filled at system manufacture time.

Overlapping functionally different pins are marked Note 3 through Note 10.

	R4200	R4600	
	=====	=====	
1	NC	NC	
2	NC	NC	
3	VSS	VSS	
4	VCC	VCC	
5	SysAD45	SysAD45	
6	SysAD13	SysAD13	
7	Status0	FaultB	Note 3
8	SysAD44	SysAD44	
9	VSSCore	VSS	
10	VCCCore	VCC	
11	SysAD12	SysAD12	
12	SysCmdP	SysCmdP	
13	SysAD43	SysAD43	
14	SysAD11	SysAD11	
15	VSS	VSS	
16	VCC	VCC	
17	SysCmd8	SysCmd8	
18	SysAD42	SysAD42	
19	SysAD10	SysAD10	
20	SysCmd7	SysCmd7	
21	VSS	VSS	
22	VCC	VCC	
23	SysAD41	SysAD41	
24	SysAD9	SysAD9	
25	SysCmd6	SysCmd6	
26	SysAD40	SysAD40	
27	VSSCore	NC	Note 1
28	VCCCore	NC	Note 1
29	VSS	VSS	
30	VCC	VCC	
31	SysAD8	SysAD8	
32	SysCmd5	SysCmd5	
33	SysADC4	SysADC4	
34	SysADC0	SysADC0	
35	VSS	VSS	
36	VCC	VCC	
37	SysCmd4	SysCmd4	
38	SysAD39	SysAD39	
39	SysAD7	SysAD7	
40	SysCmd3	SysCmd3	
41	VSS	VSS	
42	VCC	VCC	
43	SysAD38	SysAD38	
44	SysAD6	SysAD6	
45	Status1	ModeClock	Note 4
46	WrRdyB	WrRdyB	
47	SysAD37	SysAD37	
48	SysAD5	SysAD5	
49	VSS	VSS	
50	VCC	VCC	
51	NC	NC	
52	NC	NC	

	R4200	R4600	
	=====	=====	
53	NC	NC	
54	NC	NC	
55	SysCmd2	SysCmd2	
56	SysAD36	SysAD36	
57	SysAD4	SysAD4	
58	SysCmd1	SysCmd1	
59	VSS	VSS	
60	VCC	VCC	
61	SysAD35	SysAD35	
62	SysAD3	SysAD3	
63	SysCmd0	SysCmd0	
64	SysAD34	SysAD34	
65	VSS	VSS	
66	VCC	VCC	
67	VSSCore	NC	Note 1
68	VCCCore	NC	Note 1
69	SysAD2	SysAD2	
70	NC	IntB5	Note 2
71	SysAD33	SysAD33	
72	SysAD1	SysAD1	
73	VSS	VSS	
74	VCC	VCC	
75	IntB4	IntB4	
76	SysAD32	SysAD32	
77	SysAD0	SysAD0	
78	IntB3	IntB3	
79	VSSCore	VSS	
80	VCCCore	VCC	
81	IntB2	IntB2	
82	SysAD16	SysAD16	
83	SysAD48	SysAD48	
84	IntB1	IntB1	
85	VSS	VSS	
86	VCC	VCC	
87	SysAD17	SysAD17	
88	SysAD49	SysAD49	
89	IntB0	IntB0	
90	SysAD18	SysAD18	
91	VSS	VSS	
92	VCC	VCC	
93	SysAD50	SysAD50	
94	ValidInB	ValidInB	
95	SysAD19	SysAD19	
96	SysAD51	SysAD51	
97	VSS	VSS	
98	VCC	VCC	
99	ValidOutB	ValidOutB	
100	SysAD20	SysAD20	
101	SysAD52	SysAD52	
102	ExtRqstB	ExtRqstB	
103	NC	NC	
104	NC	NC	

	R4200	R4600	
	=====	=====	
105	NC	NC	
106	NC	NC	
107	VCCCore	NC	Note 1
108	VSSCore	NC	Note 1
109	VCC	VCC	
110	VSS	VSS	
111	SysAD21	SysAD21	
112	SysAD53	SysAD53	
113	RdRdyB	RdRdyB	
114	BigEndian	ModeIn	Note 5
115	SysAD22	SysAD22	
116	SysAD54	SysAD54	
117	VCC	VCC	
118	VSS	VSS	
119	ReleaseB	ReleaseB	
120	SysAD23	SysAD23	
121	SysAD55	SysAD55	
122	NMIB	NMIB	
123	VCCCore	VCC	
124	VSSCore	VSS	
125	SysADC2	SysADC2	
126	SysADC6	SysADC6	
127	DataRateB	VCC	Note 6
128	SysAD24	SysAD24	
129	VSS	VSS	
130	VCC	VCC	
131	SysAD56	SysAD56	
132	Status3	NC	Note 1
133	SysAD25	SysAD25	
134	SysAD57	SysAD57	
135	VCCCore	VCC	
136	VSSCore	VSS	
137	Status2	IOOut	Note 7
138	SysAD26	SysAD26	
139	SysAD58	SysAD58	
140	TestModeB	IOIn	Note 8
141	VCC	VCC	
142	VSS	VSS	
143	SysAD27	SysAD27	
144	SysAD59	SysAD59	
145	ColdResetB	ColdResetB	
146	SysAD28	SysAD28	
147	VCC	VCC	
148	VSS	VSS	
149	SysAD60	SysAD60	
150	ResetB	ResetB	
151	SysAD29	SysAD29	
152	SysAD61	SysAD61	
153	VCC	VCC	
154	VSS	VSS	
155	NC	NC	
156	NC	NC	

	R4200	R4600	
	=====	=====	
157	NC	NC	
158	NC	NC	
159	VSS	RClock0	Note 9
160	RClock	RClock1	
161	SyncOut	SyncOut	
162	SysAD30	SysAD30	
163	VCC	VCC	
164	VSS	VSS	
165	SysAD62	SysAD62	
166	MasterOut	MasterOut	
167	SysAD31	SysAD31	
168	SysAD63	SysAD63	
169	VCCCore	VCC	
170	VSSCore	VSS	
171	Div2	VccOK	Note 10
172	SysADC3	SysADC3	
173	SysADC7	SysADC7	
174	VCC	VCC	
175	VSS	VSS	
176	BypassPLLB	NC	Note 1
177	VCCP	NC	Note 1
178	VSSP	NC	Note 1
179	PLLCap0	NC	Note 1
180	PLLCap1	NC	Note 1
181	VCCP	VCCP	
182	VSSP	VSSP	
183	VCCP	NC	Note 1
184	VSSP	NC	Note 1
185	MasterClock	MasterClock	
186	VCCCore	VCC	
187	VSSCore	VSS	
188	Syncin	Syncin	
189	VCC	VCC	
190	VSS	VSS	
191	JTCK	JTCK	
192	SysADC5	SysADC5	
193	SysADC1	SysADC1	
194	JTDI	JTDI	
195	VCCCore	VCC	
196	VSSCore	VSS	
197	SysAD47	SysAD47	
198	SysAD15	SysAD15	
199	JTDO	JTDO	
200	SysAD46	SysAD46	
201	VCC	VCC	
202	VSS	VSS	
203	SysAD14	SysAD14	
204	JTMS	JTMS	
205	TClock	TClock0	
206	NC	TClock1	Note 2
207	NC	NC	
208	NC	NC	

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A number of pins on each package are there for purposes such as testing, R4000PC compatibility, reserved for future use, or for optional use. As a result, there are a number of ways of handling these pins, the simplest being to tie them to VCC, VSS, or NoConnect.

Note 1:
The system design must implement the function intended in the R4200 design for this pin. R4600 has a NoConnect at this pin.

```
(Relevant R4200 pins:     Pin 27  VSSCore
                          Pin 28  VCCCore
                          Pin 67  VSSCore
                          Pin 68  VCCCore
                          Pin 107 VSSCore
                          Pin 108 VCCCore
                          Pin 132 Status3
                          Pin 176 BypassPLLB
                          Pin 177 VCCP
                          Pin 178 VSSP
                          Pin 179 PLLCap0
                          Pin 180 PLLCap1
                          Pin 183 VCCP
                          Pin 184 VSSP)
```

Status3 on R4200 is optional; BypassPLLB will be tied to VCC in normal use.

Note 2:
The system design may implement the function intended in the R4600 design for this pin. R4200 has a NoConnect at these pins. It is recommended to make TClock1 a NoConnect and IntB5 tied to 0).

```
(Relevant R4600 pins: Pin 70  IntB5
                      Pin 206 TClock1)
```

The common board design will use only one RClock-TClock pair. This will be Pin 160 (RClock), Pin 205 (TClock).

Note 3:
Pin 7, Status0 (R4200) and FaultB (R4600) are both output pins.It is suggested that each be made a NoConnect. FaultB on R4600 exists primarily for compatibility with the R4000 and is not normally used in current designs. Monitoring the status pins on the R4200 is not required.

Note 4:
Pin 45, Status1 (R4200) and ModeClock (R4600) are both output pins. It is suggested that Status1 on the R4200 be made a NoConnect. Otherwise, implement system functionality for both and use jumpers or dual traces to select for one design of the other.

Note 5:
Pin 114, BigEndian (R4200) and ModeIn (R4600) are both input pins. Implement system functionality for both and use jumpers or dual traces to select for one design of the other.

Note 6:
Pin 127, DataRateB (R4200) and VCC (R4600) are both input pins.
Make Vcc default input, using a jumper if necessary to set DatarateB to active low.

Note 7:
Pin 137, Status2 (R4200) and IOOut (R4600) are both output pins.
It is suggested that this be made a NoConnect.
If status pins on R4200 are implemented, ignore value in logic when R4600 is plugged in.

Note 8:
Pin 140, TestModeB (R4200) and IOIn (R4600) are both input pins.
It is suggested that this pin be tied to VCC.
In the R4200, this pin is reserved for cache test mode and should be tied to Vcc during normal operation.

Note 9:
Pin 159, Vss (R4200) is an input power ground pin and RClock0 (R4600)
is an output pin. It is recommended to tie this pin position to VSS and clip off Pin 159 on the R4600 package.
The common board design will use only one RClock-TClock pair.
This will be Pin 160 (RClock), Pin 205 (TClock).

Note 10:
Pin 171, Div2 (R4200) and VccOK (R4600) are both input pins.
Div2 functionality is reserved until further notice - for the R4200, the default is to have the pin tied high (VCC).
This effectively means that it is sufficient to implement the functionality for VccOK only for this pin.

2/ 179-pin PGA package

For the 179-pin package, the R4000PC is the compatibility reference. R4200 and R4600 signals are the same where I/O is concerned but different in the areas of processor configuration and initialization.

It is possible to do a common design to accomodate either R4200 or R4600 processors without the use of any jumpers.

The majority of pins have an identical function. Those that have a difference are marked with a note. Where possible, conflicting functions were overlapped with NoConnects on the other processor. There are 6 such cases marked Note 1.

In a few cases, functionally different pins were aligned such that inputs overlap inputs and outputs overlap outputs. These cases can be dealt with trivially, ignoring optional or unused functionality.

Overlapping, functionally different pins are marked Note 2 through Note 6.

	R4200	R4600	
	=====	=====	
A1	No pin	No pin	
A2	Vcc	Vcc	
A3	Vss	Vss	
A4	Vcc	Vcc	
A5	SysCmd3	SysCmd3	
A6	Vss	Vss	
A7	Vcc	Vcc	
A8	Vss	Vss	
A9	Vcc	Vcc	
A10	Vss	Vss	
A11	Vcc	Vcc	
A12	Vss	Vss	
A13	Vcc	Vcc	
A14	Vss	Vss	
A15	SysAD43	SysAD43	
A16	Vcc	Vcc	
A17	Vss	Vss	
A18	Vss	Vss	
B1	Vss	Vss	
B2	SysCmd2	SysCmd2	
B3	SysAD37	SysAD37	
B4	N/C	Modeclock	Note 1
B5	SysAD6	SysAD6	
B6	SysAD7	SysAD7	
B7	SysCmd4	SysCmd4	
B8	SysADC4	SysADC4	
B9	SysAD8	SysAD8	
B10	SysCmd6	SysCmd6	
B11	SysAD9	SysAD9	
B12	SysCmd7	SysCmd7	
B13	SysAD42	SysAD42	
B14	SysAD11	SysAD11	
B15	SysAD12	SysAD12	
B16	DatarateB	FaultB	Note 2
B17	SysAD45	SysAD45	
B18	Vcc	Vcc	
C1	Vcc	Vcc	
C2	SysAD4	SysAD4	
C3	SysAD36	SysAD36	
C4	SysAD5	SysAD5	
C5	WrRdyB	WrRdyB	
C6	SysAD38	SysAD38	
C7	SysAD39	SysAD39	
C8	SysADC0	SysADC0	
C9	SysCmd5	SysCmd9	
C10	SysAD40	SysAD40	
C11	SysAD41	SysAD41	
C12	SysAD10	SysAD10	
C13	SysCmd8	SysCmd8	
C14	SysCmdP	SysCmdP	
C15	SysAD44	SysAD44	

	R4200	R4600	
	=====	=====	
C16	SysAD13	SysAD13	
C17	TClock0	TClock0	
C18	Vss	Vss	
D1	Vss	Vss	
D2	SysAD35	SysAD35	
D3	SysCmd1	SysCmd1	
D16	TClock1	TClock1	
D17	SysAD14	SysAD14	
D18	Vcc	Vcc	
E1	SysAD2	SysAD2	
E2	SysCmd0	SysCmd0	
E3	SysAD3	SysAD3	
E16	JTMS	JTMS	
E17	SysAD46	SysAD46	
E18	SysAD15	SysAD15	
F1	Vcc	Vcc	
F2	N/C	Int5	Note 1
F3	SysAD34	SysAD34	
F16	JTDO	JTDO	
F17	SysAD47	SysAD47	
F18	Vss	Vss	
G1	Vss	Vss	
G2	SysAD1	SysAD1	
G3	SysAD33	SysAD33	
G16	JTDI	JTDI	
G17	SysADC1	SysADC1	
G18	Div2	Vcc	Note 3
H1	Vcc	Vcc	
H2	SysAD32	SysAD32	
H3	IntB4	IntB4	
H16	SysADC5	SysADC5	
H17	JTCK	JTCK	
H18	Vss	Vss	
J1	Vss	Vss	
J2	SysAD0	SysAD0	
J3	IntB3	IntB3	
J16	SyncIn	SyncIn	
J17	MasterClock	MasterClock	
J18	Vcc	Vcc	
K1	Vcc	Vcc	
K2	SysAD16	SysAD16	
K3	IntB2	IntB2	
K16	VssP	VssP	
K17	VccP	VccP	
K18	Vss	Vss	
L1	Vss	Vss	
L2	SysAD48	SysAD48	
L3	IntB1	IntB1	
L16	SysADC3	SysADC3	
L17	SysADC7	SysADC7	
L18	Vcc	Vcc	

	R4200	R4600	
	=====	=====	
M1	Vcc	Vcc	
M2	SysAD17	SysAD17	
M3	SysAD49	SysAD49	
M16	SysAD31	SysAD31	
M17	BypassPLLB	VccOk	Note 4
M18	Vss	Vss	
N1	Vss	Vss	
N2	IntB0	IntB0	
N3	SysAD50	SysAD50	
N16	SysAD62	SysAD62	
N17	SysAD63	SysAD63	
N18	Vcc	Vcc	
P1	SysAD18	SysAD18	
P2	ValidInB	ValidInB	
P3	SysAD19	SysAD19	
P16	SyncOut	SyncOut	
P17	MasterOut	MasterOut	
P18	Vss	Vss	
R1	Vcc	Vcc	
R2	SysAD51	SysAD52	
R3	ValidOutB	ValidOut	
R16	RClock1	RClock1	
R17	SysAD30	SysAD30	
R18	Vss	Vss	
T1	Vss	Vss	
T2	SysAD20	SysAD20	
T3	SysAD52	SysAD52	
T4	SysAD21	SysAD21	
T5	RdRdyB	RdRdyB	
T6	SysAD54	SysAD54	
T7	SysAD55	SysAD55	
T8	SysADC2	SysADC2	
T9	N/C	Reserved I(Vcc)	Note 1
T10	SysAD56	SysAD56	
T11	SysAD57	SysAD57	
T12	SysAD26	SysAD26	
T13	N/C	IOIn	Note 1
T14	ColdResetB	ColdrestB	
T15	SysAD60	SysAD60	
T16	SysAD29	SysAD29	
T17	RClock0	RClock0	
T18	Vcc	Vcc	
U1	Vcc	Vcc	
U2	ExtRqstB	ExtRqstB	
U3	SysAD53	SysAD53	
U4	N/C	ModeIn	Note 1
U5	SysAD22	SysAD22	
U6	SysAD23	SysAD23	
U7	NMIB	NMIB	
U8	SysADC6	SysADC6	
U9	SysAD24	SysAD24	

	R4200	R4600	
	=====	=====	
U10	BigEndian	Reserved (o)N/C	Note 5
U11	SysAD25	SysAD25	
U12	N/C	IOOut	Note 1
U13	SysAD58	SysAD58	
U14	SysAD27	SysAD27	
U15	SysAD28	SysAD28	
U16	ResetB	ResetB	
U17	SysAD61	SysAD61	
U18	Vss	Vss	
V1	Vss	Vss	
V2	Vss	Vss	
V3	Vcc	Vcc	
V4	Vss	Vss	
V5	ReleaseB	ReleaseB	
V6	Vcc	Vcc	
V7	Vss	Vss	
V8	Vcc	Vcc	
V9	Vss	Vss	
V10	Vcc	Vcc	
V11	Vss	Vss	
V12	Vcc	Vcc	
V13	Vss	Vss	
V14	TestModeB	Vcc	Note 6
V15	SysAD59	SysAD59	
V16	Vss	Vss	
V17	Vcc	Vcc	
V18	Vss	Vss	

Notes to 179-pin package Pin Assignments:
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A number of pins on each package are there for purposes such as testing, R4000PC compatibility, reserved for future use, or for optional use. As a result, there are a number of ways of handling these pins, the simplest being to to tie them to VCC, VSS, or NoConnect.

Note 1:
The system design must implement the function intended in the R4600 design for these pins. R4200 has a NoConnect at these pins.

(Relevant R4600 pins: Pin B4 ModeClock
Pin F2 Int5
Pin T9 Reserved I (VCC)
Pin T13 IOIn
Pin U4 ModeIn
Pin U12 IOOut)

(It is optional to actually use Int5; IOOut is frequently connected directly to IOIn for a trivial fix).

Note 2:
Pin B16, DatarateB (R4200) is an input pin and FaultB (R4600) is an output pin. It is recommended to make FaultB a NoConnect, perhaps by removing the pin on the R4600 processor.

Note 3:
Pin G18, Div2 (R4200) functionality is reserved until further notice - for normal use this pin should be tied to Vcc. This makes it the same as the R4600 pin.

Note 4:
Pin M17, BypassPLLB (R4200) and VccOk (R4600) are both input pins. Since BypassPLLB will be set high for normal PLL use in the R4200, the VccOk functionality for R4600 should be implemented at this pin.

Note 5:
Pin U10, BigEndian (R4200) is an input pin and Reserved(o) N/C is specified as an output pin. It is recommended to tie this pin to BigEndian setting and make Reserved(o) a NoConnect, perhaps by removing the pin on the R4600 processor.

Note 6:
Pin V14, TestModeB (R4200) functionality is reserved for cache test purposes - for normal use this pin should be tied to Vcc. This makes it the same as the R4600 pin.

3/ Primary cache differences

	R4000PC	R4200	R4600	R4400PC
Cache sizes:	8KB I-cache 8KB D-cache	16KB I-cache 8KB D-cache	16KB I-cache 16KB D-cache	16KB I-cache 16KB D-cache
Cache Line size:	Software selectable between 16B and 32B	32B I-cache 16B D-cache	32B	Software selectable between 16B and 32B
Cache organization:	Direct mapped	Direct mapped	2-way set associative	Direct mapped
Cache index:	vAddr12..0	vAddr13..0(I) vAddr12..0(D)	vAddr12..0	vAddr13..0
Cache tag:	pAddr35..12	pAddr32..12	pAddr35..12	pAddr35..12
Data cache write policy:	Write-allocate & write-back	Write-allocate & write-back	Write-allocate or not based on TLB entry Write-through or not based on TLB entry	Write-allocate & write-back
Data cache miss:	Stall, output address, copy dirty data to writeback buffer, refill cache, output writeback data.	Same	Same (refill set chosen by FIFO algorithm)	Same (as R4000)
Data order for block reads:	Sub-block ordering	Sub-block ordering (trivial because only two)	Sub-block ordering	Sub-block ordering
Data order for block writes:	Sequential	Same	Same	Same
Instruction cache miss restart;	Restart after all data received and written to cache	Same	Same	Same

	R4000PC	R4200	R4600	R4400
	========	======	======	======
Data cache miss restart	Restart after all data received and written to cache	Early restart on first doubleword.	Restart on first doubleword, send subsequent doublewords to response buffer	Same as R4000
Instruction tag:	2-bit cache state	2-bit cache state	1-bit cache state	2-bit cache state
Cache miss overhead:	5-8? cycles	TBD	3 cycles	5-8? cycles
Instruction cache parity:	1 parity bit per 8 data bits	1 parity bit per 8 data bits	1 parity bit per 32 data bits	1 parity bit per 8 data bits
Data cache parity:	1 parity bit per 8 data bits	Same	Same	Same

4/ TLB differences

	R4000PC	R4200	R4600	R4400PC
Instruction virtual address translation:	2-entry I-TLB	2-entry I-TLB	2-entry I-TLB	2-entry I-TLB
JTLB:	48 entries of even/odd page pairs, fully associative	32 entries of even/odd page pairs, fully associative	48 entries of even/odd page pairs, fully associative	48 entries of even/odd pairs, fully associative
Page size:	4KB, 16KB, 64KB, 256KB, 1MB, 4MB, 16MB	4KB, 16MB	4KB, 16KB, 64KB, 256KB, 1MB, 4MB, 16MB	4KB, 16KB, 64KB, 256KB, 1MB, 4MB, 16MB
Multiple entry match in JTLB:	sets TS in Status and disables TLB until Reset to prevent damage	Same as R4000	No damage for multiple match; no detection or shutdown implemented	Same as R4000
Virtual address size:	VSIZE = 40 PSIZE = 36	VSIZE = 40 PSIZE = 33	VSIZE = 40 PSIZE = 36	VSIZE = 40 PSIZE = 36

/ Pipeline comparisons

	R4000PC	R4200	R4600	R4400PC
CPU/FPU:	Logically and physically separate	Logically separate; datapath shared	Logically and physically separate but with some cross-use	Logically and physically separate
ALU latency:	1 cycle	1 cycle	1 cycle	1 cycle
Load latency:	3 cycles	2 cycles	2 cycles	3 cycles
Branch latency:	4 cycles	2 cycles	2 cycles	4 cycles
Store buffer:	2 doublewords	1 doubleword	1 doubleword	2 doublewords
Uncached store buffer:	None	2 doublewords (1 address) - doubles as write buffer	4 doublewords (4 addresses) - doubles as write buffer	1 doubleword

N.B. Store buffer refers to buffer for writes from pipeline to cache.
Write buffer refers to buffer for writes from cache to external memory.
Uncached store buffer refers to buffer for writes from pipeline to external memory.

	R4000PC	R4200	R4600	R4400PC
Integer multiply:	Integer multiply hardware, 1 cycle to issue	done in adder/shifter, 12 cycles to issue	commondone in floating-point multiplier, 4 cycles to issue	Integer multiply hardware, 1 cycle to issue
Integer divide:	Done in integer datapath adder, 69 cycles to issue.	done in common adder/shifter, 36 cycles to issue.	done in floating-point adder, 4 cycles to issue	done in integer datapath adder, 69 cycles to issue.

N.B. It's important to appreciate the difference between cycles to issue, and cycles to completion. For example, the R4000PC can issue an integer multiply in one cycle and issue a subsequent instruction in the next cycle. However that multiply does not complete until 10 cycles later. An integer divide on the other hand, causes subsequent instructions in the pipeline to slip resulting in a high issue latency.

	R4000PC	R4200	R4600	R4400PC
Integer multiply:	HI and LO available at the same time	N/A since no new instructions are issued before multiply completes	LO available one cycle before HI	HI and LO available at the same time
Integer divide:	HI and LO available at the same time	N/A since no new instructions are issued before divide completes	HI available one cycle before LO	HI and LO available at the same time
HI and LO hazards:	Yes, HI and LO written early in pipeline	Yes, at least a one-cycle hazard. Assume two-cycle hazard (same as R4000PC) until further notice.	No, HI and LO written after W	Yes, HI and LO written early in pipeline
MFHI/MFLO latency:	1 cycle	1 cycle	2 cycles	1 cycle
SLLV, SRLV SRAV:	2 cycles	1 cycle	1 cycle	2 cycles
DSLL, DSRL, DSRA, DSLL32, DSRL32, DSRA32, DSLLV, DSRLV, DSRAC:	2 cycles	1 cycle	1 cycle	2 cycles

6/ System interface comparisons

	R4000PC	R4200	R4600	R4400PC
I/O:		LVCMOS (3.3V+/-0.3V)	R4600(3V) LVCMOS (3.3V+/-0.3V)	R4400(3V) LVCMOS (3.3V+/-0.3V)
	TTL-compatible (5V+/-0.5V)		R4600(5V) TTL-compatible (5V+/-0.5V)	R4400(5V) TTL-compatible (5V+/-0.5V)
Package:	179-pin C-PGA	179-pin C-PGA	179-pin C-PGA	179-pin C-PGA
		208-pin PQFP	208-pin MQUAD	
JTAG	Yes	Yes	No	Yes
Block transfer sizes:	16B or 32B	16B (D) 32B (I)	32B	16B or 32B
Sclock divisor:	2,3 or 4	2 or 4	2 (3-8 later)	2,3,4,6 or 8
Non-block writes:	max throughput of 1 per 4 sclock cycles	max throughput of 1 per 4 sclock cycles	two new system interface protocol options that also support 2 sclock cycle throughput	max throughput of 1 per 4 sclock cycles
Serial configuration:	As described in R4000 User's Guide	Four configuration options hardwired through dedicated pins	As described in R4600 Advance Information (different to R4000PC)	As described in R4000 User's Guide
Address bits 63...56 on reads and writes:	zero	zero	bits 19...12 of virtual address	zero

	R4000PC	R4200	R4600	R4400PC
Uncached and write-through stores:	Uncached stores stall until sent on system interface (write-through not possible)	Uncached stores buffered in 1-entry write buffer (write-through not possible)	Uncached and write-through stores buffered in 4-entry write buffer	Uncached stores buffered in 1-entry dedicated uncached store buffer (write-through not possible)
SysADC	Parity	Parity	Parity	Parity
SysADC for non-data cycles:	Zero	Parity	Zero	Parity
Parity Error during writeback:	Use Cache Error exception	Use Cache Error exception	output bad parity	Use cache Error exception
Error bit in data identifier of read responses:	Bus error if error bit set for any doubleword	Bus error if error bit set for any doubleword	Only check error bit of first doubleword; all other error bits are ignored.	Bus error if error bit set for any doubleword
Parity error on read data:	Bus Error if parity error in any doubleword	Take Cache error exception	Bad parity written to cache; take Cache Error exception if bad parity occurs on doublewords that the processor is waiting for.	Bus Error if parity error in any doubleword
Block writes	1-2 null cycles between address and data	0 cycles between address and data	0 cycles between address and data	1-2 null cycles between address and data
Release after read request:	Variable latency	0 latency	0 latency	Variable latency

	R4000PC	R4200	R4600	R4400PC
SysAD value for x cycles of writeback data pattern:	Data bus undefined	Data bus maintains last D cycle value	data bus maintains last D cycle value	Data bus undefined
SysAD bus use after last D cycle of writeback:	?	Unused for trailing x cycles (e.g. DxxDxx)	Unused for trailing x cycles (e.g. DDxxDDxx)	?
Output slew rate:	Dynamic feedback control	None	Simple CMOS output buffers with 2-bit static strength control	Dynamic feedback control
IOOut output	output slew rate control feedback loop output	No pin	Driven high,do not connect reserved for future output)	Output slew rate control feedback loop output
IOIn input	output slew rate control input	No pin	Should be driven high (reserved for future input)	output slew rate control input
GrpRunB output:	do not connect	No pin	do not connect	do not connect
GrpStallB input:	Should be connected to Vcc	No pin	Should be connected to Vcc	Should be connected to Vcc
FaultB output:	Indicates compare mismatch	No pin	Driven high, do not connect (reserved for future outout)	Indicates compare mismatch

7/ Coprocesssor 0 comparisons

	R4000PC	R4200PC	R4600	R4400PC
WatchLo, WatchHi:	Implemented	Implemented	Unimplemented	Implemented
Config:	As described in R4000 User's Guide	Subset	Subset	As described in R4000 User's Guide
Status:	As described in R4000 User's Guide, but RP not functional	As described in R4000 User's Guide, RP functional and new ITS bit	No TS or RP	As described in R4000 User's Guide, but RP not functional
Low-power mode:	No	1)Reduced-power mode (1/4 speed) 2)Instant-off mode	WAIT instruction disables internal clock, freezing pipeline and other state; resume on interupt	No
MFC0/MTC0 hazard:	Only hazardous for certain cp0 register combinations	Only hazardous for a subset of the R4000PC cp0 register combinations	Always hazardous - detected and 1-cycle slip inserted	Only hazardous for certain cp0 register combinations
EntryLo0, EntryLo1:	As described in MIPS R-series architecture	As described in MIPS R-series architecture	Two new cache algorithms added to C field for non-coherent write-through	As described in MIPS R-series architecture
TagLo, TagHi, ECC, Cacherr:	R4000SC bits implemented but meaningless	Only bits meaningful on R4000PC implemented	Only bits meaningful on R4000PC implemented	R4400SC bits implemented but meaningless

	R4000PC	R4200	R4600	R4400
TagLo:	As described in MIPS R-series architecture	Bits 31..29 defined as zero since physical address size is 3 bits shorter than R4000PC	Bits 5...3 used for reserved bits ITag28..25 bit 2 used for F bit.	As described in MIPS R-series architecture
Exceptions:	As described in MIPS R-series architecture (VCEI and VCED not possible in R4000PC)	As R4000PC but different order of priority	VCEI, VCED and WATCH exceptions not implmented	As described in MIPS R-series architecture (VCEI and VCED not possible in R4400PC)
Index CACHE ops:	Use vAddr12...4 to select line	Use vAddr13...4 (I-cache) vAddr12...3 (D-cache) to select line	Use vAddr13 to select set, vAddr12...5 to select line of set	Use vAddr13...4 to select line
Index Store Tag CACHE op:	Status.CE ignored	TagLo.P stored if Status.CE set	TagLo.P stored if Status.CE set	Status.CE ignored
PRId	Imp=0x04	Imp=0x0A	Imp=0x20	Imp=0x04

8/ Maximum ratings (spec'd not measured)

N.B. The ratings given below are for comparison purposes only. Please consult the full specifications for complete information, conditions under which these figures are considered valid, etc.

	R4200	R4600(3V)
Supply voltage(VCC):		
(min.)	3.0V	3.0V
(max.)	3.6V	3.6V
Terminal voltage w.r.t. ground (Vterm):		-0.5 to 4.6V
Input voltage(VIN):		
(min.)	-0.5V	-0.5V
(max.)	VCC+0.5V	VCC+0.5V
Storage temperature(Tst):		
(min.)	-65 deg. C.	-55 deg. C.
(max.)	+150 deg. C.	+125 deg. C.
Operating temperature:		
(min.)	0 deg. C.	0 deg. C.
(max.)	+85 deg. C.	+85 deg. C.

9/ Operating parameters (spec'd not measured)

	R4200	R4600(3V)
Output HIGH voltage(VOH): (min.)	2.4V	2.4V
Clock output HIGH voltage(VOHC): (min.)	2.7V	
Output LOW voltage(VOL): (max.)	0.4V	0.4V
Input HIGH voltage(VIH): (min.)	2V	0.7VCC
(max.)	VCC +0.5V	VCC +0.5V
Input LOW voltage(VIL): (min.)	-0.5V	-0.5V
(max.)	0.8V	0.2VCC
MasterClock Input HIGH voltage (min)	0.8 x VCC	
(max.)	VCC + 0.5V	
MasterClock Input LOW voltage (min)	-0.5V	
(max.)	0.2V x VCC	
Input Capacitance (max.)	10 pF	10 pF
Output Capacitance (max.)	10 pF	10 pF
Operating current (ICC) (max.)	0.67A	1.2A
Input leakage (ILeak) (max.):	10uA	
Input/output leakage (IOLeak) (max.)	20uA	

10/ Master clock and clock parameters (spec'd not measured)

	R4200	R4600(3V)
MasterClock High:		
TmcHigh (min.):	6 ns	4 ns
MasterClock Low		
TmcLow (min.):	6 ns	4 ns
MasterClock Freq		
(min.)	10 MHz	25 MHz
(max.)	40 MHz	50 MHz
MasterClock Period		
Tmcp (min.):	25 ns	20 ns
(max.)	100 ns	40 ns
Clock Jitter for Master Clock (Tmcjitter) (max.):		+/-250ps
Clock Jitter for MasterOut, TClock, RClock (Tmcjitter) (max.):	+/-500ps	+/-500ps
MasterClock Rise Time (Tmcrise) (max.):	5 ns	5 ns
MasterClock Fall Time (Tmcfall) (max.):	5 ns	5 ns
ModeClock Period		
Tmodeckp (max.)	N/A	256 * Tmcp
JTAG Clock period (TJTAGCKP) (min.)	4 * Tmcp	4 * Tmcp

11/ System Interface parameters (spec'd not measured)

	R4200	R4600(3V)
Data output Tdo		
(min.):	3.5 ns	1.0 ns
(max.):	10 ns	10 ns
Data Setup Tds		
(min.):	3.5 ns	3.5 ns
Data Hold Tdh		
(min.):	1.5 ns	1.5 ns
Status output Tso		
(min.):	3.5 ns	N/A
(max.):	7 ns	N/A
Clock Rise Time Tcorise		
(max.):	5 ns	
Clock Fall Time Tcofall		
(max.):	5 ns	
Clock High Time Tcohigh		
(min.):	6 ns	
Clock Low Time Tcolow		
(min.):	6 ns	
Mode data setup (Tds) (min.):	N/A	3 ns
Mode data hold ((Tdh) (min.):	N/A	0 ns
Capacitive Load Deration (CLD)		
(max.):	2 ns/25pF	2 ns/25pF