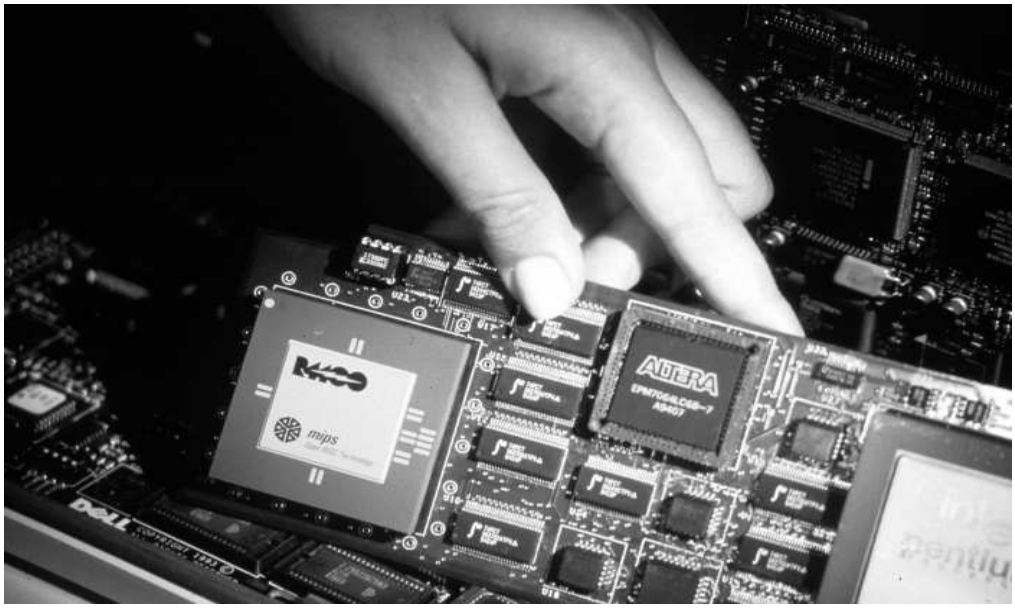
mips
Open RISC Technology

UltraP (TM)

Pentium(TM) to MIPS Upgrade

Preliminary Information



Overview:

UltraP reference design, offered through MIPS Technologies Inc., provides PC manufacturers and users a simple upgrade path from their existing Pentium(TM) based systems running Microsoft's Windows(TM) operating system, to high performance MIPS^R microprocessor based systems running the Windows NT(TM) operating system. PC vendors can use this design to build custom modules using the MIPS R4600 or R4400 microprocessors, that are plug compatible with a Pentium microprocessor. PC vendors manufacturing Pentium systems now have an option of providing to their customers, ex-factory, standard Pentium systems or upgraded higher performance MIPS based systems without losing the Pentium (Windows & DOS) environment. Alternatively, in cases where customers have already purchased Pentium systems, PC vendors can easily upgrade existing systems in the field to MIPS based Windows NT systems.

Preliminary benchmarking results indicate that UltraP systems running MIPS R4600 at 150MHz deliver upto 3.5 times the performance of Pentium 66MHz systems and over 2.5 times P54C 100MHz systems.

Architecture:

UltraP architecture uses translation logic that translates a MIPS R4600 system bus into a Pentium bus. Consequently, all interface with mother-board based core logic, e.g. PCI chip set, is done through the Pentium bus eliminating any need for modification to the mother-board. This implies that existing secondary cache, main memory, peripheral cards etc. are completely reusable.

At system start-up time, both the Pentium and the R4600 are reset simulataneously. The Pentium completes all system start-up and initialization tasks and brings up DOS. At this point, depending on user selection, Windows NT on MIPS, Windows NT on Pentium or, Windows on Pentium can be started. If the user selects Windows NT on MIPS, system control is passed over to the MIPS R4600. While in Windows NT environment the Pentium is not used at all and all tasks are done by the R4600.

On the first revision of UltraP user must reboot the system to get back to DOS/Windows environment. In future revisions itwill be possible to make this transition without the need for rebooting.

Implementation:

Bus translation logic on the first revision of UltraP consists of 1 EPLD, 4 PALs, pipeline registers for cache writeback data buffering, and read/write buffers. The EPLD and 5ns PALs generate bus cycle definition signals and control signals for the Pentium. In this design a 68 pin, 7ns EPLD in PLCC package from Altera Corp. is used. UltraP design contains a clock generation scheme where the motherboard CPU clock can be multiplied by 1.5 times to generate upto 100MHz input clock for the R4600. The translation logic can be reduced to a couple of FPGAs in future implementations bringing down manufacturing cost and providing a better form factor for the module.

MIPS R4600 microprocessor can be purcahsed from Integrated Device Technology, NKK Corporation and, Toshiba Corporation.

For more information please call MIPS at 800-998-6477(inside US); 415-933-6477 (outside US). MIPS Dial-In Fast FAX Information Service 800-446-6477 (inside US); 415-688-4321 (outside US)

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