DWG NO 98A0792

REVISIONS

SYM	DESCRIPTION	APPROVED	DATE
A	PRODUCTION RELEASE EN [illegible]7	[signature]	3/15/72
B	REVISED PER EN 80715	[illegible]	5/22-72

DR C. Towner	1-24-72	
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ENGR [signature]	1-24-72	
APPD [signature]	3/15/72	
APPD [signature]	3/[illegible]/72	

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2722 michelson drive [illegible] California 92664

TITLE

ENGINEERING DESCRIPTION
PARALLEL 8/16 BIT PAPER TAPE CONTROLLER
MODEL 620-55 or 620-51A

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	A	98A0792	B

SCALE —

SHEET 1 OF 38

96A0153-0006

ENGINEERING DATA FORM

OPTION	8/16 Bit Parallel Controller
MODEL	See Below
NO. OF LOGIC CARDS REQ'D.	1
NO. OF CARD SLOTS REQ'D.	1
LOCATION OF SLOTS (NUMBERING)	Any
CONNECTORS REQ'D. (EXCLUDING I/O)	2
KEYING	None
ST'D. DEVICE ADDRESS	Variable (0 to 77)
WIRELIST NUMBER	None
MANUAL PUBLICATIONS NUMBER	This document
PERIPHERAL EQUIPT. REQ'D	See Below
MFG'R.	
MODEL	
GEN'L. SPECS	

NOTES:

The following paper tape devices may be operated through this controller.

Remex Reader	Model #620-51A
Facit Punch and Remex Reader	Model #620-55

Drawings:

620-51A Assembly Drawing	01P1219
620-55 Assembly Drawing	01P1206
→ Controller Assembly	44P0568
Logic Diagrams	91C0369
Facit Punch Cable Drawing	53B0557
Remex Reader Cable Drawing	53B0602
Facit Punch Procurement Spec.	35A0071
Rack Mount Facit Punch Procurement Spec.	35A0077
Remex Reader Procurement Spec.	35A0082
TEST PROGRAM	92A0107-023

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FIGURES

TABLES

SECTION 1
GENERAL DESCRIPTION

1.1 Introduction

The VDM Parallel 8/16 Bit Controller is a special peripheral controller designed to interface between the VDM 620 series computers and a variety of 8 bit input or output peripherals. Data may be transferred in either sense mode or by means of the Buffer Interlace Controller (BIC). In the output mode, 8 or 16 bit data words may be transferred. In the input mode, only 8 bit words may be transferred.

1.2 Functional Description

Ref. Logic Diagrams 9IC0369
620 Computer Manual

1.2.1 Device Address

The device address may be any address from 0 to 77_8. The address is decoded from EB00 through EB05 and signal IUAX-1 (Computer Interrupt Acknowledge). These E-Bus signals are made available on the wire wrap connectors on the back plane. This allows the full device address to be hand wired on the back plane connector. (See para. 3.4).

1.2.2 External Control

The mechanization of the EXC commands is as follows: The device address, EB11+ and Function Ready Pulse (FRYX+) form FUNAD. Lines EB06 through EB08 are applied to a binary to 1 of 8 line decode. The decoded outputs (DEC 0 thru 8) are further decoded by "ANDING" them with FUNAD, thus, forming EXC decodes EXC 0 thru 7.

1.2.3 Extended External Control

Extended external control is developed as in 1.2.2 except EB15+ is the gating term instead of EB11+.

FIGURE 1.1-FUNCTIONAL BLOCK DIAGRAM

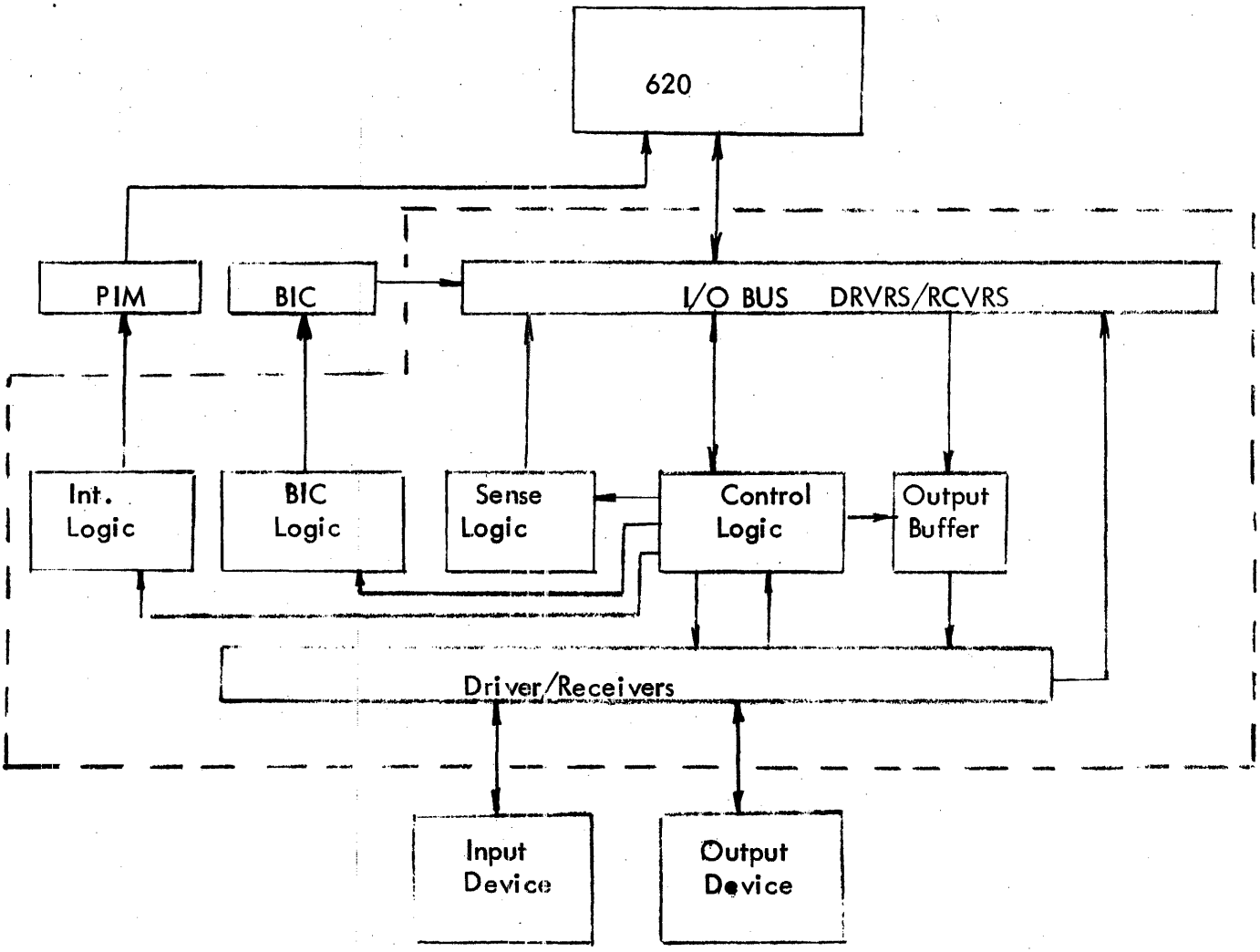
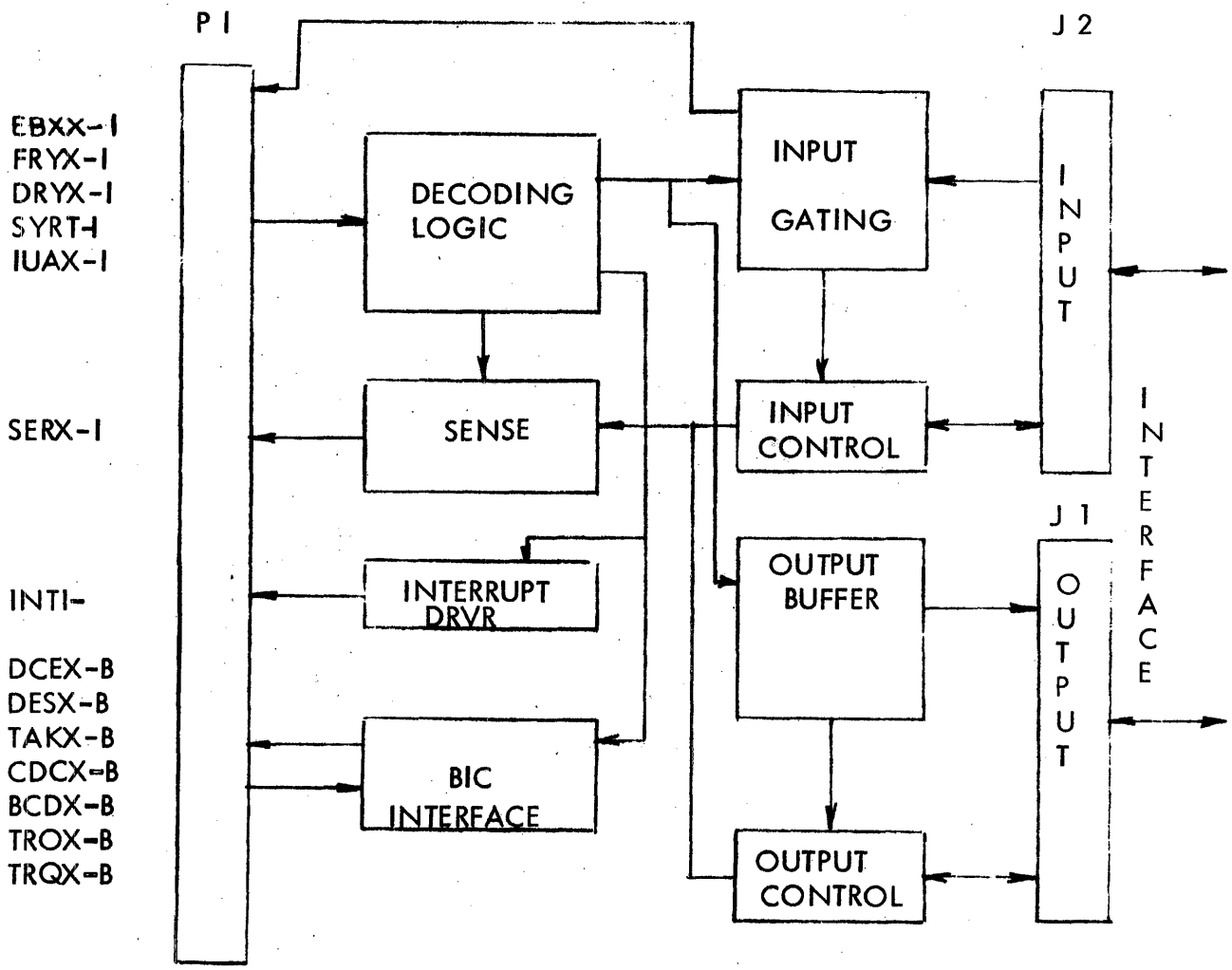


FIGURE 1.2 CONTROLLER BLOCK DIAGRAM



1.2.4 Data Transfer In (See Figure 1-3)

The data transfer in logic controls the transfer of the eight bit word from the peripheral device cable to the input (E) bus. Any of the data transfer in commands (IAR, IBR, IME, CIA, CIB) transfer the input data (DIXX+) to the E-Bus as follows:

The device address and EB13+ enabled flip flop DTIX. The trailing edge of FRYX+ clocks on the flip flop and the trailing edge of DRYX+ resets the flip flop. The output of the flip flop gates the input data onto the E-Bus. DTIX is also buffered and sent to the external device as STEP+. In the case of a Paper Tape Reader, this pulse will cause the tape to move to the next data holes. When this occurs, HRRY (Data Ready) is returned from the peripheral device and sets IRDY flip flop, signaling that next data word is ready.

1.2.5 Data Transfer Out

1.2.5.1 8 Bit Mode (See Figure 1-4)

The data transfer out logic controls the transfer of the data word to the peripheral device. Any of the data transfer out commands (OAR, OBR, OME) loads the output buffer as follows:

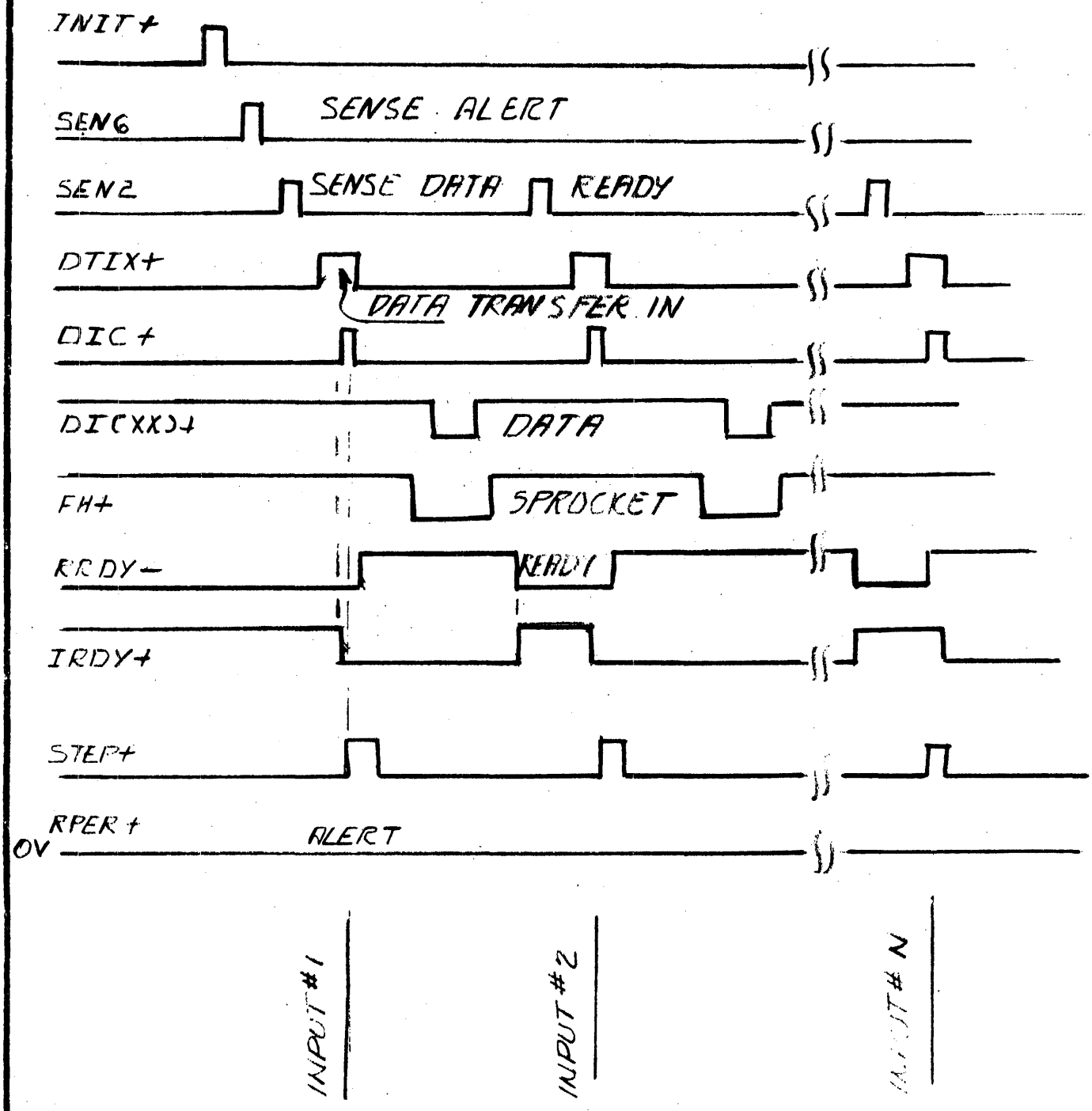
The device address and EB14+ enables the data transfer out flip flop DTOX. The trailing edge of FRYX+ clocks on the flip flop and the trailing edge of DRYX+ clocks off the flip flop.

Data (EB00+thru EB15+) is then clocked into the output buffer (OBXX+) by DOCA+. (Buffered DOC-).

DOC- (DTOX+ DRYX+) is utilized to fire one shot STRB+. This signal is buffered and sent to the peripheral device as DSTRB+, the data strobe. Gating of the least significant data bits to the interface cable is accomplished by the term SHI+ (not 16 bit mode).

The output buffer busy flip flop OBFLD+ is set by the trailing edge of DOC+, and reset by the trailing edge of the peripheral device busy pulse (RWDY-). Sensing of the OBFLD+ synchronizes data transfer with the peripheral device at its maximum rate.

FIGURE 1-3 DATA TRANSFER IN TIMING



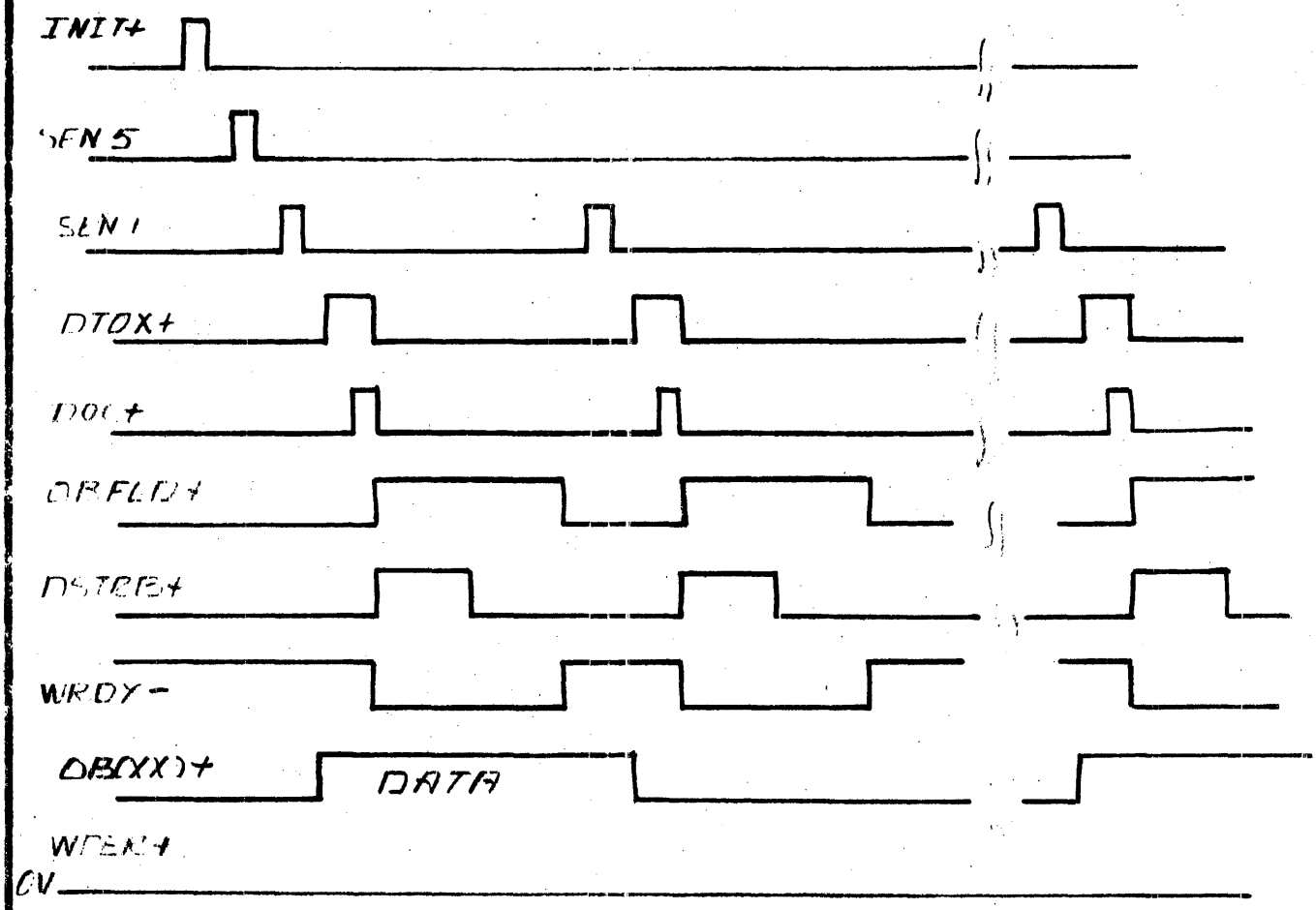


FIGURE 1·4 8 BIT DATA TRANSFER OUT TIMING

1.2.5.2 16 Bit Mode (See Figure 1-5)

Set up of the data transfer out flip flop and loading of the output buffer register is accomplished in the same way as in the 8 bit mode. Additional logic comes into play, however, to steer the two 8 bit bytes to the peripheral device.

EXC 3 is utilized to set the 16 bit mode flip flop. The output of the flip flop enables the clock for the STEER flip flop. The most significant bits (EB08 thru EB15) are transferred to the interface buffers in conjunction with the first byte strobe (DSTRB) developed by DOC+. The reset term (WRDY+) for OBFLD is inhibited by 16 BIT-, thus holding the controller in the busy state. Upon receipt of the trailing edge of the peripheral device busy pulse (LWRY), the STEER flip flop is set, which gates the least significant data bits (EB00 thru EB07+) to the interface buffers and develops the second interface strobe. Upon receipt of the trailing edge of the second peripheral device busy pulse, the steer flip flop is reset which resets the controller busy flip flop OBFLD+. A second 16 bit word may now be transferred to the controller.

1.2.6 Sense Response Logic

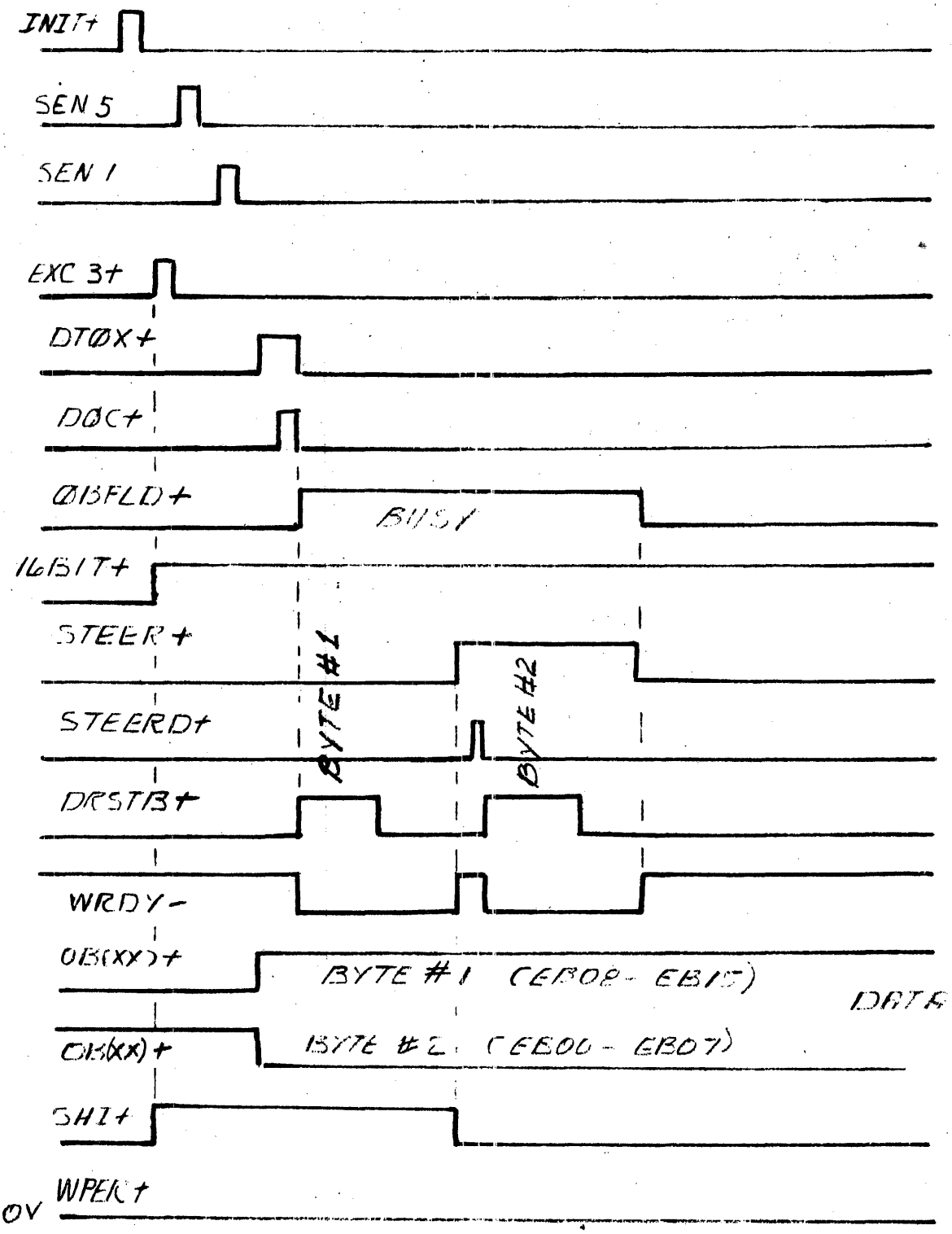
The sense commands check the peripheral device status and are mechanized as follows: Function decodes DEC(XX)+ are applied to individual collector OR'd gates which have as second inputs the various status lines. For example: The write peripheral device alert line, WPER+. In the case of the paper tape punch, if this line is true (high) at sense time, the device is in an alert (malfunction) state. This causes SERX-1, the sense line to the computer, to go true (low) indicating the alert condition.

Because this controller has been designed for more than one specific application, provision has been made within the logic to tie in either high or low active state status lines. If the high active state is used, then a ground jumper within the peripheral cable is required to disable the low active state input. This jumper will be flagged in Table 3.2 (pin assignment) of the pertinent engineering description.

1.2.7 BIC Control Logic

BIC transfer may be made in either input or output mode. Once the BIC is connected to the computer, it sends out DCEX-B which enables the set gate of flip flop CDCX. EXC connect BIC for either input or output will then set CDCX. CDCX-B is returned to the BIC indicating data transfer is now under control of BIC.

FIGURE 1-5 16 BIT DATA TRANSFER OUT TIMING



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When the peripheral device is ready (BRDY-) transfer request line TRQX-B is forced true (low). The BIC responds by forcing transfer acknowledge line TAKX-B true)low). The BIC enabled term BOCE-, in the case of an output transfer, goes true and enables data transfer out flip flop DTOX+ which initiates a data transfer out operation. In the case of a data transfer in operation, BICE- goes true and enables DTIX which initiates a data transfer in operation. This sequence of events occurs in synchronization with the peripheral device ready line until the BIC block transfer is complete. A BIC complete (DESX-B) pulse is received by the controller which resets flip flop CDCX.

If, at any time, a peripheral alert is received from the peripheral device during a BIC block transfer, signal BICAL- is pulled true (low). This generates BCDX-B which is returned to the BIC as a stop command. The BIC will then abort the transfer by returning DESX-B.

1.2.8 Interrupts

There are two interrupts available: Write Ready (WINT-) and Read Ready (RINT-). These interrupts are the differentiated trailing edges of OBFLD+ and IRDY+ flip flops, respectively.

1.2.9 Special Logic

1.2.9.1 Sprocket Recognition (Paper Tape Reader Input)

During a Paper Tape input operation, special logic has been incorporated to condition the ready line (RRDY+) so that IRDY+ will not be set if the paper tape reaches the end. (No stop code is present on the tape.) Sprocket pulse FH+ is differentiated. The resulting pulse sets flip flop SPROC+. This level is "ANDed" with RRDY+ and the result is utilized as the IRDY+ flip flop set clock. If no further sprockets pulses appear, RRDY+ is inhibited from setting IRDY.

1.2.9.2 DELETED

1.2.9.3 DELETED

TABLE 1-1 CONTROLLER MNEMONICS

MNEMONIC	DESCRIPTION	SOURCE
ADDR+	Decoded Device Address	
ASCII+	Flip Flop to allow 8 bit ASCII code to be sent to the DP2000 Series Printer.	
BCDX-B	BIC Device Disconnect	
BICAL-	BIC Abort from peripheral device.	
BICE-	BIC Input Enable Line to DTIX Flip Flop	
BOCE-	BIC Output Enable Line to DTOX Flip Flop	
BRDY-	Data Ready to BIC	
CDCX+	BIC Connected Flip Flop	
DA(XX)+	Decoded Device Address ANDed with interrupt acknowledge	
DCEX-B	BIC Device Connect	
DEC(X)-	EB6 through EB8 Decode	
DESX-B	BIC Disconnect	
DI(XX)+	Input Data from peripheral device	
DOC+	Reset term for DTOX Flip Flop	
DOCA+	Strobe for Output Buffer (Buffered DOC+)	
DRYX-I	Data Ready Pulse from CPU	
DSTRB+	Data Strobe to peripheral device	
DTIX+	Data Transfer In Flip Flop	
DTOX+	Data Transfer Out Flip Flop	
DWRDY+	Optional Write Ready Line for use when peripheral device does not supply one.	

TABLE 1-1

MNEMONIC	DESCRIPTION	SOURCE
FB(XX)+	E-Bus Bits 00 thru 15	
EXCB0-	Extended EXC Decode 0	
EXCB1-	Extended EXC Decode 1	
EXC(X)+	EXC Decodes 0 thru 7	
FH+	Sprocket Pulse from Peripheral Device	
FRYX-1	Function Ready Pulse from CPU	
FORMAT+	Format Flip Flop to transfer paper moving information to DP2000 Series Line Printer.	
FUNAD-	Function Command and Device Address	
INIT+	Initialize command.	
IØRDY+	Read or Write Ready	
IRDY+	Read Ready Flip Flop	
IUAX-1	Interrupt Acknowledge Pulse	
NØPCH-	Inhibit OBFLD+ flip flop if no output device connected.	
OBFLD+	Output Buffer Loaded Flip Flop	
OB(XX)+	Output Buffer Data Bits 00 thru 15	
OR(XX)A+	Output Bits 00 thru 15 at Interface Connector	
READ+	Read Mode Flip Flop	
RINT+	Read Ready Interrupt	
RPER+	Read Peripheral Alert	
RRDY+	Read Ready	

TABLE 1-1

MNEMONIC	DESCRIPTION	SOURCE
SERX-I	Sense Line to CPU	
SHI+	Strobe for bits 00 thry 07 to interface connector	
SHI-	Strobe for bits 08 thru 15 to interface connector	
SPROC+	Sprocket flip flop	
STEER+	Steer flip flop steers logic to second output data byte.	
STEP+	Step Pulse to external device to bring in new data.	
SYRT-I	Manual system reset from CPU.	
TAKX-B	BIC Transfer Pulse	
TRØX-B	Transfer Out Pulse	
TRQX-B	Transfer Request Pulse	
WINT-	Write Ready Interrupt	
WPER+	Write Peripheral Alert	
WRDY+	Write Ready Pulse	
ZØNSEL+	Zone Select Flip Flop (Option)	
16 BIT+	16 Bit Mode Flip Flop	

1.3 Controller Specifications

This section contains the principle specifications for the controller.

CHARACTERISTICS	DESCRIPTION
Control Capability	Any peripheral device whose requirements are eight data lines in or out with coincident strobe. The peripheral device must supply two more lines. A peripheral alert line and peripheral ready line. Both an input and an output device may be controlled on a time sharing basis. All lines must be TTL compatible.
I/O Capability	Seven External Control Commands (EXC); two Extended External Control Commands (EXCB), six Sense Commands (SEN), three Data Transfer Out Commands (OAR, OBR, OME), five Data Transfer In Commands (INA, INB, IME, CIA, CIB).
Logic Levels	
Negative Logic	Logic 1 = 0 to 0.5Vdc. Logic 0 = +2.4 to +5.0Vdc.
Positive Logic	Logic 1 = +2.4 to +5.0Vdc Logic 0 = 0 to +0.5Vdc
System Programming	Permits operating the system on an interrupt basis or by programmed sense response loops. BIC capability is also available. In the output mode, The CPU may transfer 8 or 16 bit (two 8 bit bytes) words. In the input mode, only 8 bit words may be transferred.
Size	Packaged on a single circuit card measuring 12.7 inches by 7.7 inches.
Power Requirements	+5 Volts DC @ 1 AMP
Operational Environment	0 to 50°C, 0 to 90°R.H. (without condensation)

1.4 Paper Tape System - General Specifications

1.4.1 Facit Punch Model 4070

Punch speed:	Max 75 rows per second at nominal voltage and frequency
Row spacing:	2.54 mm (0.1")
Tape feed:	Incremental, externally controlled
Feed accuracy:	Complies with ISO standard Adjacent rows, 3% 10 rows, 1% 50 rows, 0.5%
Punch hole configuration:	5-8 track ISO standard 6-track typesetting
Tape widths:	5-track 17.46 ±0.05 mm (.687" ± .002") 6-track 22.23 ±0.05mm (.875" ± .002") 7-track 22.23 ± 0.05mm (.875" ± .002") 8-track 25.4 ±0.05mm (1.000" ± .002")
Tape thickness:	Punch is adjusted for 0.1mm tape on delivery, but can be reset for tapes ranging from 0.08 mm to approximately 0.12mm in thickness.
Type of tape:	Paper, mylar or plastic tape complying with ISO standard
Tape reel hub:	Accepts 51 - 52 mm (2") cores
Outside diameter of tape reel:	Up to 200 mm (8")
Dimensions:	Length 515mm (20.3") Width 205mm (8.1") Height 210mm (8.3")
Weight:	13 kg (29 lbs.)
Mains connection:	Mains voltage shall not be connected up to punch units - control units supply the punch units with voltage

Voltage:	220 V ± 10% single phase 50 Hz ± 2Hz 220 V ± 10% single phase 60Hz ± 2Hz 115 V ± 10% single phase 50 Hz ± 2Hz 115 V ± 10% single phase 60Hz ± 2Hz	Switch Adjustable
Power Consumption:	Approximately 90W	
Control Unit		
Ambient temperature:	0°C - +40°C	
Relative Humidity:	Max 85%	
Dimensions:	Length (incl. connectors) 600 mm (23.6") Width 262 mm (10.3") Height 170 mm (6.7")	

AC INPUT Voltage:	115 V, 127 V, 220 V and 240 V + 15% -10% -1phase AC, grounded mains voltage inlet
AC INPUT Frequency:	50 - 60 Hz ± 2 Hz
Power consumption:	Max 200W with punch motor connected at rated voltage
Voltage outlet for punch:	Grounded outlet for 1-phase AC Voltage, 220 V +15% Current, max 1.1A Frequency, same as mains frequency Output impedance, max 12 ohms
Input logic levels:	
Start pulse	Logical 1, +4V to +25V
Punch motor start	Logical 0, +2 V to -25V
Data signals	Input impedance min 1.5 kohm, max 200 pf

Start pulse:	Start, logical 1 Not start, logical 0 Pulse duration, 0.1 - 3ms Rise time, max 10us
Data signal:	8 parallel lines. A DC voltage or a pulse with a duration of at least 0.1 ms arrives simultaneously with the start pulse. Hole, logical 1 Not hole, logical 0
Output logic levels: Ready signal	Negative logic Punch ready for start pulse and data signals Logical 1, nominal +5 V (can range from +4.3 V to +5.1 V) max 2 mA Punch not ready Logical 0, 0 V to +0.3 V max 20 mA Switching time, max 2us
Register:	The punch register stores one row (8 bits).

Internally programmed functions

Blank tape:	Lever on punch unit can be used to feed out tape punched only with feed hole.
Mark character:	Same lever can be used to feed out tape punched with a special mark character which can comprise any combination of holes specified by the customer. As standard, all-holes tape is punched out.

Connections and controls

The punch unit is connected to the control unit via a signal cable and power cable. The control unit shall be connected to mains having the voltage specified on its nameplate.

ON/OFF power switch:	This control unit switch turns on power throughout the system and lights an indicator lamp in the switch
Line Fuse:	3 A time-delay fuse is used in all control units.
Punch fuse:	0.5 A time-delay fuse. Rack model, 1 A time-delay fuse.

For further information, see the Instruction Book for the Facit 4070.

1.4.2 Remex Reader Model RRX1150BBX/650

Tape Movement	Bidirectional (Manual Operation Only)
Reading Speed	150 characters per second, ±10% in continuous mode and asynchronously at any speed up to 150 characters per second. See Section 5.4.5.
Tapes	Reads standard 8-track (1-inch) tapes with light transmissivity of 57% or less and thickness between 0.0027 and 0.0045 inch (oiled buff paper tape). Options for 6 channel typesetter available.
Input Power	115 VAC (RRX1150BBX/650/S000) or 230 VAC (RRX1150BBX/650/E000), ±10%, 47 to 420 Hz. single phase at 0.6 amp peak (115 VAC) or 0.3 amp (230 VAC). 100 VAC, 47 to 420 Hz option also available.
Temperature	Operating: 0°C to +55°C, free air. Non-operating: -55°C to +85°C.
Weight:	RR-1150BBX: 12 lbs. RRF1150BBX: 13 lbs.
Mounting Dimensions	RR-1150BBX/650: 5-1/4" high, 19" wide, 6" behind 1/4" panel, 2-1/2" in front of panel. RRF1150BBX/650: 7" high, 19" wide, 6" behind 1/4" panel, 2-1/2" in front of panel.
Drive Control (Remex Mode 6)	Stop: +2.4 V +5.0 (2K to +5V) or open circuit Drive: 0 V +0.4 @ 5ma.
Data Output (Remex Mode 5)	Hole: +2.4 V +5.0 @ 0.2 ma (2.2K resistor to +5V dc) No hole: 0 V +0.4 @ 16 ma. (sink) Data envelops sprocket by at least 100 usec on both rising and falling edges.
Slew Mode Operation	250 cps nominally

SECTION 2
PROGRAMMING

2.1 PAPER TAPE SYSTEM PROGRAMMING REQUIREMENTS

The paper tape system may be programmed in a multi-peripheral environment by the external interrupt structure or individually selected by programmed response loops. Four EXC instructions control the operations with data transfers and sense interrogations affected by standard 620 programming methods. BIC capability is also available.

2.2 Description of Commands

There are a total of seventeen instructions reserved for use with the paper tape system. These include four external functions, eight transfers, and five sense. The reserved instructions are listed and described in the paragraphs that follow. It is assumed here that the paper tape system is assigned to device address 37.

2.2.1 External Control

EXC (N=0 or 1)	100N37	Write Connect (BIC)
EXC 3	100337	16 Bit Output Mode
EXC 4	100437	Initialize Controller
EXC (N=2 or 5)	100N37	Read Connect (BIC)

2.2.2 Sense

SEN 1	101137	Write Ready
SEN 2	101237	Read Ready
SEN 5	101537	Read and Write Ready
SEN 6	101637	Write Peripheral Alert
SEN 7	101737	Read Peripheral Alert

2.2.3 Data Transfer Out

OAR	103137	Output A Register
OBR	103237	Output B Register
OME	103037	Output from Memory

2.2.4 Data Transfer In

INA	102137	Input to A Register
INB	102237	Input to B Register
IME	102037	Input to Memory
CIA	102537	Clear and Input to A Register
CIB	102637	Clear and Input to B Register

2.3 Instruction Set Description

2.3.1 External Control Commands

BIC Write Connect (EXC 0 or 1)

This command connects the controller to a 620 BIC for output of data to the paper tape punch under DMA control. It should be issued after the BIC is initialized and loaded with the parameters of the DMA Transfer. DMA operation requires a BIC option.

BIC Read Connect (EXC 2 or 5)

This command connects the controller to a 620 BIC for input of data from the paper tape reader under DMA control. It should be issued after the BIC is initialized and loaded with the parameters of the DMA Transfer.

16 Bit Output Mode (EXC 3)

In the 16 bit mode, a 16 bit (2 bytes) data word may be sent to the controller. The controller will transmit this data to the punch in two 8 bit bytes. The first byte will correspond to CPU bits 08 through 15 and the second byte CPU bits 00 through 07. (See Figure 2-1.) The controller will hang up in a busy state during the full two byte transfer to the punch.

Initialize (EXC 4)

This command initializes the controller to the following state:

Write Ready
BIC disconnected
Eight Bit Mode

2.3.2 Sense Commands

Write Ready (SEN 1)

This instruction is answered affirmative when the paper tape punch is ready to accept a data character.

Read Ready (SEN 2)

This instruction is answered affirmative when the paper tape reader is available and a previous sprocket hole has been recognized.

Read/Write Ready (SEN 5)

This instruction is answered in the affirmative when the punch is ready to accept data and reader data is available.

Write Peripheral Alert (SEN 6)

This instruction is answered in the affirmative when there is a punch alert for the following conditions:

Punch Power not on
No paper tape

Read Peripheral Alert (SEN 7)

This instruction is answered in the affirmative when there is a reader alert for the following conditions:

Reader Power not on
Run load switch in load position

2.3.3 Data Transfer Out Commands

Any of the data transfer out commands (OAR, OBR, OME) loads the 16 bit output buffer register with E-Bus bits 00 through 15. If the controller is in the 8 bit mode (initialize), only E-Bus bits 00 through 07 will be transferred to the punch. If EXC 9 (16 bit mode) has been previously executed, then two bytes will be transferred to the punch. E-Bus bits 08 through 15 will be the first byte and E-Bus bits 00 through 07 will be the second byte.

2.3.4 Data Transfer In

Any of the data transfer in commands (INA, INB, IME, CIA, CIB) will input an 8 bit data word to the CPU E-Bus. See Figure 2.2 for data E-Bus relationships.

2.3.5 Interrupts

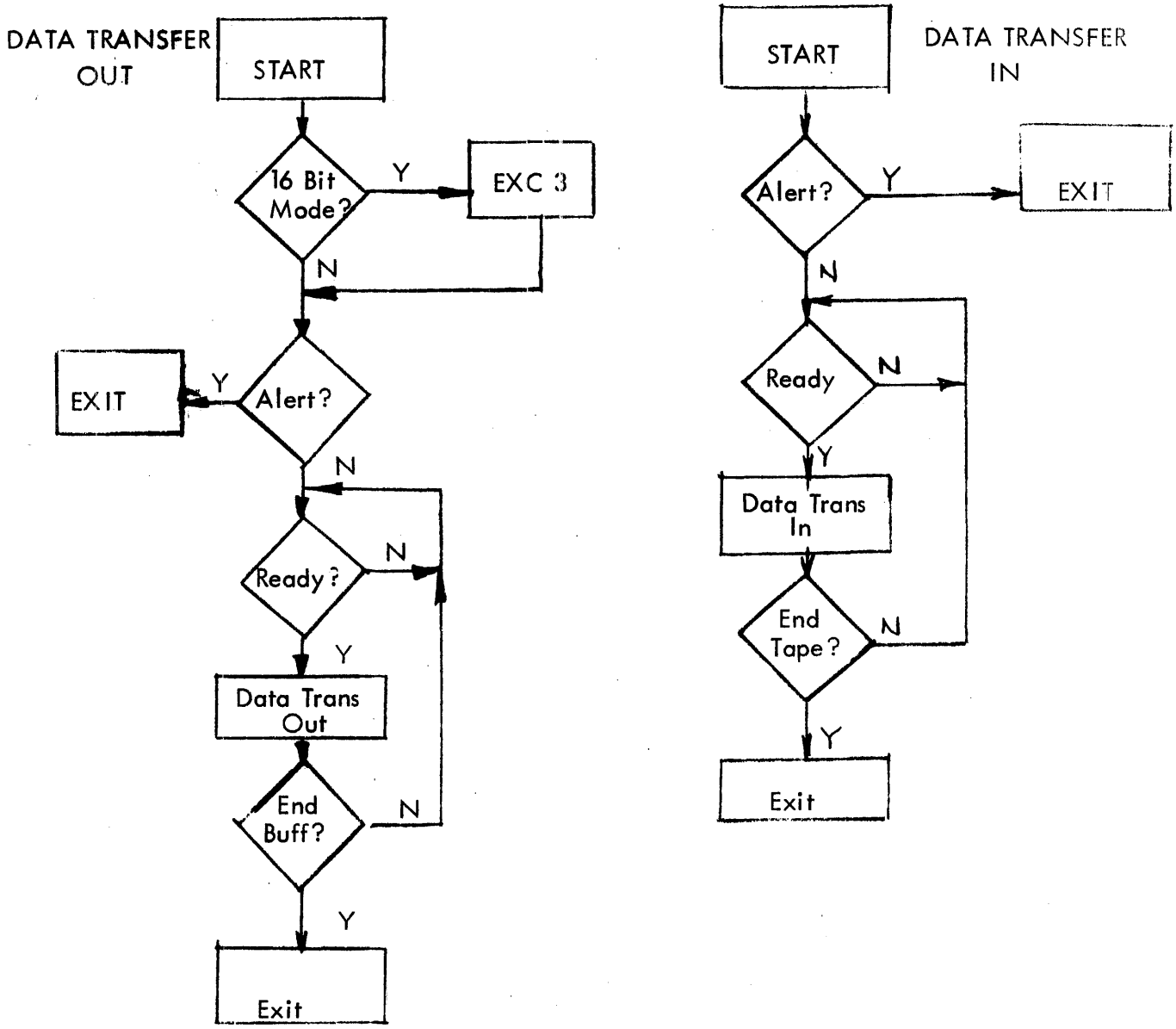
There are two interrupts available: Write Ready and Read Ready. These interrupts correspond to SENS 1 and SENS 2 respectively.

2.4. Typical Operations and Programs

Flow diagrams of typical operating sequences for reading tapes under programmed sense control are illustrated in figure 2.1.

FIGURE 2.1

DATA FLOW



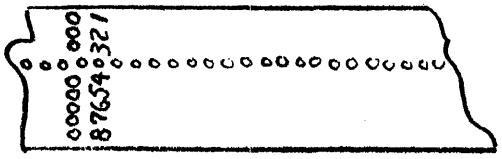
2.5 Data Format

The E-Bus to input or output bits relationship is shown in Figure 2A.2.

Figure 2A-2 - E-Bus to Data Relationship

Input or Output 8 Bit Mode

7	6	5	4	3	2	1	0	E-Bus
8	7	6	5	4	3	2	1	Hole



Output 16 Bit Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	E-BUS
8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1	HOLE

First Byte Second Byte

2.6 Models Applicable Punch and/or Reader

The following paper tape models can be operated using this controller.

620-51A Paper Tape Reader (150 cps)

620-55 Paper Tape Reader (150 cps) Paper Tape Punch (75 cps)

The paper tape reader is defined in procurement specification 35A0082 and is the Remex 150 cps Reader Model RR(X)-150BBX/650.

The paper tape punch is defined in procurement specification 35A0071 OR 35A0077 and is the 75 cps model 4070.

SECTION 3
INSTALLATION

3.1 General

Installation of the Paper Tape System in the field is normally accomplished by Varian Data Machines Customer Service Engineers. Logic diagrams, assembly layout, and Eng. Description are provided at the time of purchase. The following installation data is provided for planning purposes.

3.2 Pre-Installation Requirements

Prior to the installation of the system, proper operation of the computer should be assured through use of the diagnostic test routines described in the 620 Maintenance Manual. An Expansion/Peripheral Controller Chassis must be installed in close proximity to the computer. The chassis is connected to the I/O bus by means of the I/O cable. The I/O BUS IS TERMINATED AT THE LAST EXPANSION CHASSIS

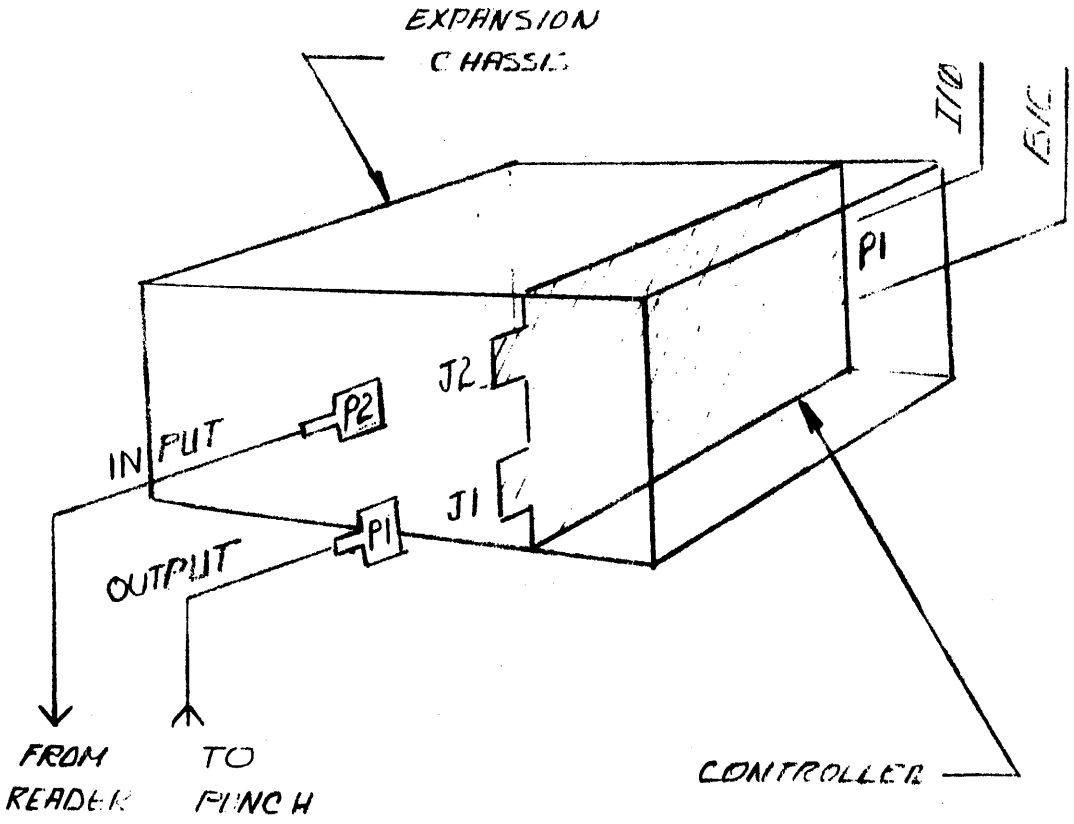


FIGURE 3-1 TYPICAL INSTALLATION

3.3 Wiring Requirements

3.3.1 Controller Back Plane Wiring

The controller requires one card slot space. It uses the standard back plane I/O bus and power wiring used with the expansion chassis (See table 3-1).

3.3.2 Peripheral Device Cabling

There is one cable connecting each peripheral device to the controller. The output cable is connected to controller edge connector J1 and the input cable is connected to controller edge connector J2. Pin assignments are shown in Table 3.2 and Table 3.3, respectively. See Figure 3-1 for typical installation.

TABLE 3-1 Controller Card, P1 Pin Assignments

PIN	MNEMONICS	PIN	MNEMONICS
1	GND	64	EB00+
2	EB00-I	65	EB00-
4	EB01-I	66	EB0I+
6	EB02-I	67	EB01+
8	EB03-I	68	EB01-
10	EB04-I	69	EB1I+
11	EB05-I	70	EB02+
12	EB06-I	71	EB02-
13	EB07-I	72	EB2I+
14	EB08-I	76	EB3I+
15	EB09-I	77	EB4I+
16	EB10-I	78	EB5I+
17	EB11-I	82	EB03+
18	EB12-I	83	EB03-
19	EB13-I	84	EB04+
20	EB14-I	85	EB04-
21	EB15-I	86	EB05-
27	FRYX-I	87	EB05+
29	DRYX-I	90	RINT-
31	SERX-I	96	WINT-
43	SYRT-I	100	GND
44	IUAX-I	118	+5V
48	GND	122	GND
49	TRQX-B		
50	TRØX-B		
52	BCDX-B		
54	CDCX-B		
56	DCEX-B		
58	TAKX-B		
60	DESX-B		

Table 3-2 J1 Pin Assignments

PIN	MNEMONIC	DESCRIPTION	SOURCE
1	DSTRB+	Strobe	Controller
2	Ret		
5	OR03+		
6	Ret		
7	OR02+		
8	Ret		
9	OR01+	Data	Controller
10	Ret		
11	OR00+		
12	Ret		
13	OR07+		
14	Ret		
15	OR06+		
16	Ret		
17	OR04+		
18	Ret		
19	OR05+		
20	Ret		
21	HWRY+	Ready	Device
22	Ret		
23	LWRY-	~~Ready~~	Device
24	Ret		
25	HWPER-	~~Alert~~	Device
26	Ret		
27	DSTRB-	~~Strobe~~	Controller
28	Ret		
29	LWPER+ *	Alert	Device
30	Ret		
32	NO PCH-	Device connected	Controller

* This line is grounded within the cable (Ref. Paragraph 1.2.6).

TABLE 3-3 J2 Pin Assignments

PIN	MNEMONIC	DESCRIPTION	SOURCE
1	Ret		
2	D100+		
3	Ret		
4	D103+	Data	Device
5	Ret		
6	D102+		
7	Ret		
8	D101+		
9	Ret		
10	STEP+	Send Data	Controller
11	Ret		
12	LRRY+	Data Ready	
13	Ret		
14	HRRY-	~~Data Ready~~	Device
15	Ret		
16	HRPER-	$\overline{\text{Alert}}$	Device
17	Ret		
18	FH+	Sprocket Pulse	Device
19	Ret		
20	STEP-	~~Send Data~~	Controller
22	LRPER+	Alert	Device
23	Ret		
35	D105+		
36	Ret		
37	D106+	Data	Device
38	Ret		
39	D104+		
40	Ret		
41	D107+		

3.4 Device Address

Any address from 0 to 77 may be wired in on the back plane. Table 3-4 lists the true and complement inputs and outputs of the I/O bus address bits. Table 3-5 lists wiring connections required for the least significant portion of the device address and Table 2-6 lists wiring connections required for the most significant portion of the device address. Device address of first paper tape system is normally 37_8.

TABLE 3-4 Device Address Input and Output Pins

TERM	PIN (P1)	TERM	PIN (P1)
EB00+	64	EB03+	82
EB00-	65	EB03-	83
EB0I+	66	EB3I+	76
EB01+	67	EB04+	84
EB01-	68	EB04-	85
EB1I+	69	EB4I+	77
EB02+	70	EB05+	86
EB02-	71	EB05-	87
EB2I+	72	EB5I+	78

TABLE 3-5 Device Address Jumpers (least significant address)

DEVICE ADDRESS	JUMPER PINS	DEVICE ADDRESS	JUMPER PINS
X0	65 to 66 68 to 69 71 to 72	X4	65 to 66 68 to 69 70 to 72
X1	64 to 66 68 to 69 71 to 72	X5	64 to 66 68 to 69 70 to 72
X2	65 to 66 67 to 69 71 to 72	X6	65 to 66 67 to 69 70 to 72
X3	64 to 68 67 to 69 71 to 72	X7	64 to 66 67 to 69 70 to 72

TABLE 3.6 Device Address Jumpers (most significant address)

DEVICE ADDRESS	JUMPER PINS	DEVICE ADDRESS	JUMPER PINS
0X	83 to 76 85 to 77 87 to 78	4X	83 to 76 85 to 77 86 to 78
1X	82 to 76 85 to 77 87 to 78	5X	82 to 76 85 to 77 86 to 78
2X	83 to 76 84 to 77 87 to 78	6X	83 to 76 84 to 77 86 to 78
3X	82 to 76 84 to 77 87 to 78	7X	82 to 76 84 to 77 86 to 78

3.5 Peripheral Device Installation and Operation

3.5.1 General

A complete description and operating instructions will be found in the peripheral device maintenance and operation manual that is delivered with the system.

SECTION 4
MAINTENANCE

4.1 General

This section defines the appropriate equipment, diagnostic routines, and required tests to insure the controller's proper performance. Maintenance requirements for the peripheral device are called out in the appropriate peripheral device instruction manual.

4.2 Maintenance of the Controller

The following are standard hardware and software devices for checkout. Addition and/or deletion of these devices may be made in the future, if necessary.

4.2.1 Test Equipment

The Tektronix 545 Oscilloscope or one of similar performance specification is required.

4.2.2 Tools

A standard extender board allows for easy access to the controller during test.

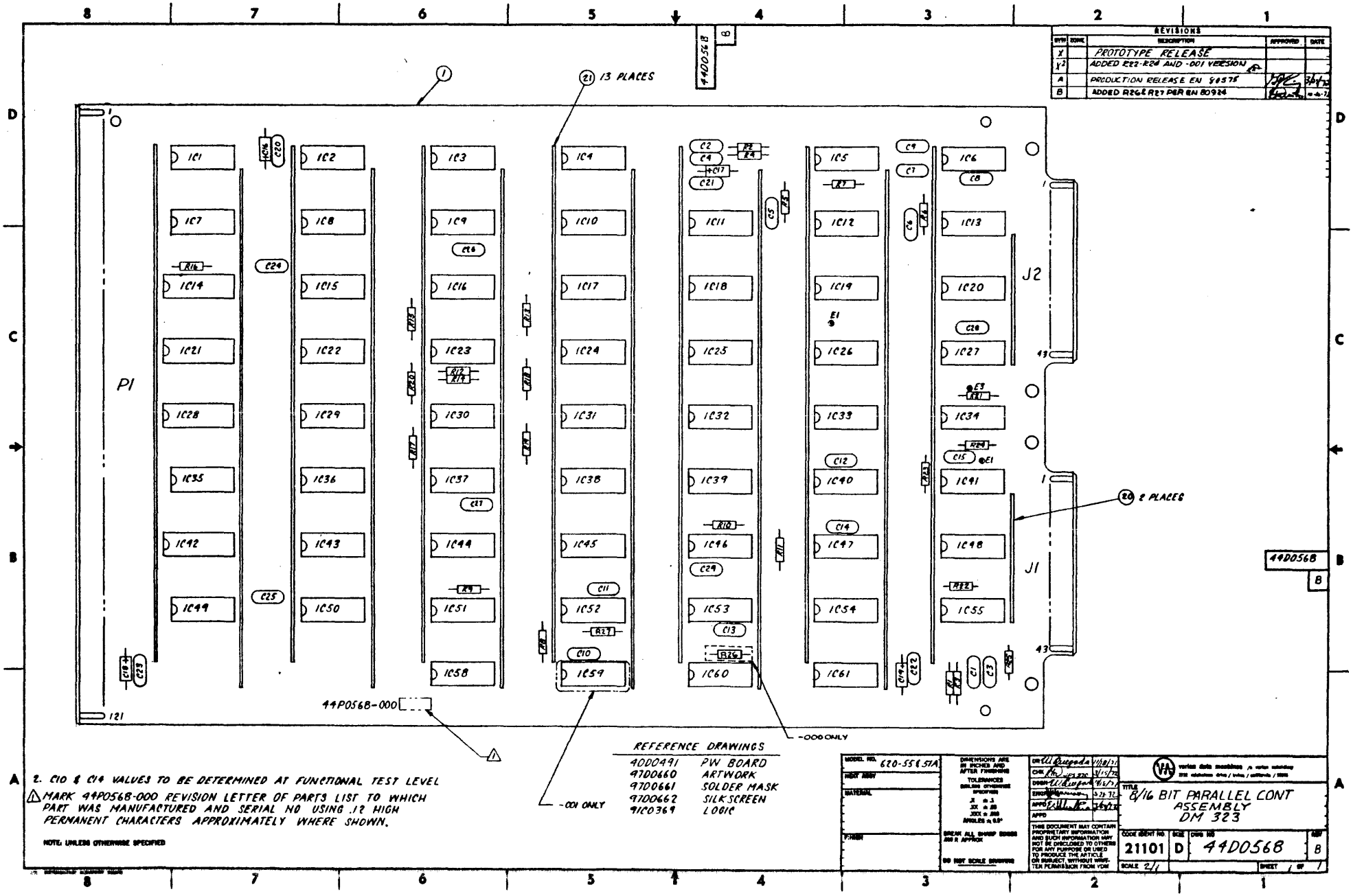
4.2.3 Software (Diagnostic)

Test utilized for diagnosis and trouble shooting of the controller and peripheral devices are as follows:

TEST PROGRAM 92A0107-023

4.3 Maintenance of the Peripheral Device

Maintenance procedures are completely defined in the peripheral device maintenance manual.



2. C10 & C14 VALUES TO BE DETERMINED AT FUNCTIONAL TEST LEVEL

⚠ MARK 44P056B-000 REVISION LETTER OF PARTS LIST TO WHICH PART WAS MANUFACTURED AND SERIAL NO USING .12 HIGH PERMANENT CHARACTERS APPROXIMATELY WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS

4000491	PW BOARD
9700660	ARTWORK
9700661	SOLDER MASK
9700662	SILKSCREEN
9100369	LOGIC

MODEL NO. 620-55&STA
NEXT ASSY
MATERIAL
FINISH

DIMENSIONS ARE IN INCHES AND AFTER FINISHING
TOLERANCES UNLESS OTHERWISE SPECIFIED
X ± .1
XX ± .05
XXX ± .010
ANGLES ± 0.5°
BREAK ALL SHARP EDGES .005 R APPROX
DO NOT SCALE DRAWING

DR W. Rugeda 1/18/72
CHK [illegible] 3/15/72
DESIGN W. Rugeda 4/5/72
ENGR [illegible] 3/24/72
APPD [illegible] 3/24/72
APPD

TITLE 8/16 BIT PARALLEL CONT ASSEMBLY DM 323

CODE IDENT NO. 21101 | SIZE D | DWG NO. 44D056B | REV B

SCALE 2/1 SHEET 1 OF 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

REVISIONS					
CODE	SYM	ZONE		APPROVED	DATE
--	A		PRODUCTION RELEASE EN 80575		8/24/72
--	B		RESISTOR VALUE NOTE WAS 570 OHMS 1259 NOTE WAS -002 ONLY EN. 80715		9/22/72
--	C	CW	ADDED RES. R26 & R27 AND REVISED PER EN 80924		10.16.72
--	D	CW	REVISED PER EN 81033		10.16.72
--	E	CW	REVISED PER EN 81088		10.16.72
--	-	B	REVISED CONN. P1, PIN 95 & 96 ON SHT 9 PER EN 83209		1/10/74

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
1C61	
R27	
C29	

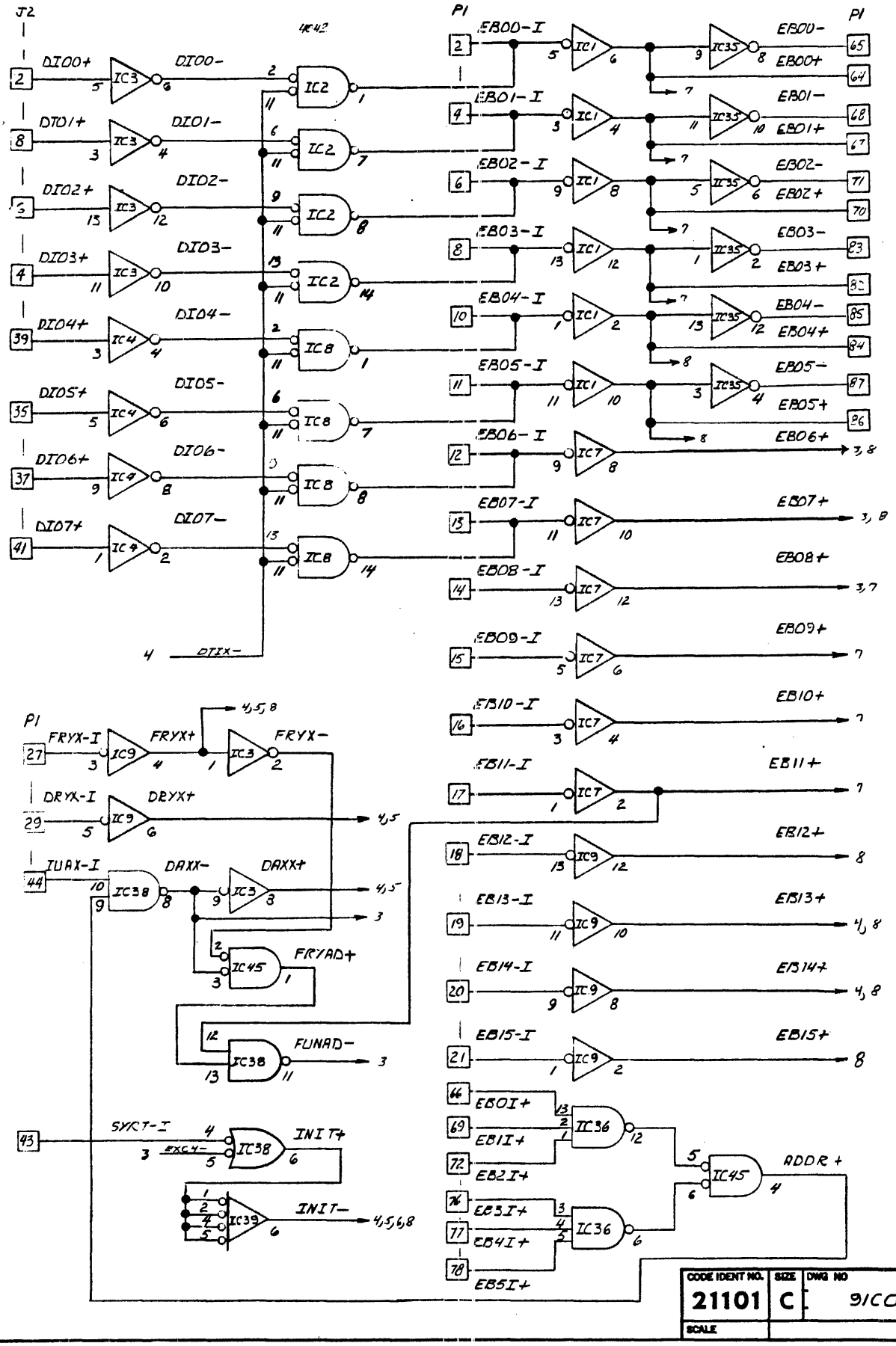
REFERENCE DRAWINGS	
44D0568	ASSEMBLY
44P0568	PARTS LIST
97D0660	ARTWORK
97D0662	SILKSCREEN
97D0661	SOLDERMASK
90D0491	P.W. BOARD

DR	—	—
CHK	[illegible]	3/19/72
DSGN	—	—
ENGR	[illegible]	11-24-71
APPD	[illegible]	8/24/72
APPD		

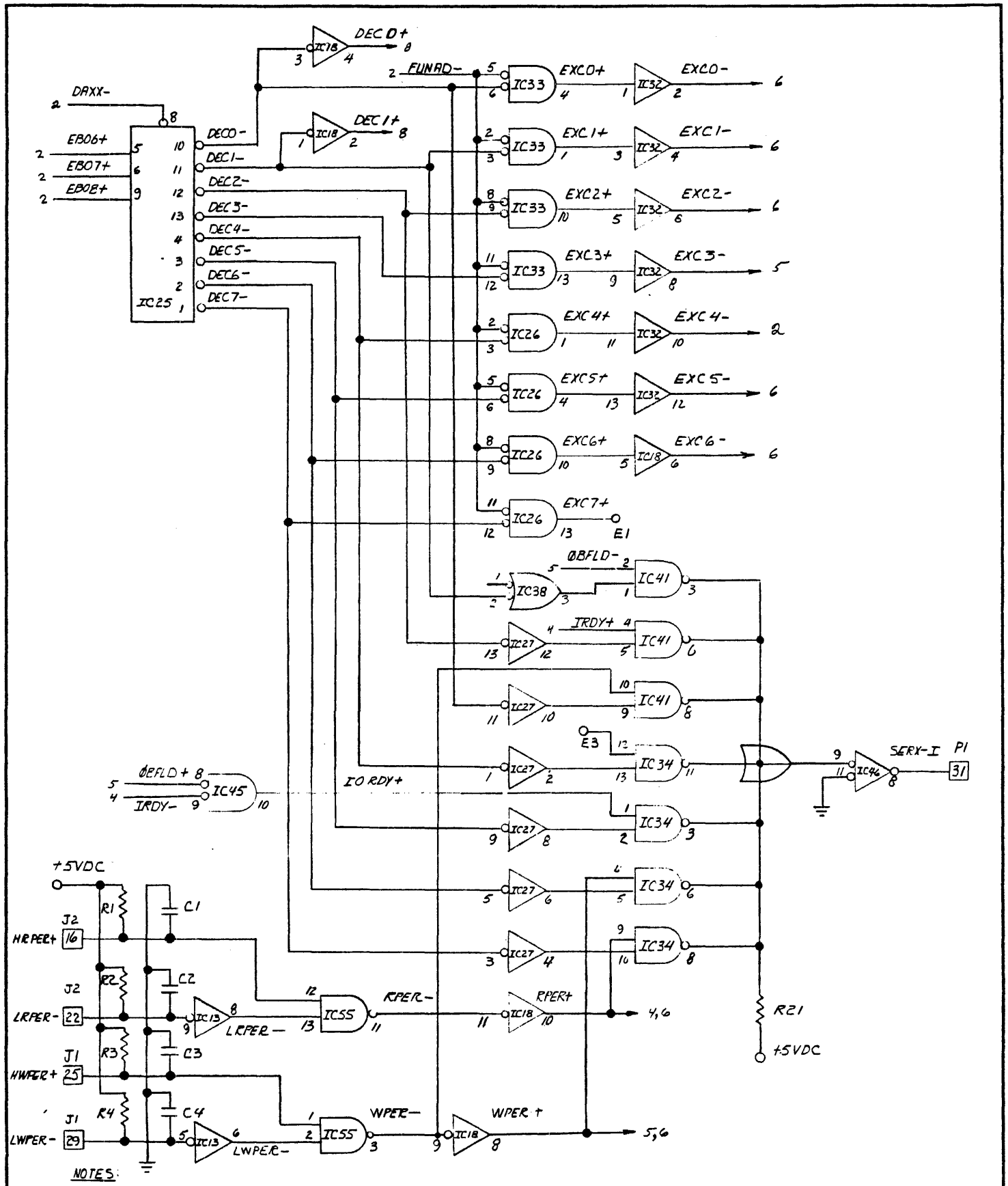
varian data machines /a varian subsidiary
2722 michelson drive / irvine / california / 92664

TITLE LOGIC DIAGRAMS
8/16 BIT PARALLEL CONTROLLER

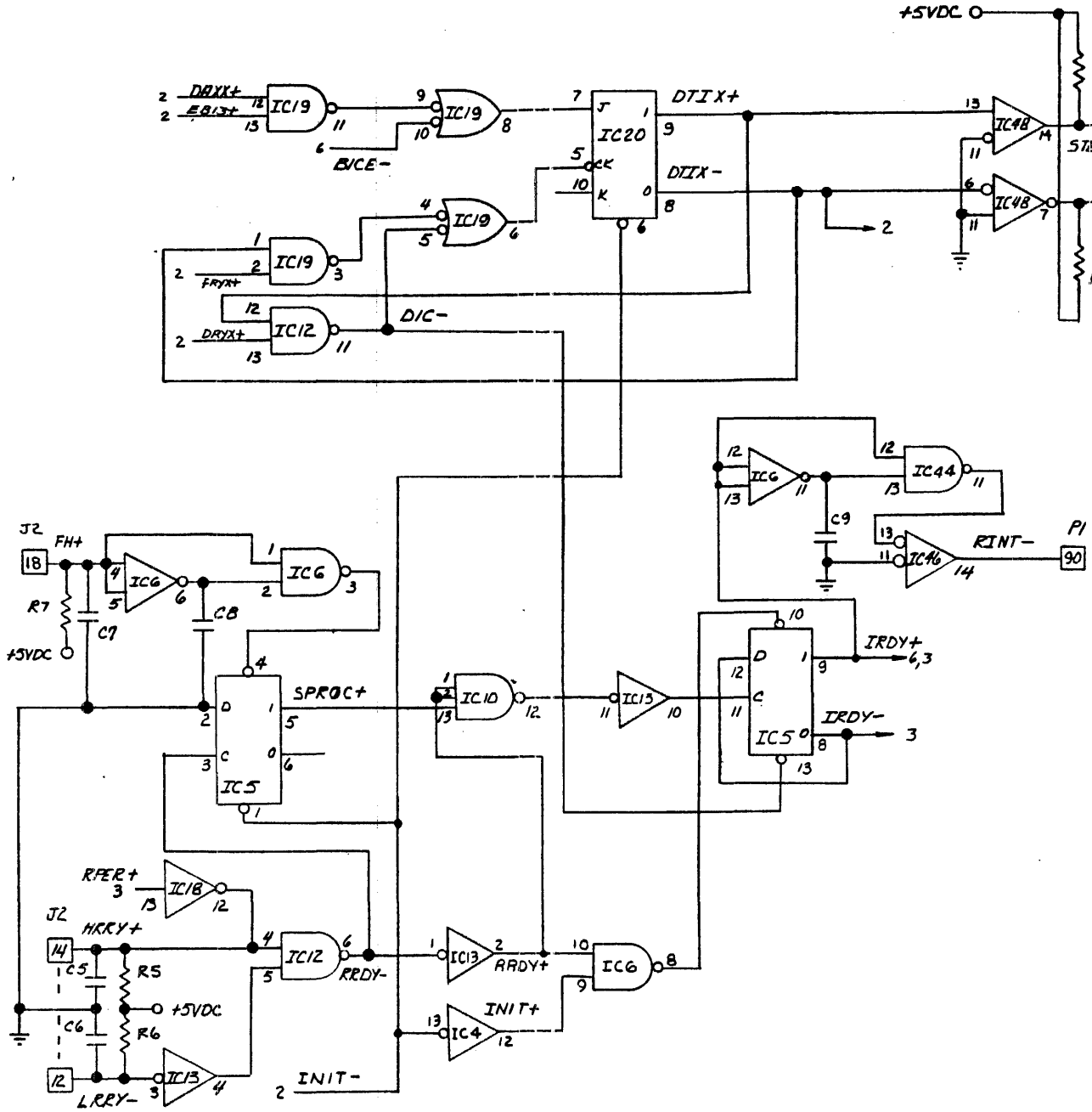
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE —	620-51A, 620-55	SHEET 1 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 2 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 3 OF 9	



NOTES

UNLESS OTHERWISE SPECIFIED ALL

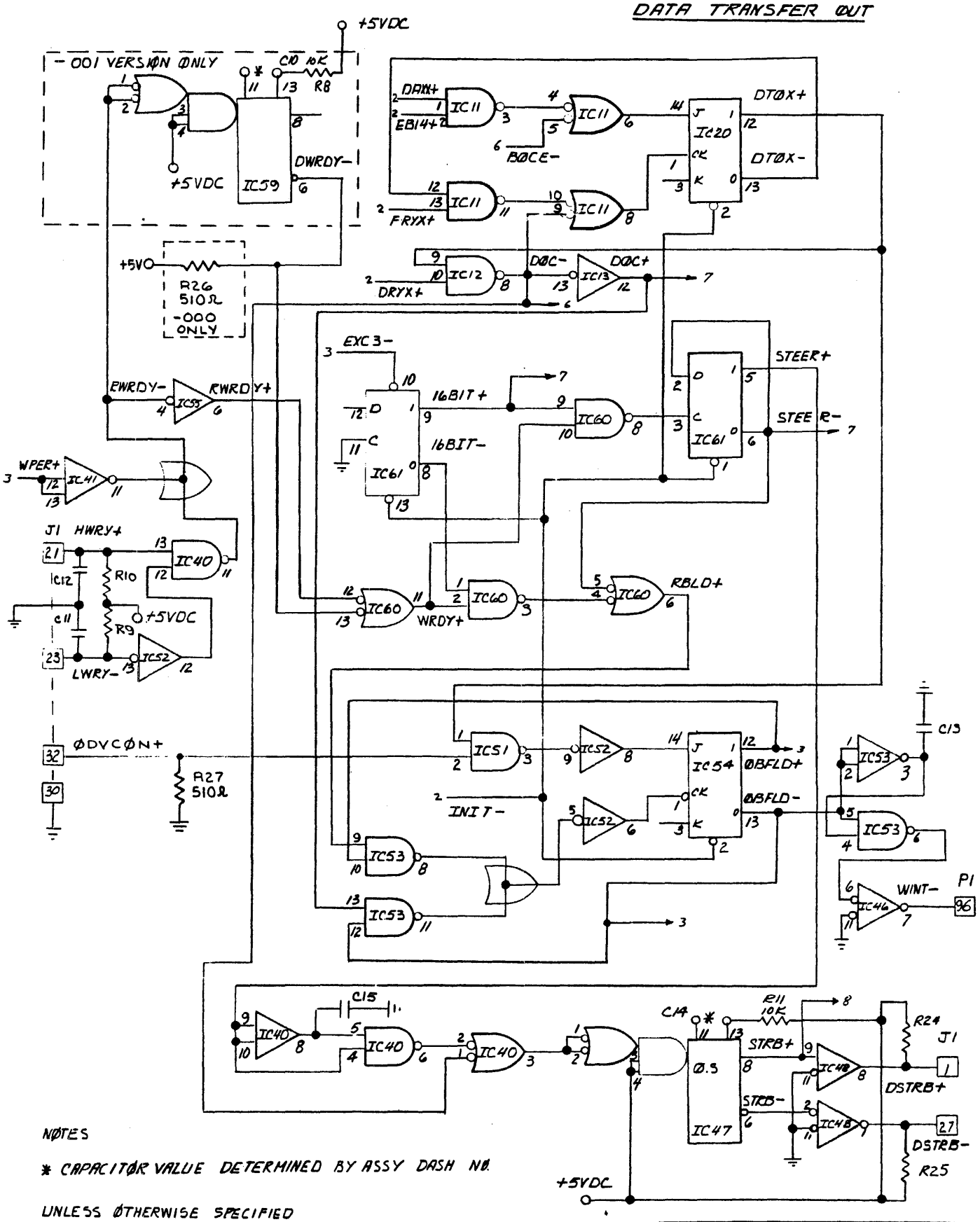
RESISTORS ARE 510 OHM 1/4 W

CAPACITORS ARE 680pf

DATA TRANSFER IN

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 4 OF 9	

DATA TRANSFER OUT



NØTES

* CAPACITØR VALUE DETERMINED BY ASSY DASH NØ.

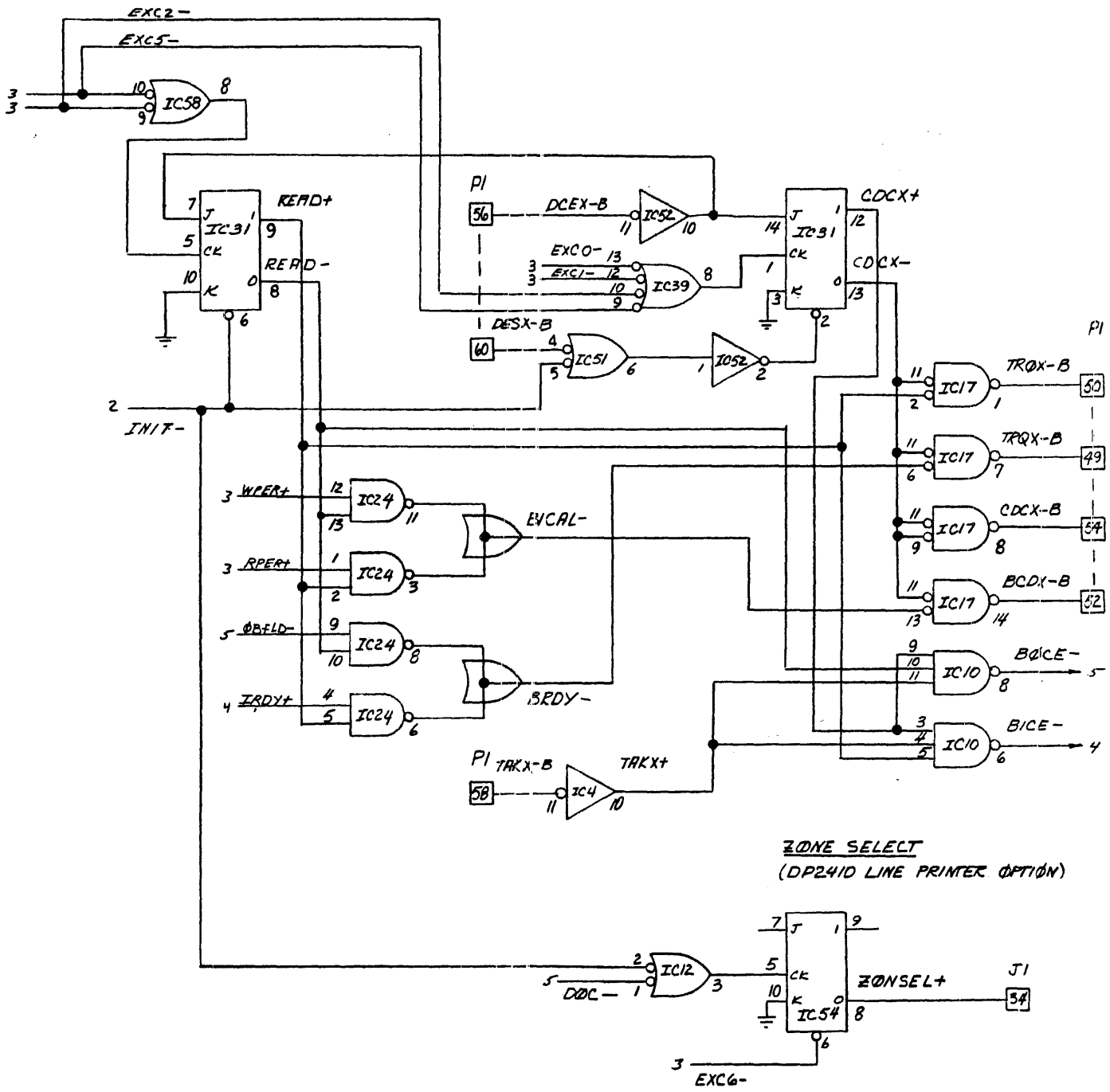
UNLESS ØTHERWISE SPECIFIED

CAPACITØR VALUES ARE 680 pf

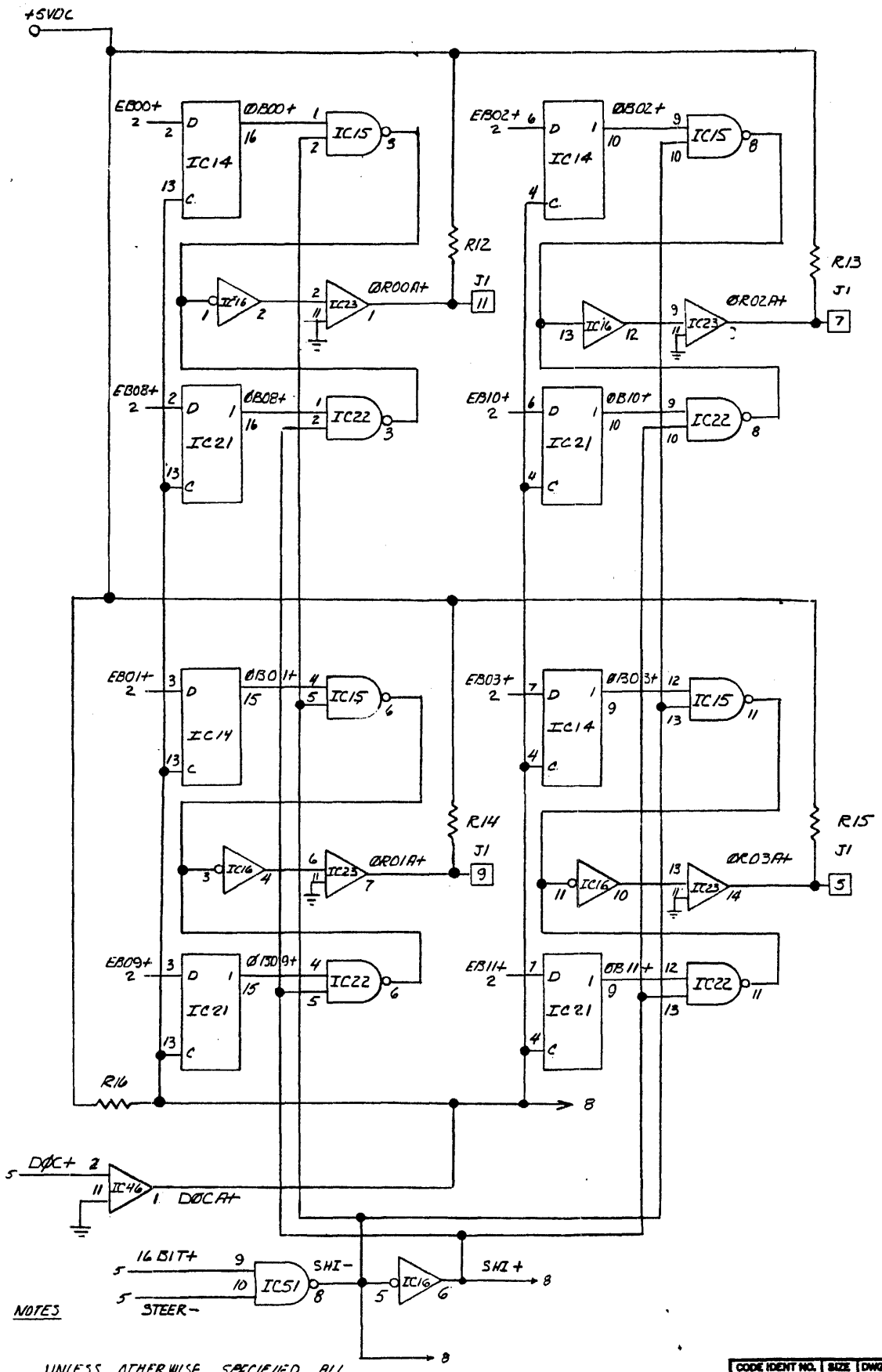
RESISTØR VALUES ARE 510 OHM 1/4 W

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 5 OF 9	

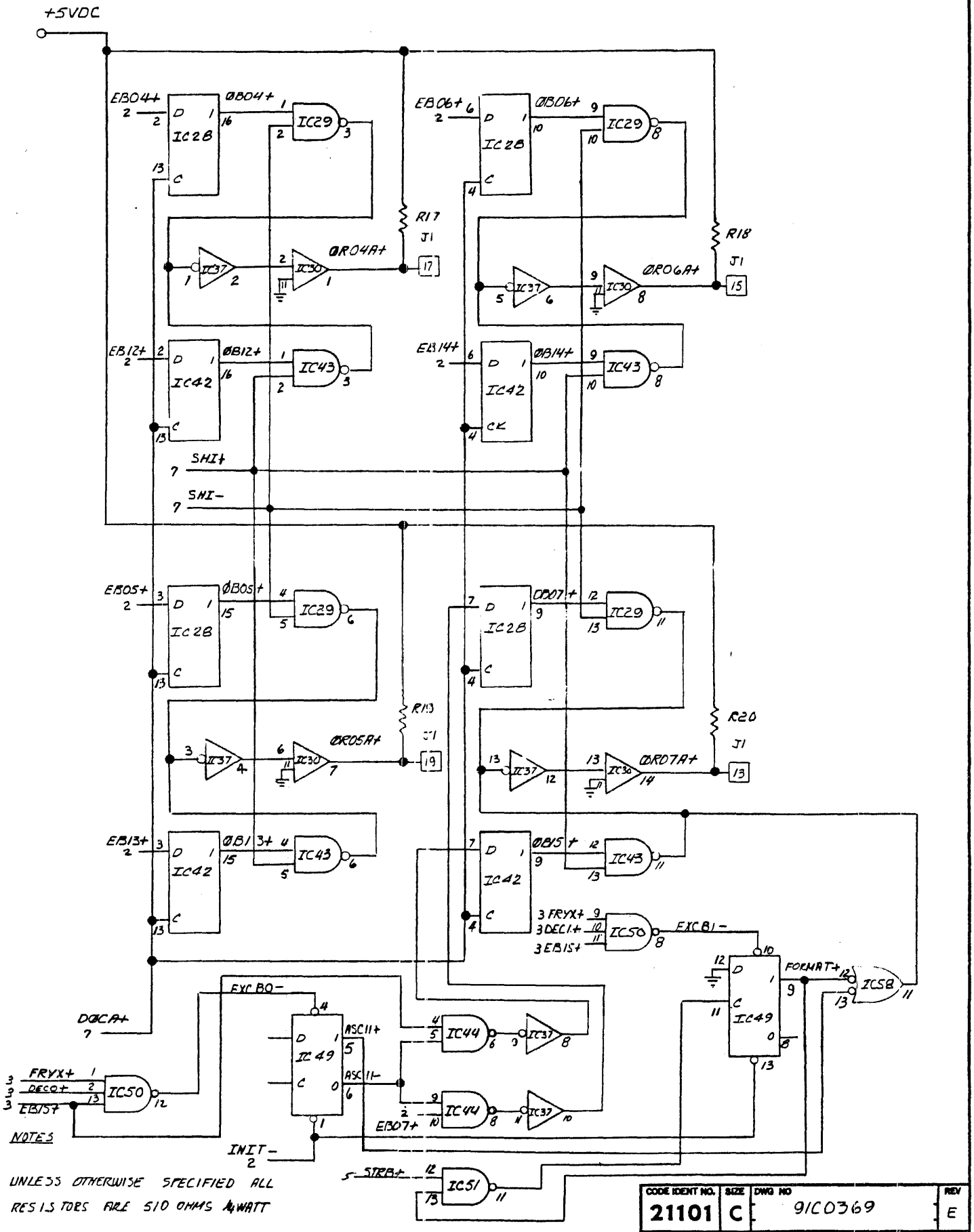
BIC CONTROL



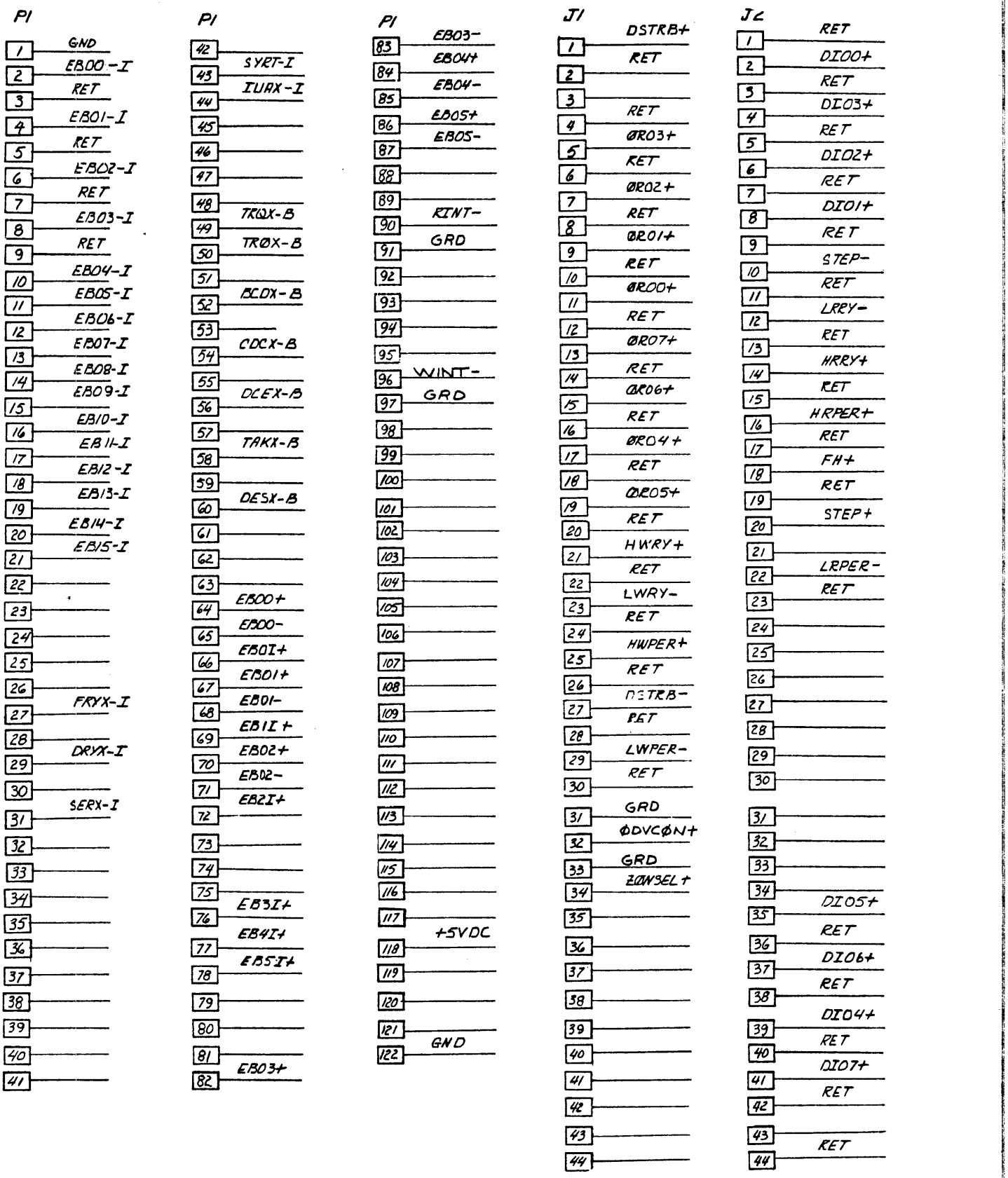
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 6 OF 9	



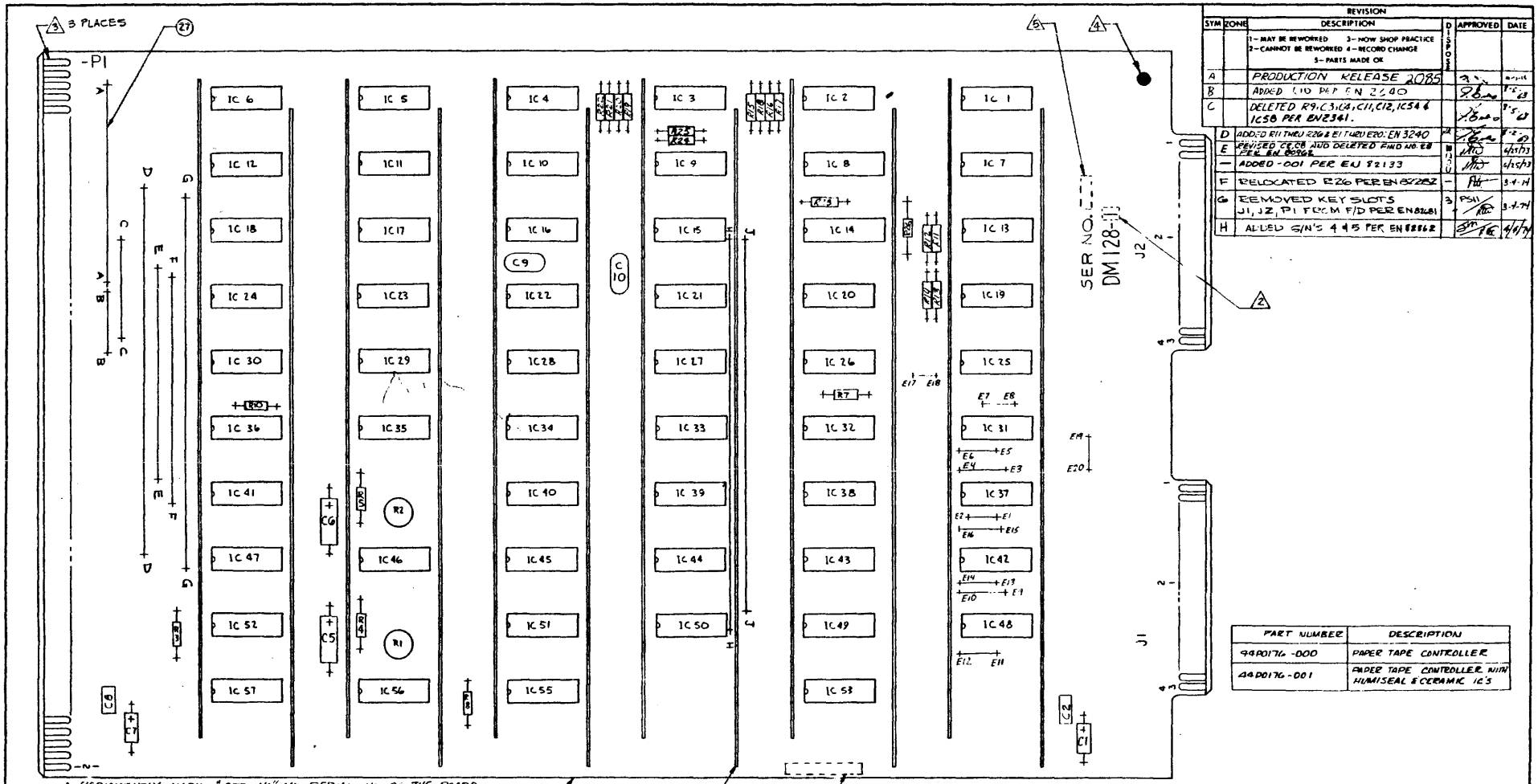
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 7 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 8 OF 9	



CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0369	E
SCALE		SHEET 9 OF 9	



REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1 – MAY BE REWORKED 3 – NOW SHOP PRACTICE 2 – CANNOT BE REWORKED 4 – RECORD CHANGE 5 – PARTS MADE OK			
A		PRODUCTION RELEASE 2085			
B		ADDED C10 PER EN 2640			7-5-73
C		DELETED R9, C3, C4, C11, C12, IC5 & 6 IC58 PER EN2341.			7-5-73
D		ADDED R11 THRU R226 & E1 THRU E20: EN 3240	M		7-2-73
E		REVISED CR, CB AND DELETED FIND NO. E8 PER EN 80962	M		4/25/73
—		ADDED -001 PER EN 82133	M		4/25/73
F		RELOCATED R26 PER EN 82282	—		3-1-74
G		REMOVED KEY SLOTS J1, J2, P1 FROM F/D PER EN 81281	B	PSH	3-1-74
H		ADDED S/N'S 4 & 5 PER EN 82862			4/8/74

PART NUMBER	DESCRIPTION
44D0176-000	PAPER TAPE CONTROLLER
44D0176-001	PAPER TAPE CONTROLLER WITH HUMISEAL & CERAMIC ICS

3 PERMANENTLY MARK "SER NO" AND SERIAL NO. OF THE BOARD IN .12 HIGH CHARACTERS APPROX WHERE SHOWN.

4 PERMANENTLY APPLY .3 YELLOW DOT TO BOARD APPROX WHERE SHOWN.

5 AFTER FINAL TEST AND PRIOR TO ACCEPTANCE TEST (-001 ONLY) MASK OFF CONNECTOR CONTACT AREA, BOTH SIDES OF F/N 1 AND TOTALLY COAT BOTH SIDES OF ASSEMBLY WITH F/N 40

2 MARK APPLICABLE VERSION (A) .19 HIGH PERMANENT CHARACTERS LOCATE APPROX. WHERE SHOWN.

1 MARK PART NUMBER 44D0176-(APPLICABLE VERSION) AND REVISION LETTER OF PARTS LIST TO WHICH PART WAS MANUFACTURED IN .12 HIGH PERMANENT CHARACTERS. LOCATE APPROX. WHERE SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS
91D0018 . . LOGIC DIAGRAM
91D0132 . . PHOTOMASTER
40D0199 . . BOARD DETAIL
44D0176 . . PARTS LIST

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

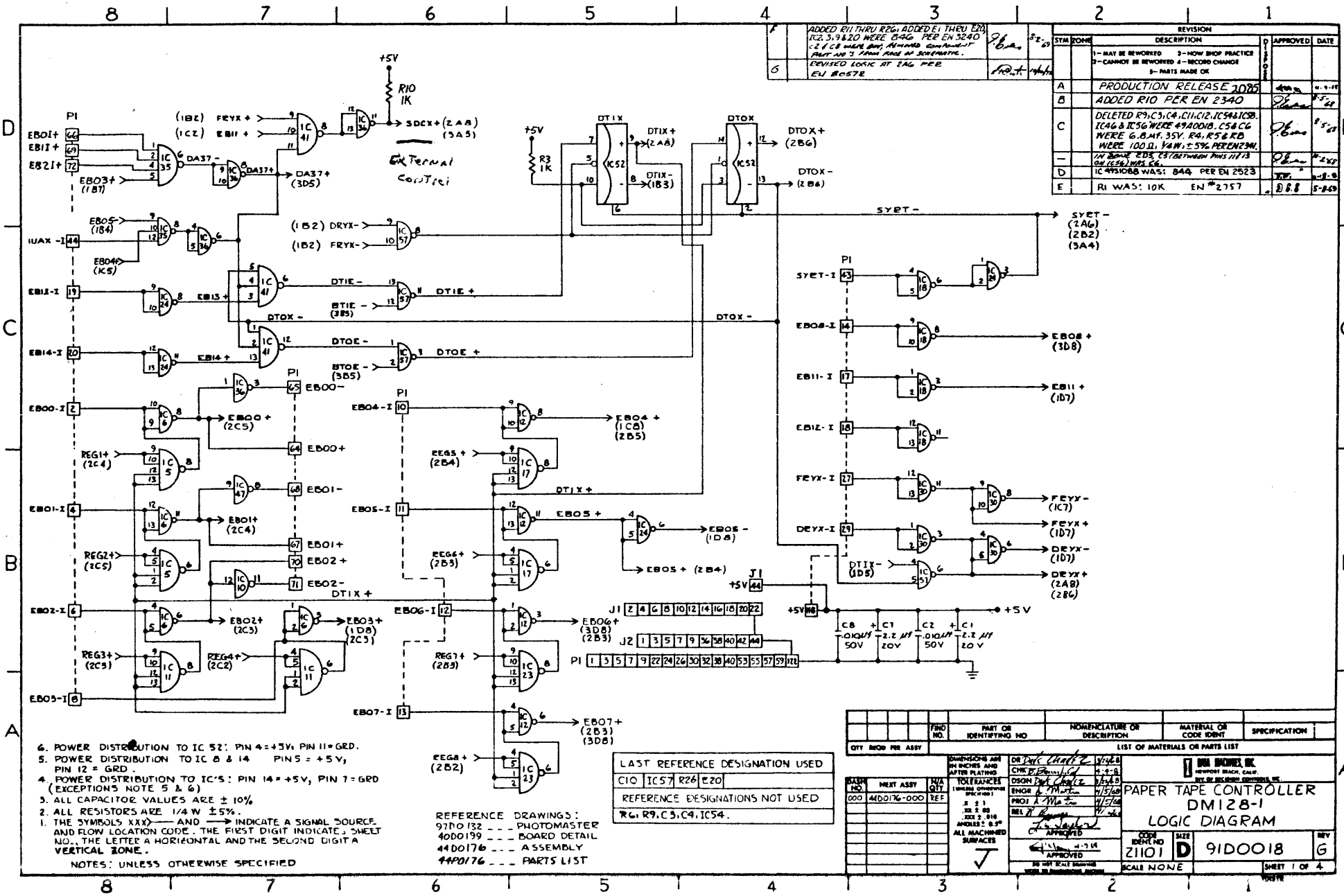
DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR Earl Christy 7/6/73
CHK [illegible] 7-9-73
DSGN [illegible]
ENGR [illegible]
PROJ [illegible]
REL A [illegible]
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS ONLY

PAPER TAPE CONTROLLER
DM 128-1
ASSEMBLY

CODE IDENT NO	SIZE		REV
21101	D	44D0176	H
SCALE 2/1		SHEET 1 OF 1	



SYM	ZONE	REVISION DESCRIPTION	APPROVED	DATE
		1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE 2 - CANNOT BE REWORKED 4 - RECORD CHANGE 5 - PARTS MADE OK		
A		PRODUCTION RELEASE 2085		4-9-69
B		ADDED R10 PER EN 2340		8-5-68
C		DELETED R3, C3, C4, C11, C12, IC58 & IC59. IC46 & IC56 WERE 4940018. C58 & C6 WERE 6.8 MF. 35V. R4, R5 & R8 WERE 100 Ω, ¼W, ± 5% PER EN 2341.		8-5-68
—		IN ZONE 2B5, C8 BETWEEN PINS 11 & 13 ON IC56 WAS C6.		4-8-9
D		IC 4931088 WAS: 844 PER EN 2523		5-8-69
E		R1 WAS: 10K EN #2757		5-8-69

SYM	ZONE		REVISION DESCRIPTION	APPROVED	DATE
F			ADDED R11 THRU R26; ADDED E1 THRU E20; IC2, 3, 9 & 20 WERE 846 PER EN 3240 C2 & C8 WERE 6MF; REMOVED COMPONENT PART NO'S FROM PAGE OF SCHEMATIC.		8-2-69
G			REVISED LOGIC AT 2A6 PER EN 80572		10-6-69

6. POWER DISTRIBUTION TO IC 52: PIN 4 = +5V, PIN 11 = GRD.
5. POWER DISTRIBUTION TO IC 8 & 14 PIN 5 = +5V, PIN 12 = GRD.
4. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GRD (EXCEPTIONS NOTE 5 & 6)
3. ALL CAPACITOR VALUES ARE ± 10%
2. ALL RESISTORS ARE 1/4 W ±5%.
1. THE SYMBOLS XXX ——— AND ———→ INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED				
C10	IC57	R26	E20	
REFERENCE DESIGNATIONS NOT USED				
R6, R9, C3, C4, IC54.				

REFERENCE DRAWINGS:
91D0132 - - - PHOTOMASTER
90D0199 - - - BOARD DETAIL
44D0176 - - - ASSEMBLY
44P0176 - - - PARTS LIST

FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION	QTY REQD PER ASSY
		LIST OF MATERIALS OR PARTS LIST			

BASIC NO.	NEXT ASSY	N/A QTY
000	44D0176-000	REF

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± 1
.XX ± 03
.XXX ± 010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR	Dale Chaffee	3/4/68
CHK	[illegible]	4-4-68
DSGN	Dale Chaffee	3/24/69
ENGR	A. Martin	4/5/68
PROJ	A. Martin	4/5/68
REL	[illegible]	4/5/68
	APPROVED	
	[illegible] 4-9-69 APPROVED	

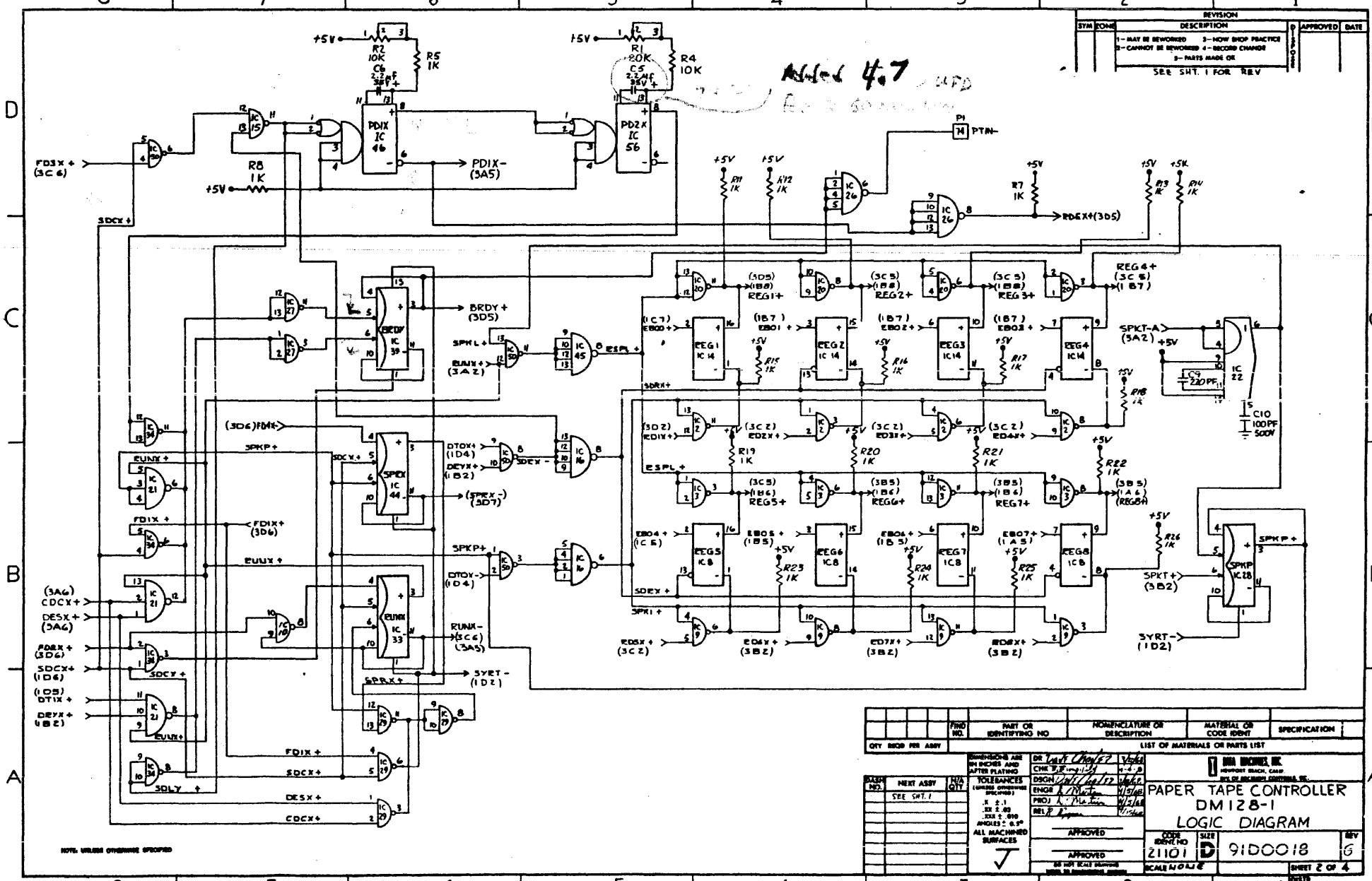
DO NOT SCALE DRAWING

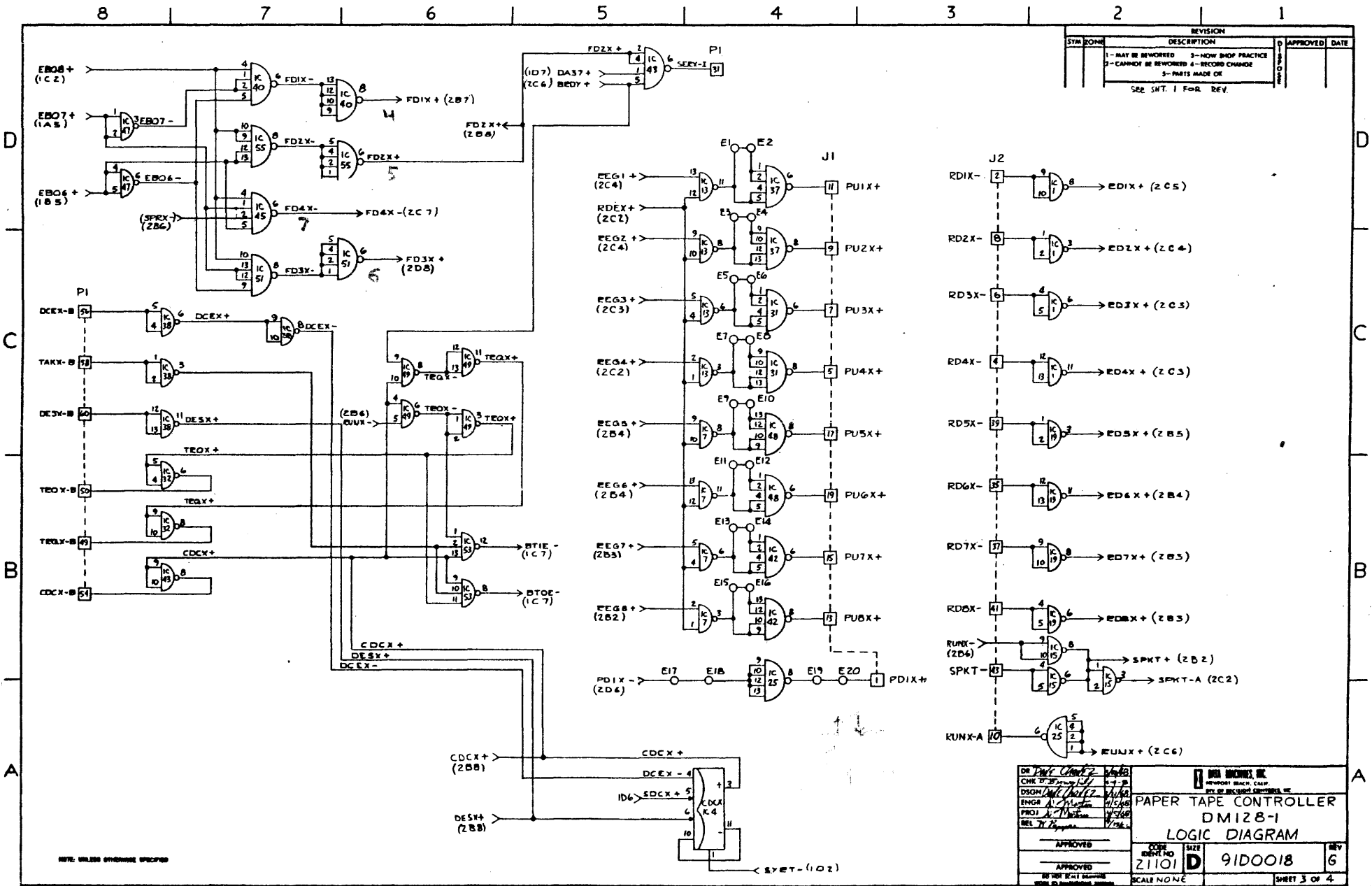
DIGI DYNAMICS, INC. NEWPORT BEACH, CALIF.

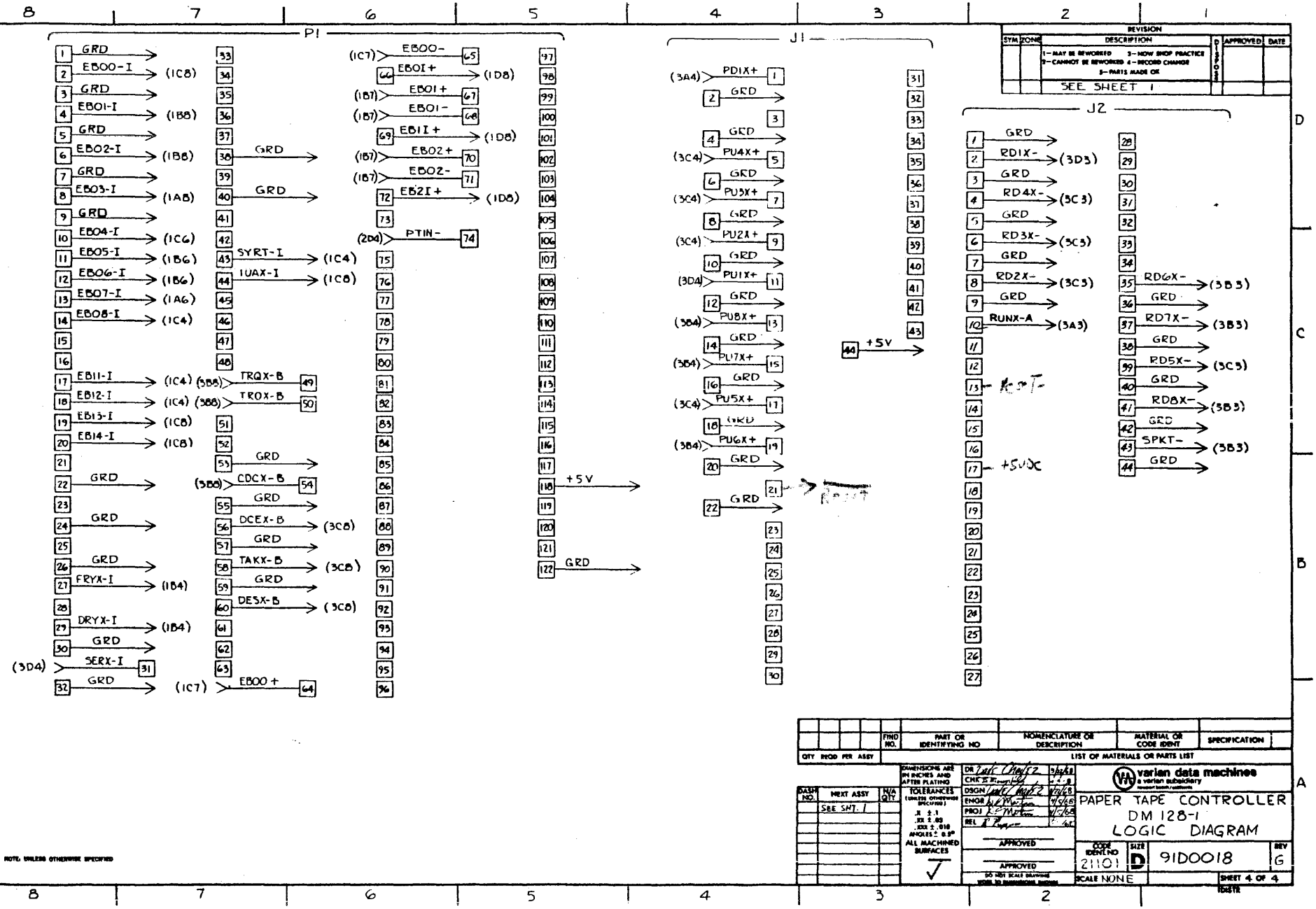
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM

CODE IDENT NO	SIZE	DWG NO	REV
21101	D	91D0018	G

SCALE NONE SHEET 1 OF 4


REVISION
SEE SHT. 1 FOR REV
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM
91D0018
SHEET 2 OF 4
PDIX-
(3A5)
PDEX+(3D5)
PTIN-
BRDY+
(3D5)
SPKT-A
(3A2)
SPKT+
(3B2)
SYRT-
(1D2)
RUNK-
(3C6)
(3A5)
SYET-
(1D2)
REG1+
REG2+
REG3+
REG4+
REG5+
REG6+
REG7+
REG8+
PDIX+
(3D6)
SPKP+
RUNX+
SDCX+
SDEX+
SPRX+
SDLY+
DESX+
CDCX+
FDIX+
FDEX+
SDRX+
SPKI+
ESPL+


REVISION
STM ZONE DESCRIPTION DATE APPROVED
1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE
2 - CANNOT BE REWORKED 4 - RECORD CHANGE
5 - PARTS MADE OK
SEE SHT. 1 FOR REV.
EB08+ (1C2)
EB07+ (1A5)
EB06+ (1B5)
(SPRX-) (2B6)
FD1X+ (2B7)
FD4X-(2C7)
FD3X+ (2D8)
FD2X+ (2B8)
(1D7) DA37+
(2C6) BEDY+
SERY-1
P1
DCEX-B
TAKX-B
DESX-B
TEQX-B
TEQX-B
CDCX-B
DCEX+
DCEX-
TEQX+
TEQX-
TEQX+
(2B6) CLRX-
TEQX+
CDCX+
DESX+
DCEX-
BTIE-(1C7)
BTOE-(1C7)
J1
EEG1+ (2C4)
RDEX+ (2C7)
EEG2+ (2C4)
EEG3+ (2C3)
EEG4+ (2C2)
EEG5+ (2B4)
EEG6+ (2B4)
EEG7+ (2B3)
EEG8+ (2B2)
PU1X+
PU2X+
PU3X+
PU4X+
PU5X+
PU6X+
PU7X+
PU8X+
PD1X- (2D6)
PD1X+
J2
RD1X-
RD2X-
RD3X-
RD4X-
RD5X-
RD6X-
RD7X-
RD8X-
RUNX- (2D6)
SPKT-
RUNX-A
ED1X+ (2C5)
ED2X+ (2C4)
ED3X+ (2C3)
ED4X+ (2C3)
ED5X+ (2B5)
ED6X+ (2B4)
ED7X+ (2B3)
ED8X+ (2B3)
SPKT+ (2B2)
SPKT-A (2C2)
RUNX+ (2C6)
CDCX+ (2B8)
DESX+ (2B8)
CDCX+
DCEX-
SDCX+
SYET-(1D2)
PAPER TAPE CONTROLLER
DM128-1
LOGIC DIAGRAM
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DATA MACHINES, INC.
CODE IDENT NO 21101
SIZE D
91D0018
REV 6
SCALE NONE
SHEET 3 OF 4



REVISION					
SYM	ZONE	DESCRIPTION		APPROVED	DATE
		1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE 2 - CANNOT BE REWORKED 4 - RECORD CHANGE 5 - PARTS MADE OK			
		SEE SHEET 1			

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY	LIST OF MATERIALS OR PARTS LIST			

ASSY NO.	NEXT ASSY	N/A QTY
	SEE SHT. 1	

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES √

DR	Carl Chaffee	3/4/68
CHK	S Frumkin	3-4-68
DSGN	Carl Chaffee	3/4/68
ENGR	L F Martin	4/5/68
PROJ	L F Martin	4/5/68
REL	[illegible]	[illegible]

APPROVED

APPROVED

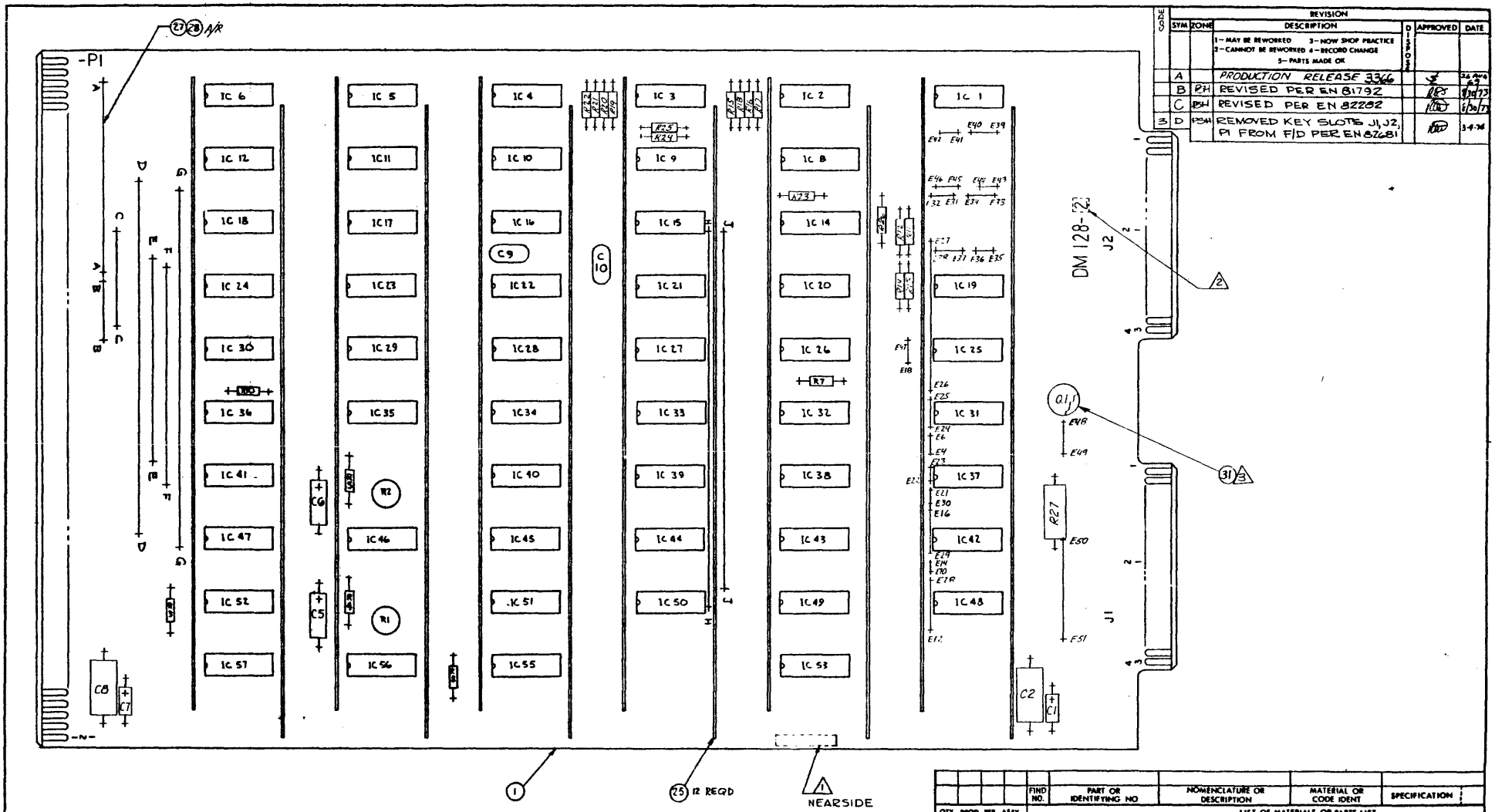
DO NOT SCALE DRAWING
WORK TO DIMENSIONS SHOWN

varian data machines
a varian subsidiary
newport beach, california

PAPER TAPE CONTROLLER
DM 128-1
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0018	G
SCALE NONE			SHEET 4 OF 4

NOTE: UNLESS OTHERWISE SPECIFIED



CODE	SYM	ZONE	REVISION DESCRIPTION (1 – MAY BE REWORKED 2 – CANNOT BE REWORKED 3 – NOW SHOP PRACTICE 4 – RECORD CHANGE 5 – PARTS MADE OK)	DISPOSITION	APPROVED	DATE
	A		PRODUCTION RELEASE 3366			24 APR 69
	B	PH	REVISED PER EN 81792			9/9/73
	C	PSH	REVISED PER EN 82282			1/30/74
3	D	PSH	REMOVED KEY SLOTS J1, J2, P1 FROM F/D PER EN 82681			3-4-74

FIND NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY		LIST OF MATERIALS OR PARTS LIST		

DASH NO.	NEXT ASSY	N/A QTY

DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED)
.X ± .1
.XX ± .03
XXX ± .010
ANGLES ± 0.5°
ALL MACHINED SURFACES

DR		11/2/69
CHK		7-31-69
DSGN		7/21/69
ENGR		
PROJ		
REL		

APPROVED

APPROVED

DO NOT SCALE DRAWING

DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF BECKMAN CONTROLS, INC.

PAPER TAPE CONTROLLER ASSY, DM 128-2 (120 CPS)

CODE IDENT NO	SIZE	DWG NO	REV
21101	D	44D0311	D

SCALE 2/1 SHEET 1 OF 1

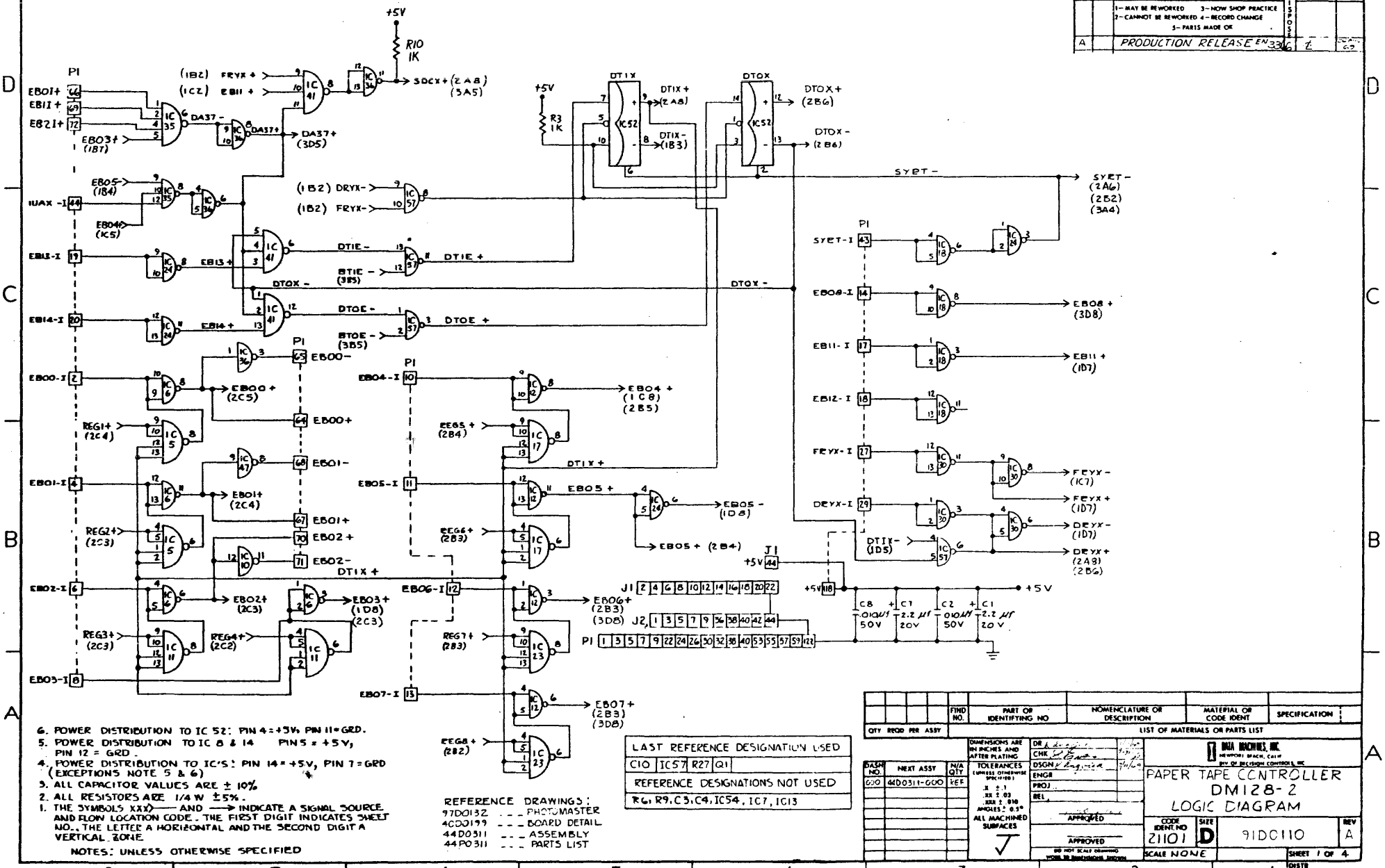
3 USE OF TRANSISTOR MOUNTING PADS OPTIONAL.

2 RUBBER STAMP VERSION APPROX WHERE SHOWN: USE .19 HIGH NUMBER AND BLACK ACID ETCH INK.

1 RUBBER STAMP CURRENT PARTS LIST NO., VERSION AND REVISION LETTER APPROX. WHERE SHOWN, USE .12 HIGH CHARACTERS AND BLACK ACID ETCH INK.

NOTE: UNLESS OTHERWISE SPECIFIED

REFERENCE DRAWINGS
91D0110 ___ LOGIC DIAGRAM
97D0132 ___ PHOTOMASTER
40D0199 ___ BOARD DETAIL
44P0311 ___ PARTS LIST



6. POWER DISTRIBUTION TO IC 52: PIN 4 = +5V, PIN 11 = GRD.
5. POWER DISTRIBUTION TO IC 8 & 14 PIN 5 = +5V, PIN 12 = GRD.
4. POWER DISTRIBUTION TO IC'S: PIN 14 = +5V, PIN 7 = GRD (EXCEPTIONS NOTE 5 & 6)
3. ALL CAPACITOR VALUES ARE ± 10%
2. ALL RESISTORS ARE 1/4 W ±5%.
1. THE SYMBOLS XXX⟩—— AND ——⟩ INDICATE A SIGNAL SOURCE AND FLOW LOCATION CODE. THE FIRST DIGIT INDICATES SHEET NO., THE LETTER A HORIZONTAL AND THE SECOND DIGIT A VERTICAL ZONE.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED
C10 IC57 R27 Q1
REFERENCE DESIGNATIONS NOT USED
R6, R9, C3, C4, IC54, IC7, IC13

REFERENCE DRAWINGS:
97D0132 ___ PHOTOMASTER
4CD0199 ___ BOARD DETAIL
44D0311 ___ ASSEMBLY
44P0311 ___ PARTS LIST

REVISION					
SYM	ZONE	DESCRIPTION	DISPOSITION	APPROVED	DATE
		1- MAY BE REWORKED 3- NOW SHOP PRACTICE 2- CANNOT BE REWORKED 4- RECORD CHANGE 5- PARTS MADE OR			
A		PRODUCTION RELEASE EN 33	C	Z	

FIND NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL OR CODE IDENT	SPECIFICATION
QTY REQD PER ASSY	LIST OF MATERIALS OR PARTS LIST			

DASH NO.	NEXT ASSY	N/A QTY
000	44D0311-000	REF

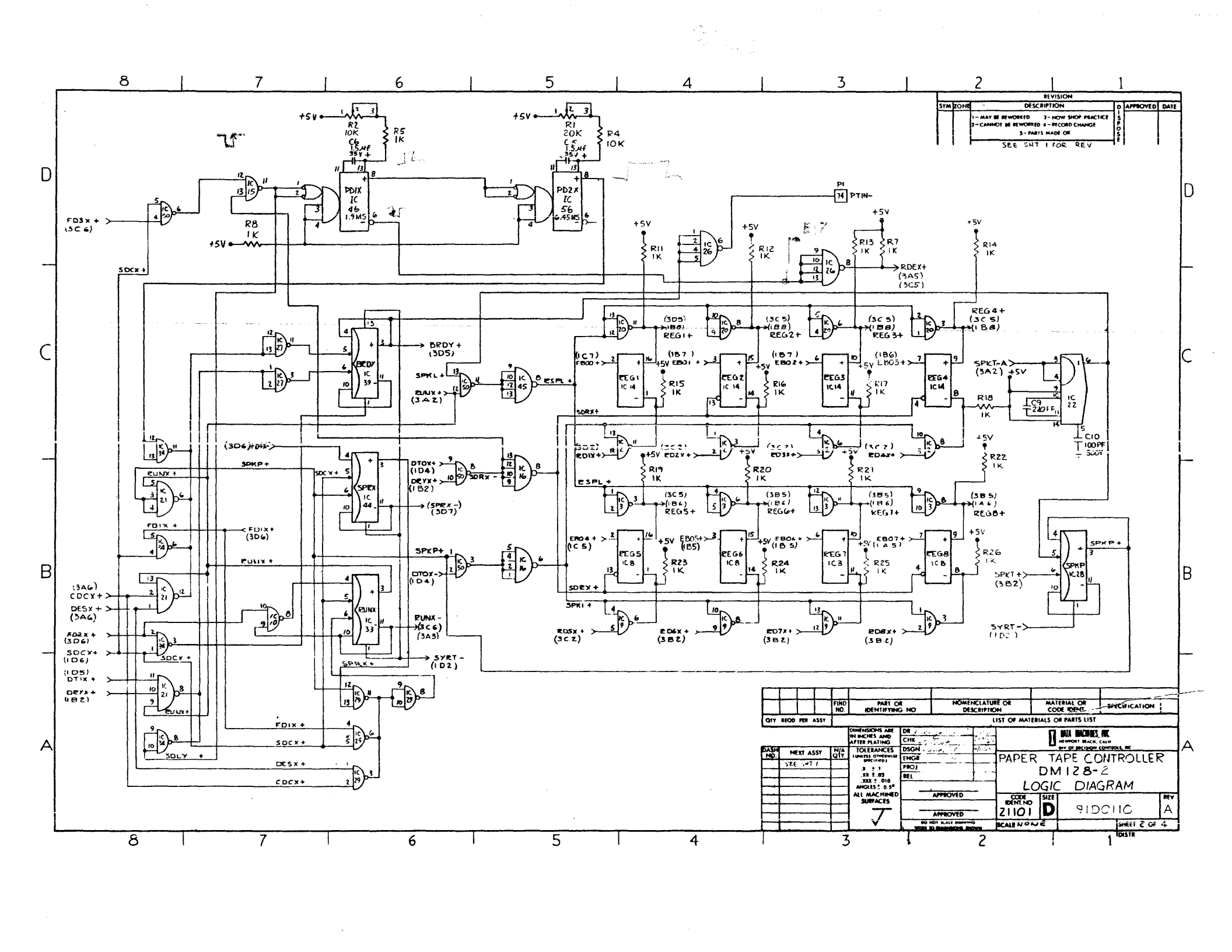
DIMENSIONS ARE IN INCHES AND AFTER PLATING
TOLERANCES (UNLESS OTHERWISE SPECIFIED) .X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 0.5° ALL MACHINED SURFACES

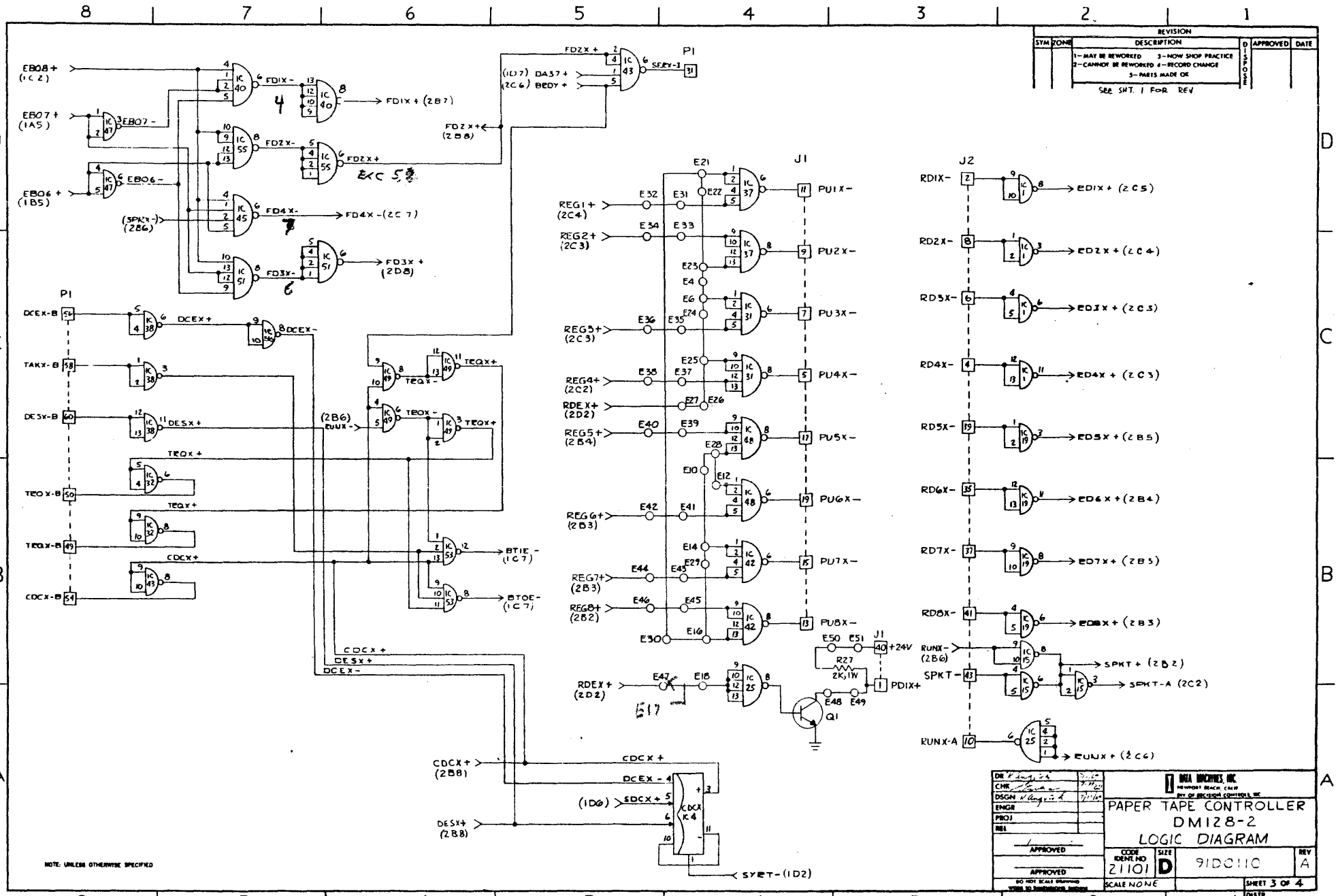
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING WORK TO DIMENSIONS SHOWN

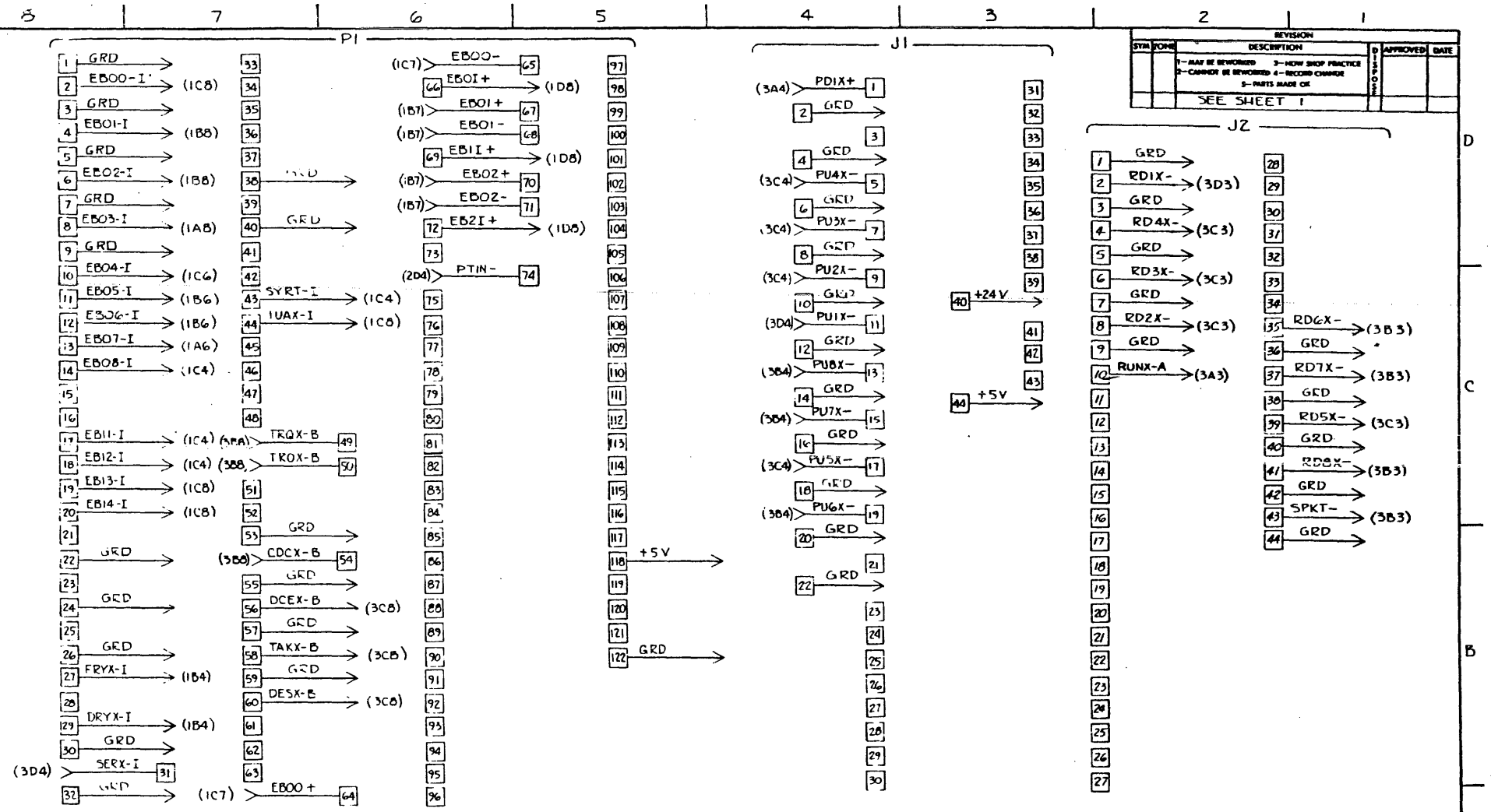
DATA DYNAMICS, INC. NEWPORT BEACH, CALIF. DIV. OF BECKMAN CONTROLS, INC.

PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0110	A
SCALE NONE		SHEET 1 OF 4	


REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1 - MAY BE REWORKED 3 - NOW SHOP PRACTICE
2 - CANNOT BE REWORKED 4 - RECORD CHANGE
5 - PARTS MADE OR
SEE SHT 1 FOR REV
PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM
DATA MACHINES, INC.
CODE IDENT NO 21101
SIZE D
91D0110
REV A
SCALE NONE
SHEET 2 OF 4
LIST OF MATERIALS OR PARTS LIST
FIND NO. PART OR IDENTIFYING NO. NOMENCLATURE OR DESCRIPTION MATERIAL OR CODE IDENT. SPECIFICATION
QTY REQD PER ASSY
DASH NO. NEXT ASSY N/A QTY
TOLERANCES
ALL MACHINED SURFACES
APPROVED
APPROVED
DR CHK DSGN ENGR PROJ REL
PTIN-
RDEX+ (3A5) (3C5)
BRDY+ (3D5)
SPKT-A (3A2)
SPKT+ (3B2)
SYRT- (1D2)
RUNX+ (3A2)
RUNX- (3C6) (3A3)
SPRX+
SDCX+
SDLY+
DESX+
CDCX+
FD3X+ (3C6)
FD2X+ (3D6)
SDCX+ (1D6)
(1D5) DTIX+
DEYX+ (1B2)
(3A6) CDCX+
DESX+ (3A6)
FDIX+ (3D6)
SPKP+
DTOX- (1D4)
DEYX+ (1B2)
(SPRX-) (3D7)
SDRX+
ESPL+
REG1+
REG2+
REG3+
REG4+
REG5+
REG6+
REG7+
REG8+
EB00+
EB01+
EB02+
EB03+
EB04+
EB05+
EB06+
EB07+
RDIX+
RDEX+
RD3X+
RD4X+
RDSX+
RD6X+
RD7X+
RD8X+
PDIX IC 46 1.9MS
PD2X IC 56 6.45MS
R1 20K
R2 10K
R4 10K
R5 1K
R7 1K
R8 1K
R11 1K
R12 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R21 1K
R22 1K
R23 1K
R24 1K
R25 1K
R26 1K
C5 1.5MF 35V
C6 1.5MF 35V
C9 .2MFD
C10 100PF 300V


REVISION
SYM ZONE DESCRIPTION APPROVED DATE
1-MAY BE REWORKED 3-NOW SHOP PRACTICE
2-CANNOT BE REWORKED 4-RECORD CHANGE
5-PARTS MADE OK
SEE SHT. 1 FOR REV.
EB08+ (1C2)
EB07+ (1A5)
EB07-
EB06+ (1B5)
EB06-
FDIX-
FD2X-
FD4X-
FD3X-
FDIX+ (2B7)
FD2X+ (2B8)
FD4X-(2C7)
FD3X+ (2D8)
FDZX+
(1D7) DA37+
(2C6) BEDY+
SERV-1
P1
DCEX-B
TAKX-B
DESX-B
TEQX-B
CDCX-B
DCEX+
DCEX-
TEQX+
TEQX-
BTIE- (1C7)
BTOE- (1C7)
(2B6) EUUX-
CDCX+
DESX+
DCEX-
CDCX+ (2B8)
DESX+ (2B8)
(1D6) SDCX+
SYET-(1D2)
J1
REG1+ (2C4)
REG2+ (2C3)
REG3+ (2C3)
REG4+ (2C2)
RDEX+ (2D2)
REG5+ (2B4)
REG6+ (2B3)
REG7+ (2B3)
REG8+ (2B2)
PU1X-
PU2X-
PU3X-
PU4X-
PU5X-
PU6X-
PU7X-
PU8X-
+24V
R27 2K,1W
PDIX+
Q1
RDEX+ (2D2)
J2
RDIX-
RD2X-
RD3X-
RD4X-
RD5X-
RD6X-
RD7X-
RD8X-
RUNX-(2B6)
SPKT-
RUNX-A
EDIX+ (2C5)
ED2X+(2C4)
ED3X+(2C3)
ED4X+(2C3)
ED5X+(2B5)
ED6X+(2B4)
ED7X+(2B5)
ED8X+(2B3)
SPKT+(2B2)
SPKT-A (2C2)
EUUX+(2C6)
NOTE: UNLESS OTHERWISE SPECIFIED
DR
CHK
DSGN
ENGR
PROJ
REL
APPROVED
APPROVED
DO NOT SCALE DRAWING
DATA MACHINES, INC.
NEWPORT BEACH, CALIF.
DIV. OF DECISION CONTROLS, INC
PAPER TAPE CONTROLLER
DM128-2
LOGIC DIAGRAM
CODE IDENT. NO 21101
SIZE D
91D0110
REV A
SCALE NONE
SHEET 3 OF 4
DISTR



DASH NO.	NEXT ASSY	N/A QTY
	SEE SHT. 1	

NOTE: UNLESS OTHERWISE SPECIFIED

varian data machines
a varian subsidiary

PAPER TAPE CONTROLLER
DM 128-2
LOGIC DIAGRAM

CODE IDENT NO	SIZE		REV
21101	D	91D0110	A

SCALE NONE SHEET 4 OF 4