TELETYPE CONTROLLER

an option for the
Varian Data Machines 620/f
Computer System

Specifications Subject to Change Without Notice

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FOREWORD

The 620/f Teletype Controller Manual defines and explains the logical, electrical, and mechanical parameters that control the interface between a 620/f and a TTY.

The six sections of the manual:

- Introduce the controller in relation to the system
- Describe its installation and interfacing
- Give a detailed theory of operation
- Describe testing and troubleshooting procedures for maintaining it in the field
- Reference all hardware with drawings, parts lists, and wire lists

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SECTION 1
INTRODUCTION

1.1 SYSTEM OVERVIEW

The *Model 620/f Teletype Controller (TC)* is a mainframe option for the Varian Data Machines 620/f computer system. The TC controls the command and information transfer between the computer and a factory-modified Teletype (TTY).

The TC card contains all circuitry except for the transmit/receive clocks and relays K1 and K2 on the clock card. The TC plugs into the CPU tray, which slides into the mainframe of the computer. Each TC can control one TTY. If more are required, the additional circuit card and a special buffer card plug into an expansion chassis.

Memory access for the TC can be controlled directly by the CPU or indirectly through the I/O bus. If a system requires more than one TTY, the additional TC is indirectly controlled. A TTY buffer board (assembly 01A0688-000) is required for TTY/TCs 2 through 8. Additional TCs are 620/i-type units; they operate with the buffer interlace controller (BIC).

The factory-modified TTY controlled by the TC can be a model 33 ASR, 35 ASR, or 35 KSR. The ASR models have automatic send and receive facilities and include a paper tape reader and punch; the KSR model uses only keyboard-entered instructions and data.

1.2 FUNCTIONAL DESCRIPTION

The TC is functionally divided into seven circuits: input and output registers, input and output timing controls, TC/CPU interface, and TC/clock card/TTY interface (see figure 1-1).

1.2.1 Input Register

The input or read (R) register stores eight bits of data from the teletype. When the CPU generates an input data command, the R register places its data on the A bus.

1.2.2 Output Register

The output or write (W) register stores eight bits of data from the CPU. When the CPU generates an output data command, the W register is loaded from the bidirectional A bus.

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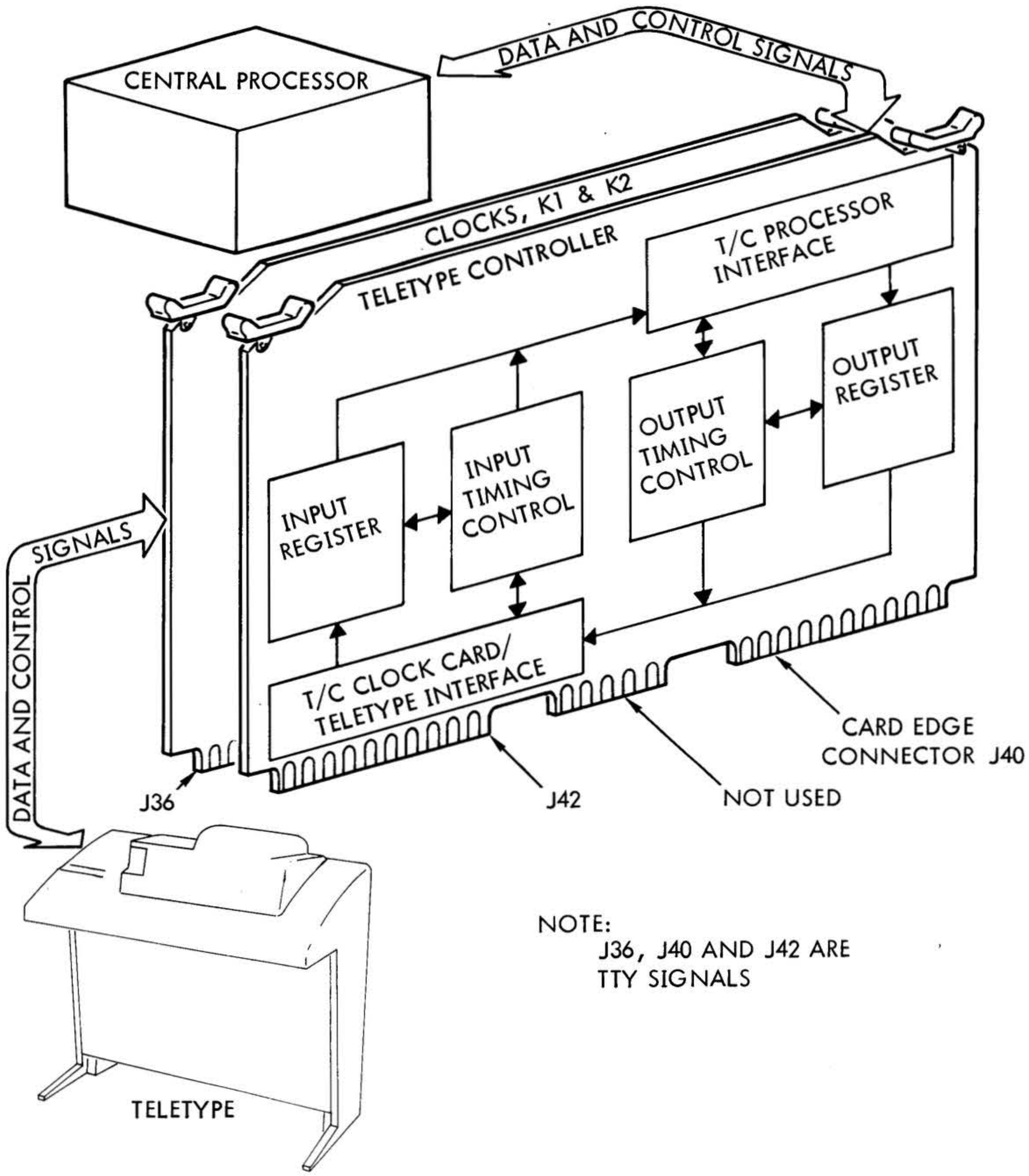

NOTE:
J36, J40 AND J42 ARE TTY SIGNALS

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Figure 1-1. Teletype Controller Functions

1.2.3 Input Timing Control

The input timing control circuit provides event storage, gating, and a 4.55-millisecond clock signal to regulate three input sequences. These sequences are: start data input, load the R register with input data from the TTY and transfer data to the CPU via the A bus.

1.2.4 Output Timing Control

The output timing control circuit provides event storage, gating, and a 9.1-millisecond clock signal to regulate two output sequences after the TC is ready to write. These sequences are: load the W register with output data from the CPU and transmit data to the TTY.

1.2.5 TC/CPU Interface

The TC/CPU interface circuit provides bidirectional A bus drivers and receivers for the respective R register and W register. This circuit also includes gating logic for control signals to and from the CPU.

1.2.6 TC/Clock Card/TTY Interface

The TC/clock card/TTY interface circuit provides two relays to transmit and receive serial data signals, respectively, to and from the TTY. This circuit also includes transmit/receive clocks and cabling between the TTY and the clock card. Operation between the TC and TTY is full-duplex, serial, and asynchronous. Appendix A gives TTY ASCII codes.

1.3 SPECIFICATIONS

The physical, electrical, and operating specifications of the TC are listed in table 1-1.

SECTION 1
INTRODUCTION

Table 1-1. Teletype Controller Specifications

Parameter	Description
Organization	Contains input and output registers, timing control circuitry for simultaneous two-way transmission, and CPU/TTY interface logic
Peripheral Device	A factory-modified TTY model 33 ASR, 35 ASR, or 35 KSR including a cable
Speed	TC operation is controlled by TTY speed. Ten characters per second (100 milliseconds per character) at either random or sustained rate
Modes	Input: from keyboard or paper tape Output: to typewriter or paper tape
Device Address	TC 001 (additional TCs, 002 through 007)
Sense Responses	Ready to read Ready to write
Memory Access Control	By CPU directly or indirectly
Types of Interrupt	Write ready and read ready interrupts available to a priority interrupt module (PIM)
Logic Levels	Positive logic
Internal	True: +2.4 to +5.5V dc False: 0.0 to +0.5V dc
Interrupts and CPU/TC Interface	True: 0.0 to +0.5V dc False: +2.4 to +5.0V dc

Table 1-1. Teletype Controller Specifications *(continued)*

Parameter	Description
BIC Capability	With additional 620/i-type controllers only
Size	Two 3-by-15-inch (7.7 x 38.1 cm) etched-circuit cards (TC and clock circuit card)
Interconnection	Interfaces with CPU, I/O bus, and TTY through mainframe backplane connector
Connectors	One 182-terminal card-edge connector (inserts in female connector on CPU tray). TTY connects to a three-terminal connector at rear of mainframe
Input Power	+5V dc at 1.25 amperes
Operational Environment	0 to 50 degrees C, 0 to 90 percent relative humidity without condensation.

2.1 PHYSICAL DESCRIPTION

The TC is on a 3-by-15-inch (7.7 x 38.1 cm) etched-circuit card (DM274). This is a socket card type 2 accommodating one 24-pin, four 16-pin, and sixty-four 14-pin sockets. All components are integrated circuits (ICs). All connections to the TC are through card-edge connectors P1, P2, and P3, which have 76, 30, and 76 pins, respectively. These mate with connectors J40, J41, and J42 on the CPU tray.

The clock board assembly is a printed circuit card type 3 for discrete components with the same dimensions and edge connector as the TC card (DM253). The edge connectors mate with connectors J34, J35, and J36 on the CPU tray (see figure 2-1).

Device address 001 is automatically wirewrapped; additional TC device addresses are handwired.

2.2 SYSTEM LAYOUT AND PLANNING

The TC circuit card is located in card slot 13 of the CPU tray. The card slots in the CPU tray, that is mounted in the mainframe, are numbered 1 through 14 from rear to front when facing the front panel. If a system includes more than one TC, the additional circuit cards are located in an expansion chassis and require special TTY buffer cards. Optional controllers and the TTY buffer are on 7.75-by-12-inch (19.7 x 30.3 cm) cards.

The clock card is located in card slot 11 on the CPU tray in the mainframe (figure 2-2).

2.3 SYSTEM INTERCONNECTION

The TC and clock circuit cards are inserted into their designated card slots when the CPU tray is extended out the front of the mainframe and held by an extender assembly bolted to the front of the mainframe. The cards are inserted into the mounting guides of slots 13 and 11 with the component side of the cards toward the backplane connectors.

Apply moderate pressure to seat the card-edge connectors firmly into the mating connectors on the CPU tray. To prevent damage to the connectors or to the nylon guides, apply even pressure across the top of the cards during insertion. The cards have ejector handles for unseating them from their mating connectors. The transmit (TTXX-T), receive (TTRX-T), and return (TTSR-T) lines extend from clock card slot 11, P3, at A30, A34, and A36, respectively, and connect to J13 at the rear of the CPU mainframe through P2 on the CPU tray. J13 mates to the TTY through a 20-foot cable.

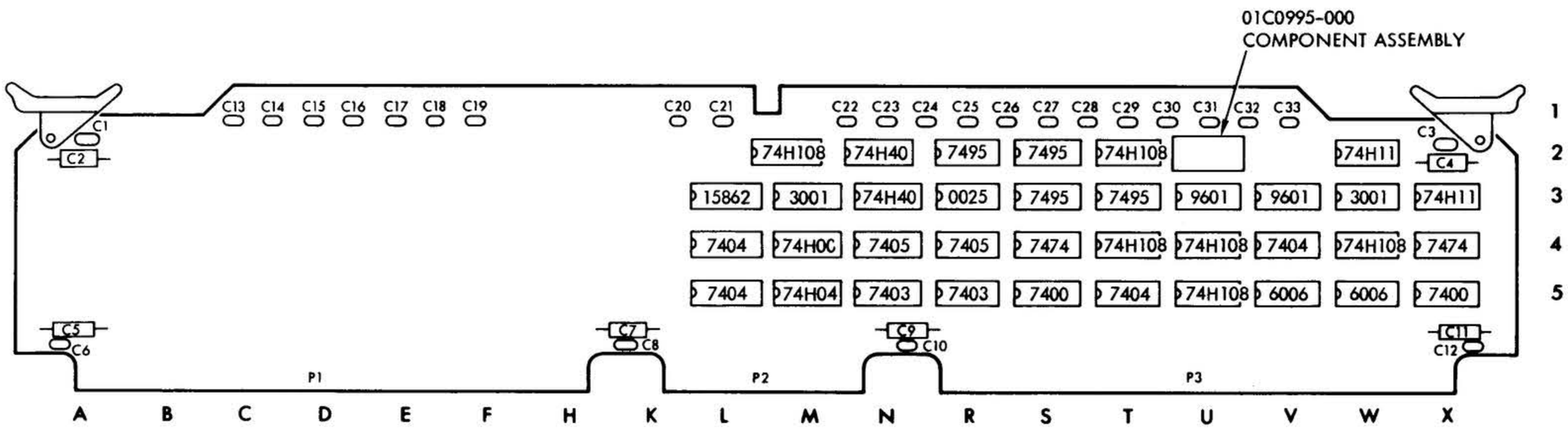

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Figure 2-1. TC Component Layout Assembly

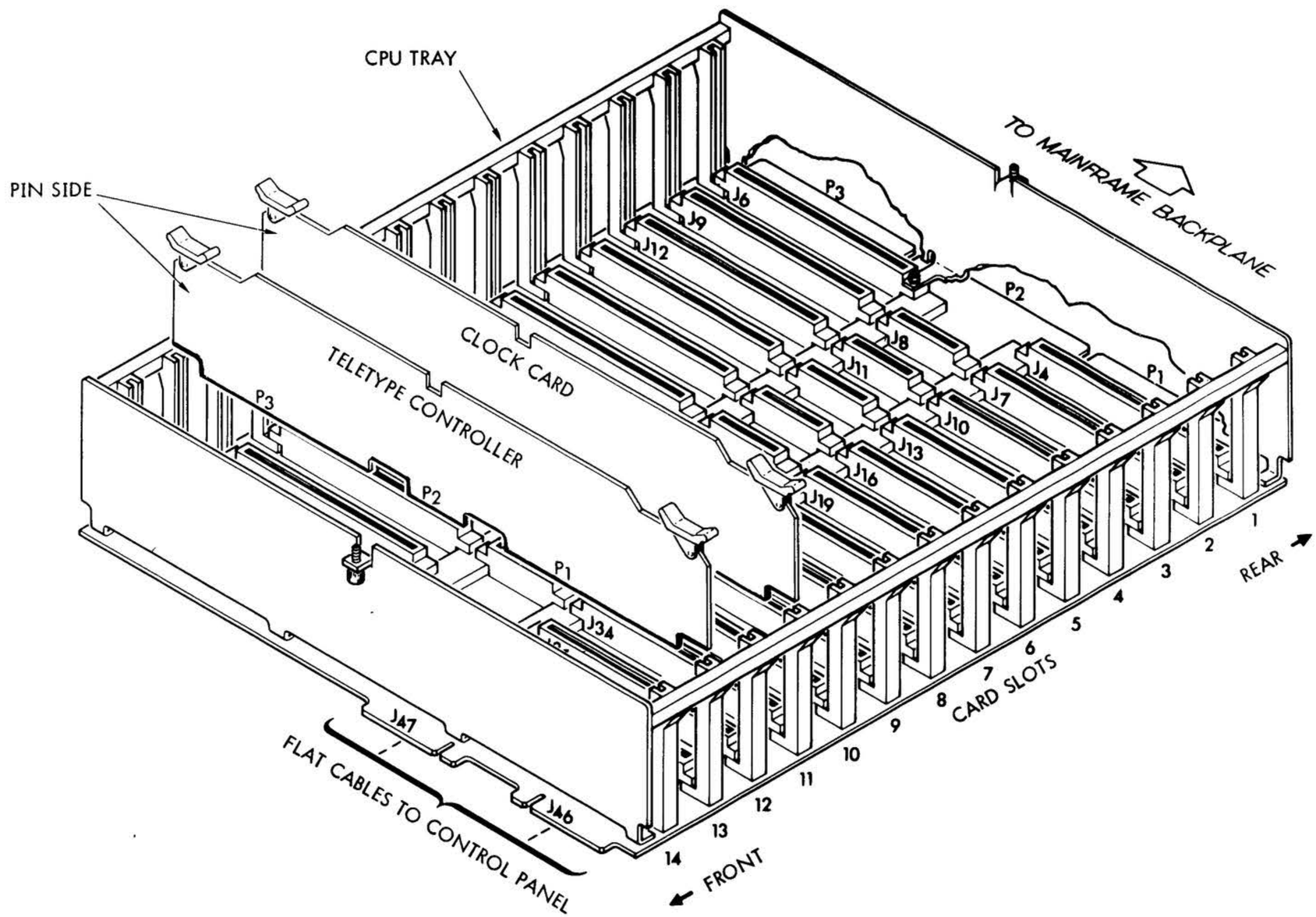

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Figure 2-2. Card Locations for TC and Clocks

2.4 SIGNAL INTERFACES

2.4.1 General

The TC interfaces with the basic computer and a factory-modified TTY. No other options are required; however, the TC can interface with a PIM. This section describes the TTY interface in a general manner. The PIM interface and interface signal are also described. Refer to the manuals and reference material supplied with the TTY equipment for specific information.

2.4.2 Teletype Interface

The TC interfaces a model 33 or 35 TTY via the clock circuit card. The TTYs are modified at the factory prior to delivery to the customer. To modify the 33 ASR TTY:

a. Set the TTY for 20 mA operation. This includes the addition of a wire that enables the TTY to supply " battery" for the send and receive data loops to the clock card (the TTY is the current source for the TC relay drivers.

b. Set the TTY for full-duplex operation.

c. Disable the WRU contacts.

d. Disable parity on the keyboard.

e. Modify the answer-back drum.

f. Install the 180801 function lever.

The model 35 is similarly modified. Model 33 and 35 TTYs are electrically interfaced and cabled to the TC in almost the same manner, although they are physically quite different in appearance and in their internal operation.

The cable used for the TC/TTY interface for the 33 ASR runs from S connector plug P2 in the TTY to J13 at the rear of the CPU. The S connector is located at the right rear, top row, second connector from the right. The cable (drawing 53C0266) is normally 20 feet long with three leads in a cable.

The TTY end of the cable (P2) includes two other wires. Pins 7, 4, and 5 are connected. These connections tie internal TTY leads brought into the S connector plug as part of wiring. Note that both ends of the cable are keyed to ensure proper mating.

The cable between the model 35 TTY and the TC runs from J13 which connects to T1 at the rear of the CPU to a power terminal block in the TTY. This terminal block is located at the right lower rear of the cabinet behind the TTY printing mechanism.

Clock Card-Pin	J13 End	P2 End (-33)	TB End (-35)	Function
P3-36	1	9	Terminal 4	Return
P3-34	2	6	Terminal 5	Receive
P3-30	3	8	Terminal 7	Send

NOTE

The TTY cable is normally installed at the TTY by Varian Data Machines before customer delivery.

The model 33 TTY requires about 3 amperes of ac power.

The model 35 TTY requires about 6 amperes of ac power.

2.4.2.1 TTY DESIGN

The 33 ASR is primarily designed for light to medium use. Normally, it is the basic computer input/output device and is the most widely used unit. Its full-duplex operating mode allows simultaneous input and output.

The 35 ASR performs the same function as the 33 ASR, but it is designed for heavy, sustained use.

The 35 KSR is used for keyboard send/receive only and lacks the paper tape punch (PTP) and paper tape reader (PTR) capability of the ASR models. The operating characteristics are similar to model 33 keyboard operation. This unit is also designed for heavy, sustained use.

2.4.2.2 TTY INPUT METHODS

TTY input can be via the keyboard or the PTR. At the keyboard, the operator types at a random rate not greater than 10 characters per second (cps), the maximum rate for TTY input. Standard eight-level paper tapes are read by the PTR at a rate of 10 cps.

2.4.2.3 TTY OUTPUT METHODS

TTY output is either printed (typed) or punched on paper tape. For the printer or the PTP, the TC sends control codes or data at a random rate or at the maximum output rate of 10 cps. Data are printed, or control functions, such as line feed or carriage return, are performed on the printer. Similarly, control codes regulate the operation of the PTP, and data are punched into eight-level paper tape.

2.4.2.4 TTY SWITCHES

The ON/OFF switch controls the motor. The power supply and battery for TC relay drivers remain on, independent of this switch.

NOTE

> If the TTY motor switch is in the ON position when the computer power switch is off, an open circuit or run command will be transmitted to the TTY. In this case, the TTY motor switch should be in the OFF position.

The line switch controls the TC/TTY interface. In the ON-LINE position, the interface is complete, and the TTY is under CPU control. In the OFF-LINE position, the TTY is independent of the TC, and can be used for printing or preparing tapes.

The following switches control the tape and are not on the 35 KSR. The START/STOP/FREE switch on the PTR causes the tape to move in START, to stop in STOP, and to be released from the sprocket drive wheel in FREE. Pressing BSP on the PTP backspaces the tape one character. Pressing REL removes pressure from the tape. Pressing LOCK ON locks the punch on (prevents change of punch status). Pressing UNLOCK unlocks the punch and enables punch status change by the TC or from the keyboard.

The 35 ASR mode switch mechanism enables the following operating modes.

Position	Keyboard	Reader	Printer	Punch
K	On line	Disabled	On line	Off line
KT	On line	On line	On line	On line
T	Off line	On line	On line	Off line
TTS	Off line	On line	Disabled	Off line
TTR	Off line	Disabled	Disabled	On line

2.4.2.5 TTY FUNCTION CODES

The TTY receives control codes from the TC that cause it to perform specific functions. The codes are listed below. An enable code must follow a disable code. Codes R, T, Q, and S are not applicable to the 35 KSR.

Code	Bit Format	Function
Control A	10000001	Enable printer
Control D	10000011	Disable printer
Control R	10010010	Enable punch
Control T	10010100	Disable punch
Control Q	10010001	Enable reader
Control S	10010011	Disable reader

2.4.2.6 RELAY ISOLATION

Relays K1 and K2 in the TC perform the actual interface between the TC and the TTY. The relays are used to electrically and physically isolate the two units.

K1, the receiving relay, is driven by the TTY. K2, the sending relay, is driven by the TC. The relays switch approximately 20 milliamperes of current on or off the line. This method of interface is called " make-break" . Each relay can be said to drive or be driven by a current loop. When there is current flowing through a relay coil, the relay contacts and the current loop are closed. The line is then in the make condition (also referred to as the mark condition). When no current flows through the relay coil, the relay contacts and the current loop are open. The line is then in the break condition (also referred to as the space condition). The steady state of the loops is the mark condition when both the computer and TTY power is on, and both K1 and K2 relays are energized. When either the computer or TTY power is off, the steady state of the loops is in the break condition, and neither K1 nor K2 is energized.

SECTION 2
INSTALLATION

Except for the difference in switching control location, the send and receive loops have identical functions. The loops are shown in full-duplex configuration in figure 2-3. The factory-modified system is full-duplex to provide simultaneous transmission of data in both directions.

The current source for the two loops originates in the TTY and is sometimes referred to as " battery" . The CPU and TC use no loop source current, since they are isolated by the K1 and K2 relay contacts. Typical current in a factory-modified TTY interface loop is 20 mA.

This relay-controlled current-loop interface method enables the CPU-TC and the TTY to be placed far apart without noise interference, ground loops, etc., affecting the system. Normally, the TTY cable is 20 feet long.

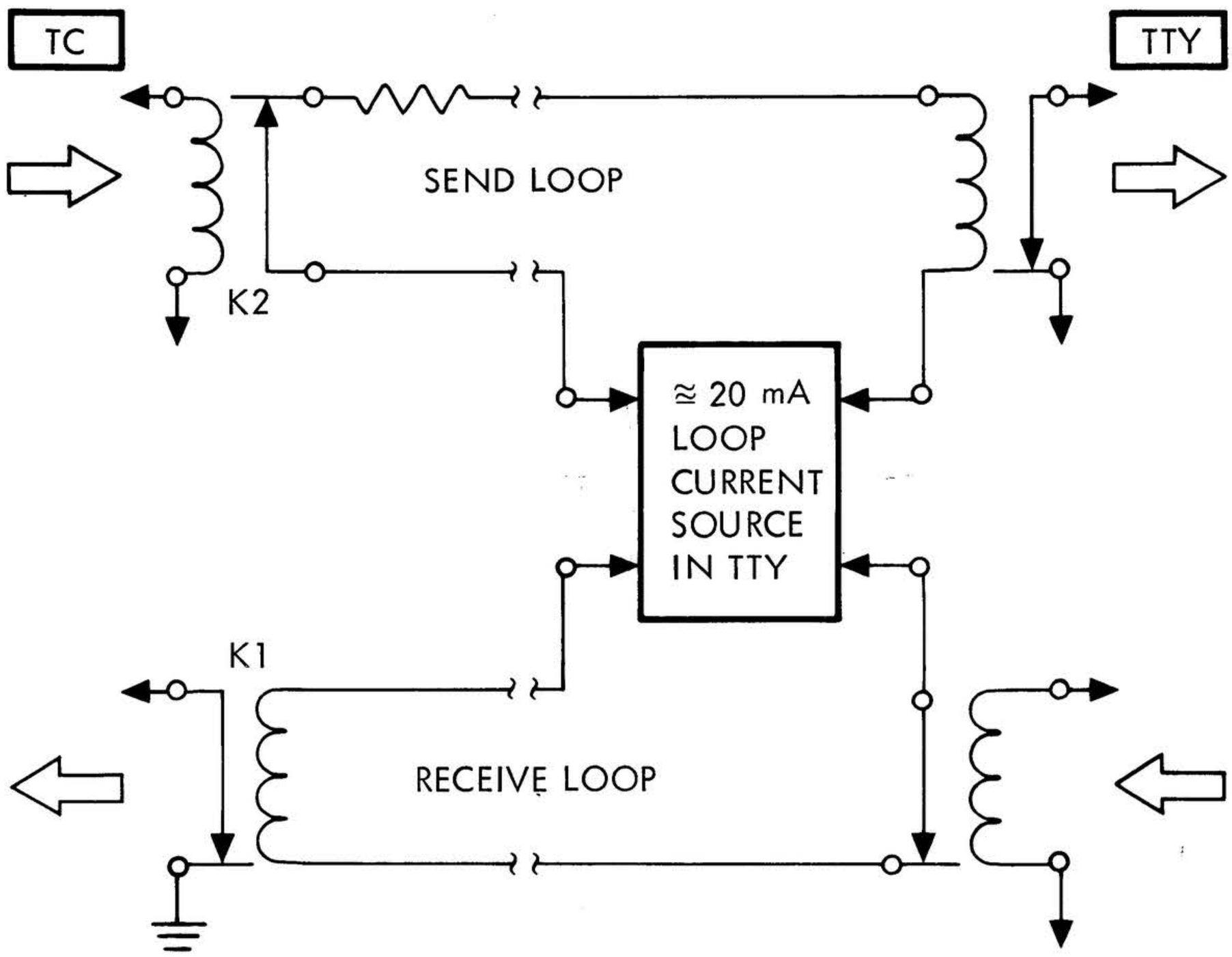
When either the TTY or the TC sends data, K1 or K2 operate (make or break) to conform to the character pattern being sent. The normal relay switching rate is 9.1 milliseconds per bit. Characters are sent or received serially by the current loop.

2.4.2.7 TTY CHARACTER BIT FORMAT

Each teletype character or command is serial and is divided into 11 periods or bits consisting of one start bit, eight data bits (the eight bit is always mark), and two stop bits (see figure 2-4).

The bit pattern for the character shown in figure 2-4 is 10101011. The bit length is 9.1 milliseconds and the bit rate is 110 bits per second (bps). The character length is 100 milliseconds, and the character rate is 10 cps. The start bit is always a space = zero bit = no current in loop = loop open. Data bits are either mark or space. A mark = one bit = current in loop = loop closed.

The eighth data bit is always mark. It might be used by the TTY as an even parity bit on an optional basis. The stop bits in the character bracket the data bits. This simplifies the design and operation of the TC receiving circuitry.



NOTE: Equivalent, not actual, circuit with two independent current loops for full-duplex operation. The current loops may have a single common current source and return wire. Isolation is achieved by relays.

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Figure 2-3. Relay Isolation for TC/TTY Interface

NOTE

The expression, the TTY is running open, means the send loop to the TTY lacks current = steady spacing condition. This occurs if relay K2 remains open, if the loop current source fails, or if the send loop opens at any point.

2.4.2.8 TTY INPUT CHARACTER

The receiving circuitry synchronizes at start-bit time. The TC receiving oscillator (4.55-millisecond clock) normally begins to run at the leading edge of the start bit. The bit pattern is sampled and shifted in the center of the start bit and continues at the center of each data bit through to the eighth data bit. Normally, each sampled bit is shifted into a register. When the last data bit has been sampled and shifted, the character is ready for transfer to permanent storage (e.g., the computer). The TC enables transfer to the CPU at the middle of the first stop bit. The stop bit period is used for the transfer of the character to the CPU; therefore, these bits are not sampled. Typically, the TC receiving oscillator stops after the data bits and the first stop bit are transferred and will not start again until a new start bit is received (figure 2-5).

To keep the receiving unit synchronized with the sending TTY, the receiving oscillator or

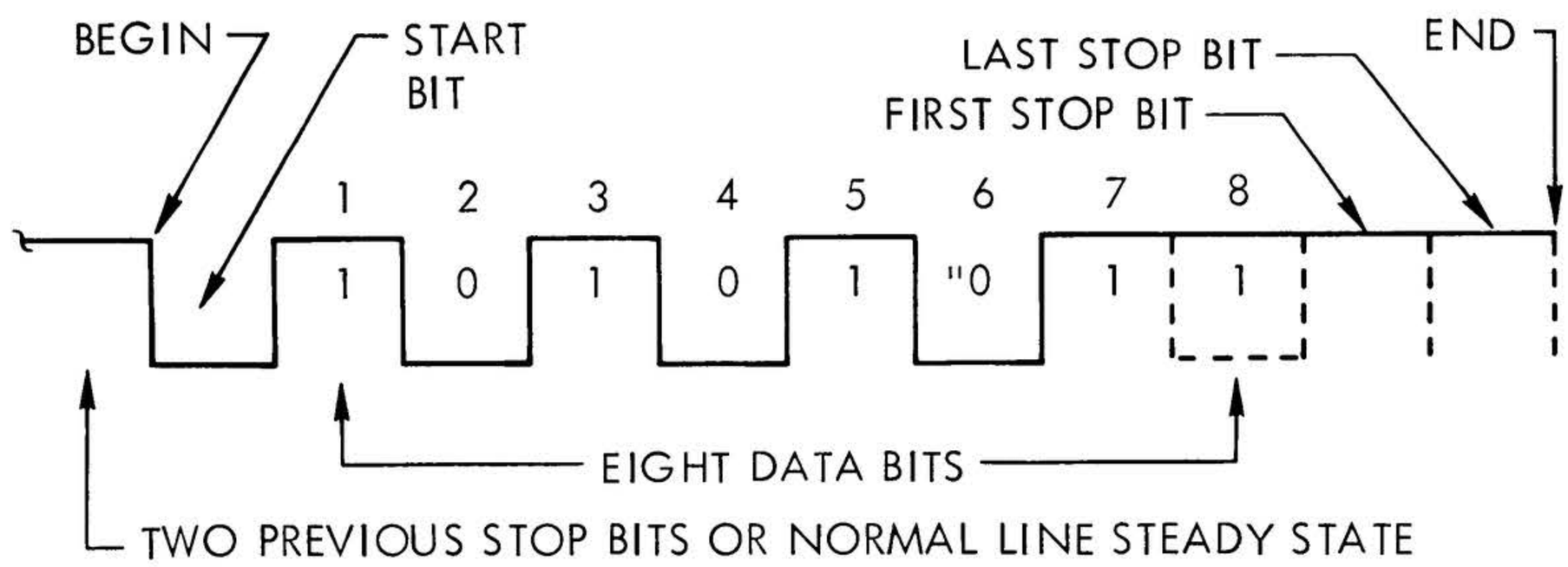

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Figure 2-4. Typical TTY Character

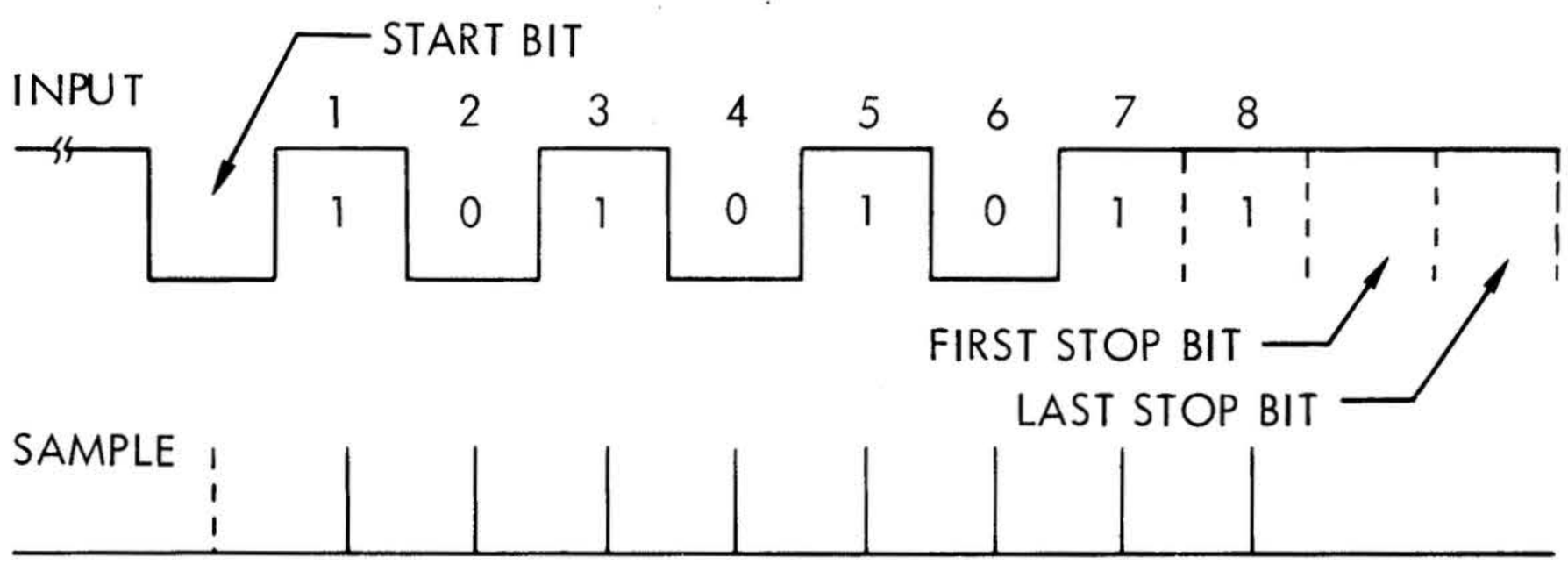

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Figure 2-5. Input Character Sampling

equivalent timing circuit must be allowed to stop and restart when the start bit for the next character occurs. If the sending device outputs a new start bit before the receiving oscillator has time to stop and recover, the two units are out of synchronization and erroneous data result. The next new character start bit may occur immediately after the stop bit or may not occur for an indefinite time interval. This is typical of asynchronous transmission. The receiving unit must be able to receive and synchronize to new data at any time.

2.4.2.9 TTY OUTPUT CHARACTER

The TTY is assumed ready to receive data at any time. The TC output sequence is as follows.

A character is loaded into the output register. A continuously running oscillator circuit is synchronized when ready to send a start bit. All bit times (start and data) are equal, and each bit takes one oscillator period. The oscillator and sync pulse initiate the start bit and enable the serial shifting of one character to the TTY. The last stage in the register drives the relay send circuitry (K2). The oscillator continues to run and shift out all eight data bits.

When the last data bit is sent, the TC obtains a new character from the CPU in preparation for the next character transmission. The oscillator in the TC continues to run during the stop bit. Typically, the TC obtains a new character during the last stop bit. If there are no more output characters, the TC oscillator continues running and places a steady one-bit level on the output line. The TTY can then await a new start bit which occurs on the next output character.

2.4.2.10 ASYNCHRONOUS TRANSMISSION

The previous subsections detailed basic TTY input and output. Several points should be stressed.

a. The sending unit transmits at a full or random rate at any time.

b. The receiving unit must be able to accept data at any time, at a full or random rate.

c. The receiving unit must resynchronize with each new start bit (every character) to maintain proper synchronization. The oscillator used for this purpose is called a start-stop or gated synchronizable oscillator.

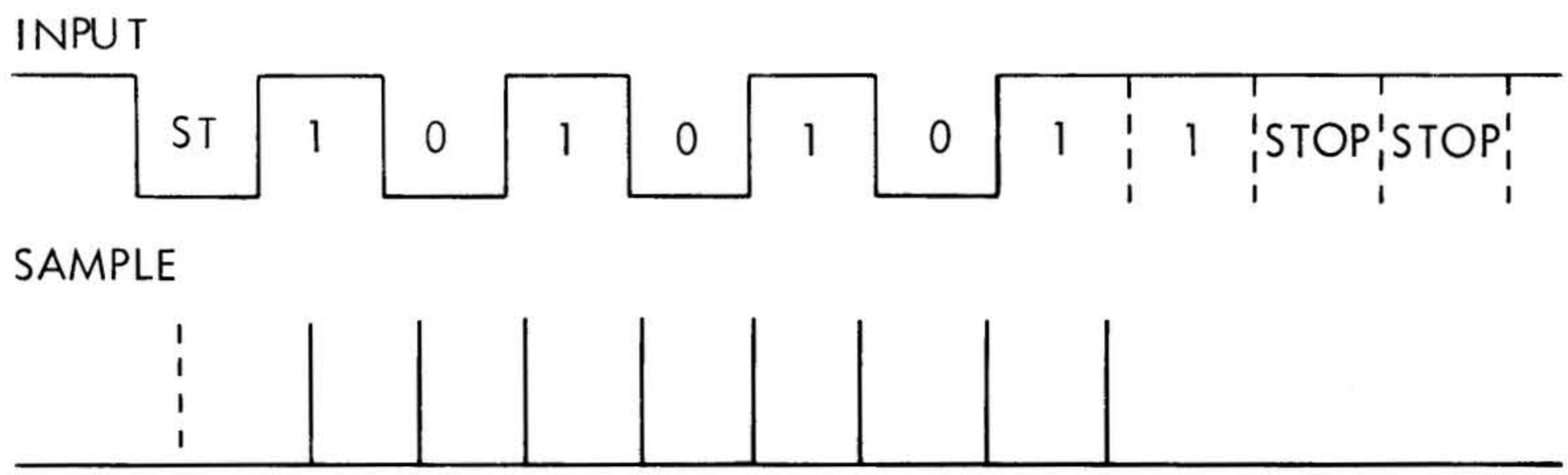

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Figure 2-6. Misadjusted Input Clock

d. The length of the output character must be carefully maintained. The receiving circuit can normally tolerate some distortion (less than 1/2 bit per total character). If the length of output characters is short or long and cannot be corrected, the receiving sampling circuitry can sometimes be adjusted to compensate. The waveforms of figure 2-6 illustrate an example of proper output character length but misadjusted input timing.

2.4.3 PIM Interface

The PIM drivers are wired from the TC to the PIM logic (DM124), which is either in the I/O backplane of the mainframe or in one of the expansion chassis. The computer must be equipped with the PIM in order to use these drivers.

2.4.4 Interface Signals

The TC interfaces with the computer and the TTY via the control and data lines listed in table 2-1. A circuit-card pin number follows each signal mnemonic. For definitions of the mnemonics, refer to section 4.

Table 2-1. TC Inputs and Outputs

Input Signals	Output Signals
AB00-C,P1-55	AB00-C,P1-55
AB01-C,P1-56	AB01-C,P1-56
AB02-C,P1-57	AB02-C,P1-57
AB03-C,P1-58	AB03-C,P1-58
AB04-C,P1-59	AB04-C,P1-59
AB05-C,P1-60	AB05-C,P1-60
AB06-C,P1-61	AB06-C,P1-61
AB07-C,P1-62	AB07-C,P1-62
AB08-C,P3-37	IUAA-I,P3-69
AB11-C,P3-14	IUBB-I,P3-70
AB13-C,P3-35	RDDX + ,P3-9
AB14-C,P3-36	SERX-C,P3-34
DRYX-C,P3-18	TTDO − ,P3-75
FRYX-C,P3-20	TTRX-I,P3-23
IUAX-C,P3-17	WCKP + ,P3-26
RCLP,P3-12	
SYRT-C,P3-38	

SECTION 3
OPERATION

There are no operating controls or indicators on the TC or clock circuit card. Data and control between the TC and TTY are under CPU software control.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

The theory of operation is described as a series of sequences that exercise the TC. Refer to section 6 for the TC logic diagram 91D0219 (DM274) and clock board circuit diagram 91C0209 (DM253). Three-digit numbers in parentheses indicate the chip location. The first number locates the sheet, the following letter and number indicate the chip location on the controller board. Circuit elements that are not on the DM274 card are followed by their circuit board number in parentheses.

Signal mnemonic levels referred to in the theory of operation are the levels of the signals at their point of origin or their entry into the TC. Stages of inversion are disregarded for the purpose of clarity. Signals resulting from the outputs of flip-flops are designated FF set and FF reset if they are high when the flip-flop is set or reset, respectively. J-K flip-flops (74H108) are negative-edge-triggered.

The write (transmit) and read (receive) shift registers each have two 7495 medium scale integrated circuit chips. During a write (DTOX+) operation, the W register is parallel-loaded because the mode control is high (+5V dc). During a read (RRCX-) operation, the R register is cleared by parallel-loading of high (+5V dc) and serial-loaded with mode control low (gnd). The write register is never cleared. Data are transferred to the output pins when the clocks (pins 8 and 9) go from high to low and the data are present at the inputs prior to clocking.

Figure 4-1 presents a functional block diagram of the TTY for reference when studying the descriptions of TTY theory in the following subsections.

4.2 INITIAL CONDITION

When computer power is first turned on, the TC and the CPU circuitry can be in an undefined state. Pressing the RESET switch on the control panel initializes the TC (and the computer) to properly perform various functions under program control. Basically, this enables the TC to monitor the TTY for input characters and to accept output characters from the CPU to the TTY. When initialized, the TC also transmits a steady mark to the TTY by keeping relay K2 (DM253) energized. The TC can also be initialized under program control; the command, however, must not be issued while the TC is communicating with the TTY.

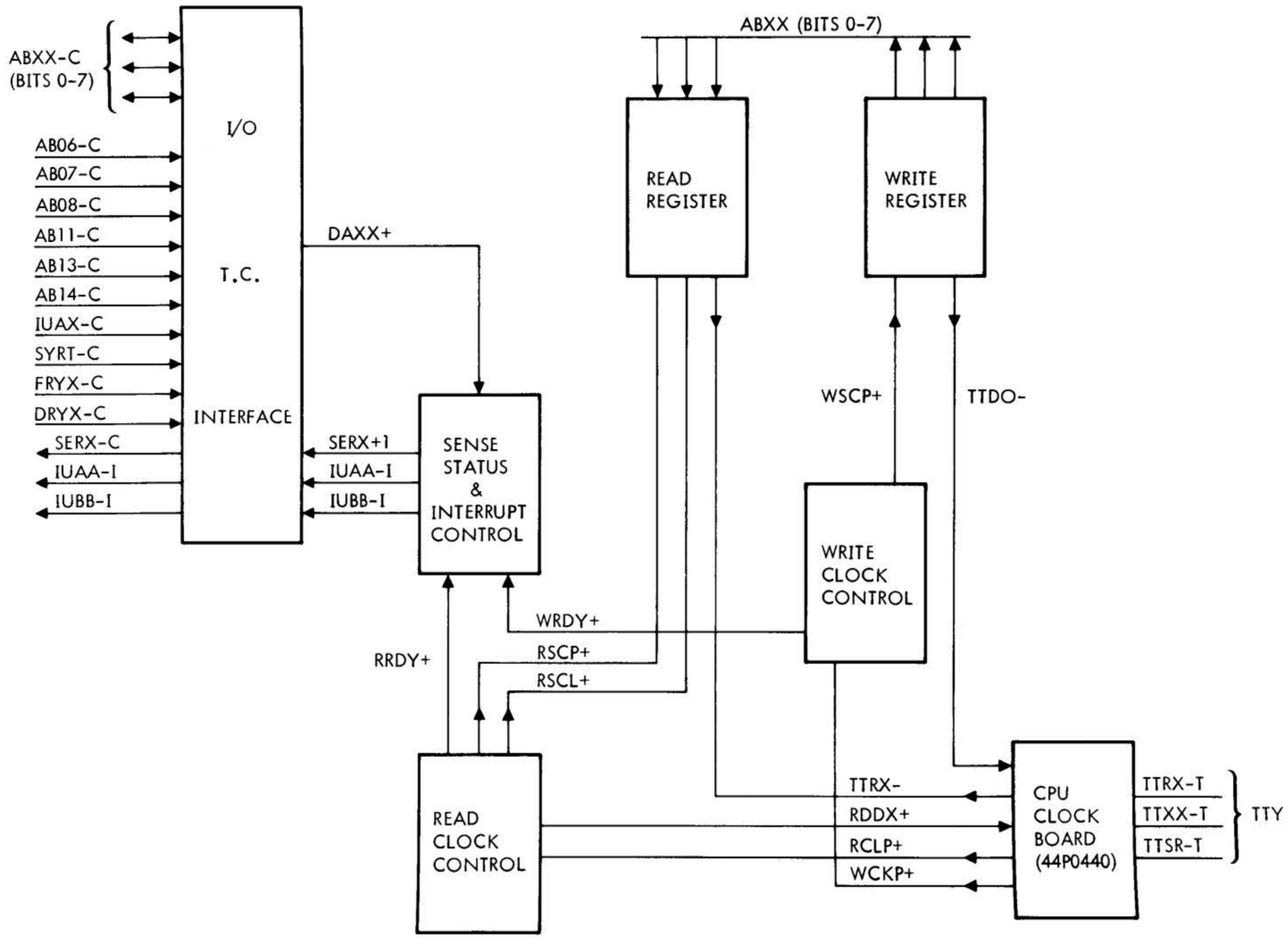

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Figure 4-1. TTY Functional Block Diagram

NOTE

An initialization command performs the same function as pressing the RESET switch.

Either SYRT-C low or TY08 + and EXCX + high, which produces WIRE01 low, generates INZX + high (1M4). INZX + high and INZX- low verify that the following flip-flops are initialized to the state shown.

Set	Reset
WRDY	RRDY
W00X	RDDX
WSYNC	DTOX
	DTIX
	RRCX
	R09X
	RSCX
	WSEX

As a result, the 4.55-millisecond clock is off.

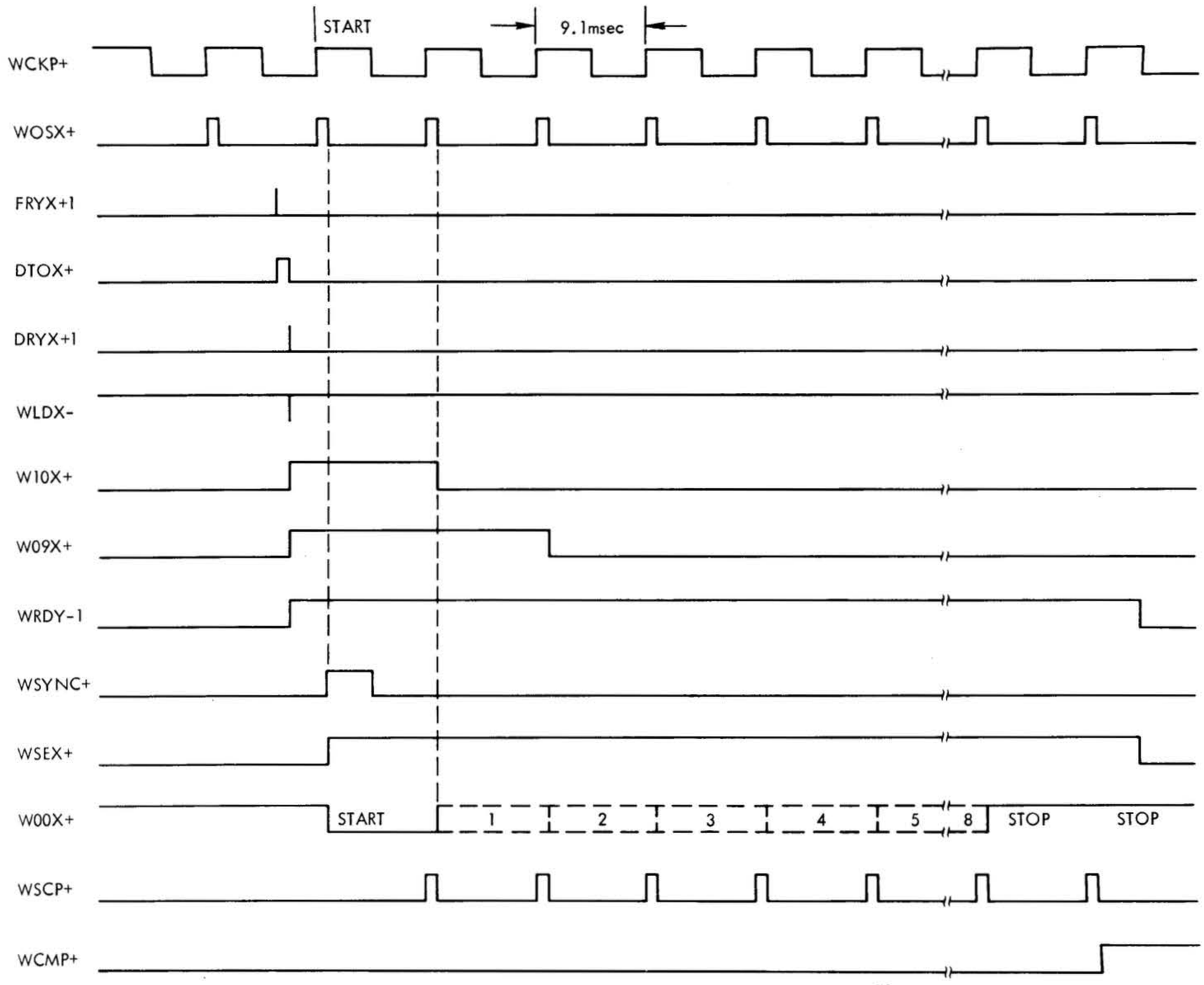
Note that with the exception of flip-flop W00X, the R and W registers are not cleared initially. If TTY power is on, the TTY energizes relays K1 and K2 (DM253), and the TC receives a steady mark. The TC is then in a line-monitoring state.

4.3 TC/CPU INTERFACE

The CPU commands the TC via the A bus with signals such as FRYX-C and DRYX-C. When any such command is issued, the following device address sequence occurs.

DAXX + is high if the proper address (01) is put on the A bus and IUAX-C is high (no interrupt). DAXX + high enables the command generation gates.

The functions of the A bus signals are: AB00-C through AB05-C enable device address signal DAxx + (1N4). AB06-C enables the output ready sense response. AB07-C enables the input ready sense response. AB08-C and AB11-C enable the initializing sequence. AB13-C enables the input command sequence. AB14-C enables the output command sequence (figure 4-2).



VT11-1065

Figure 4-2. External Control Timing

IUAX-C inhibits TC selection when the CPU has an interrupt, direct memory access (DMA), trap-in, or trap-out. The CPU can issue any of several commands. All of the following commands are accompanied by the device address, and some are also accompanied by FRYX-C and DRYX-C. The input and output timing diagrams (sections 4.4.1 and 4.6.2) illustrate the sequence that results with FRYX-C and DRYX-C.

a. Sense write ready (AB06-C) -- FRYX only

b. Sense read ready (AB07-C) -- FRYX only

c. Execute (initialize) (AB08-C and AB11-C) -- FRYX only

d. Output (load/write register) (AB14-C) -- FRYX and DRYX

e. Input (read/read register) (AB13-C) -- FRYX and DRYX

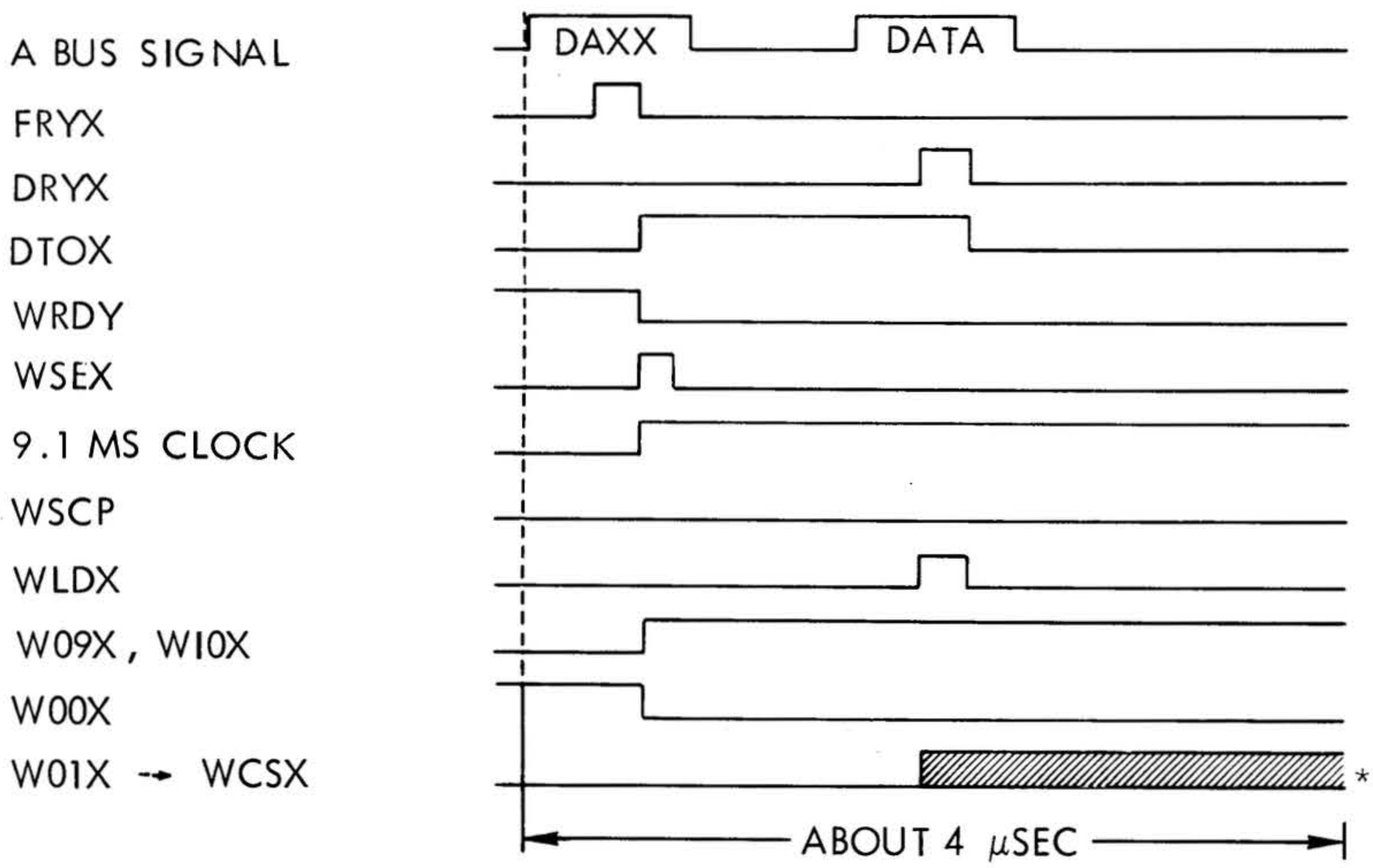
If a sense condition is met, SERX-C goes low. A sense command is normally issued before input or output. SERX-C low is enabled by FF set signal RRDY + high (3U5) or FF set signal WRDY + high (2S4). These two signals signify that the TC has an input character or is in a condition to accept an output character, respectively.

When initialized, flip-flop WRDY + is set to enable immediate output under CPU control. Flip-flop RRDY + is not set until the TTY has loaded a complete character into the R register.

When the CPU issues an output command, a FRYX/DRYX sequence sets and resets flip-flop DTOX +. When the CPU issues an input command, a FRYX/DRYX sequence sets and resets flip-flop DTIX +.

4.4 TC OUTPUT (WRITE)

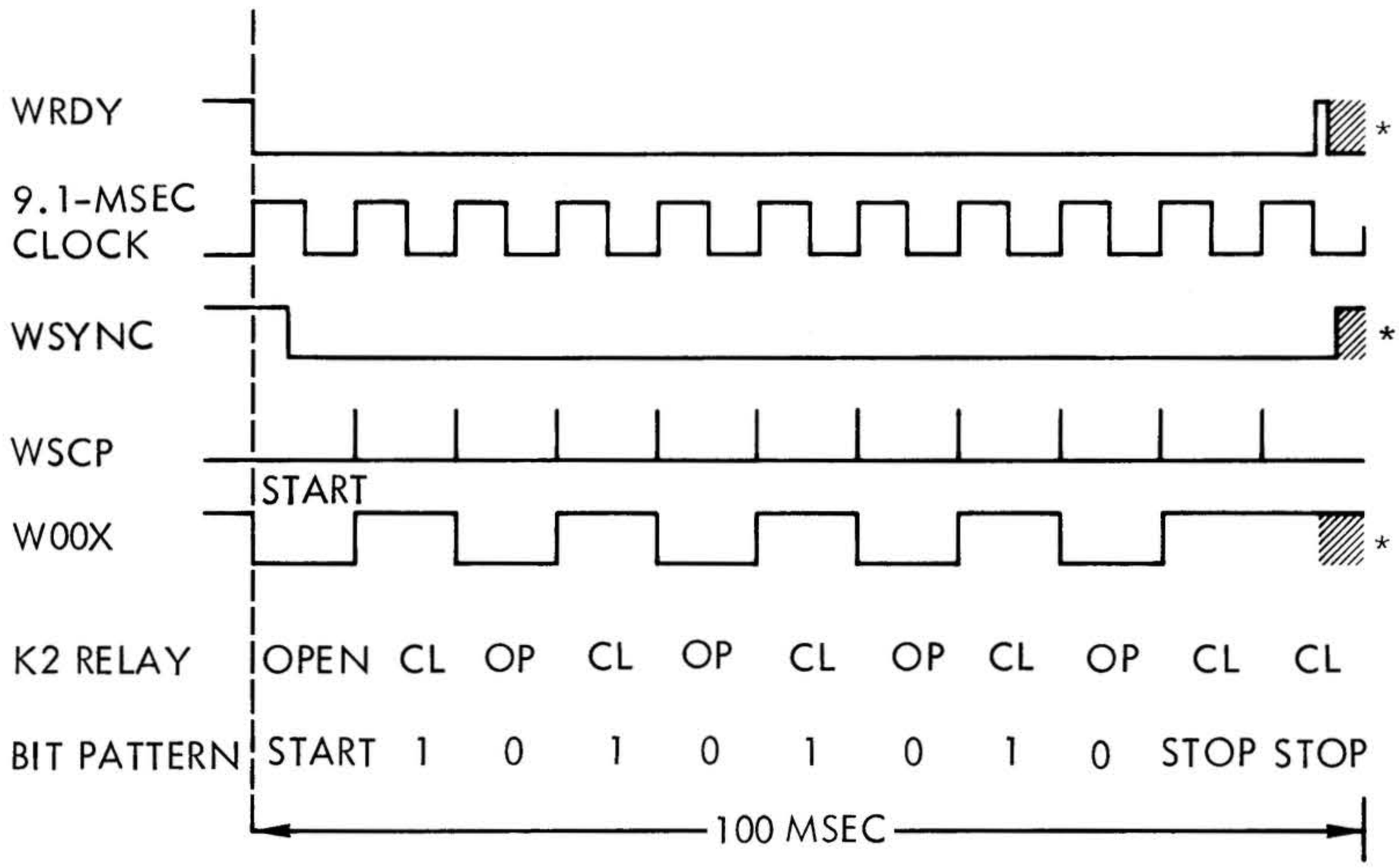
The TC output circuits include portions of the TC/CPU interface, output timing control, output register, and portions of the TC/TTY interface. Circuit elements are control flip-flops, a group of gates enabled by the A bus, a 110-Hz free-running clock that is asynchronous to the CPU, an 11-bit write register, and an output relay to the TTY with associated drive circuitry. The data and control output waveforms illustrate the loading of output from the CPU to the TTY (figures 4-3 and 4-4). For these waveforms, assume that the TC has been initialized; the CPU has sensed write ready and issued an output command; and the output character is 01010101.



*The W register (W01X-W08X) accepts the A bus bit pattern at WLDX time.

VT11-0999

Figure 4-3. Output from the CPU to the TC Timing



*WRDY enables sense response logic. The computer can then respond at any time. The output sequence restarts as above, except actual line output of new character does not begin until the 9.1-msec clock recovers. WSYNC keeps relay K2 energized after W00X is reset and until the 9.1-msec clock restarts.

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Figure 4-4. Data Transfer Out Timing

Data are output from the CPU in a two-word format; the first word contains the device address and the function type, and the second word, character data. The device address is sampled on the trailing edge of FRYX-C, and data are sampled on the trailing edge of DRYX-C.

4.4.1 Load Output Register

DAxx + and FRYX + 1 clock the DTOX + flip-flop true if JDTOX + is high. DTOX + is reset on the trailing edge of DRYX-C. The clocking signal (FDRY +) for both DTIX + and DTOX + implements:

$$FDRY+ = (DRYX+1)(DTIO+) + (DAxx+)(FRYX+1)$$

In addition, FDRY + clocks eight bits of data into the parallel in-serial out shift register (4S3,T3) if DTOX + is high. FDRY + is ANDed with DTOX + (2S5) to clear the WRDY + flip-flop (2S4) and preset bits W10X + and W09X + of the write shift register (4T2). Note that W10X + and W09X + are the two stop bits for the TTY character, and bit W00X + is the start bit. The clearing of the WRDY + flip-flop enables the set input of the write sync (WSYNC) flip-flop, which results in a sync pulse on the next WOSX- clock (2U3).

The basic write clock (WCKP +) is input to the WOSX + one-shot (2U3) to generate an 80-nanosecond pulse for clocking the write data register. On the first positive-going edge of WCKP + (after the WRDY + flip-flop is set), WSYNC (2X4) is set. The WOSX pulse that clocks WSYNC + high does not clock the data register, but is inhibited by WSEX + (2S4). The WSYNC + flip-flop resets when WCKP + goes low. WSYNC + true presets the WSEX + flip-flop and clears W00X + to start the character transfer.

4.4.2 Output to TTY

With the WSEX + flip-flop set, subsequent WOSX + pulses clock the write register. This continues until W00X + is high and W01X + through W08X + are low, at which time the set input of the write ready flip-flop goes high. The falling edge of WCKP + sets the WRDY flip-flop, which clears the WSEX flip-flop and disables further WSCP + pulses. For continuous TTY transmission, the CPU must output another character within 4.53 milliseconds after the WRDY + flip-flop goes high.

NOTE

WRDY+ becomes true at T = 95.45 milliseconds (of the 100-millisecond character), which gives the CPU 4.53 milliseconds to load a new output character and maintain a full rate.

4.5 CPU RESPONSE

If the CPU responds within 4.55 milliseconds, the load/write register sequence occurs. The 9.1-millisecond clock does not restart until the previous 100-millisecond character period has elapsed; hence, flip-flop WSEX+ stays set and the TC keeps relay R2 energized, forcing the end of the last stop bit. When the 9.1-millisecond clock recovers, flip-flop WSEX+ resets, and the output proceeds as for the previous character.

If the CPU responds after 4.55 milliseconds, the load/write register sequence occurs exactly as described in the preceding paragraphs because the 9.1-millisecond clock has recovered. Flip-flop W00X is set, keeping a mark on the line to the TTY through relay K2. The CPU may not respond at all; in which case, the above condition continues until the CPU responds. In any case, the TTY remains ready to accept a new (start bit) character (figure 4-5).

4.6 TC INPUT (READ)

The TC input circuits include portions of the TC/TTY interface, input timing control, input register, and portions of the TC/CPU interface. Circuit elements are control flip-flops, a group of gates to enable the A bus, a 4.55-millisecond oscillator, a 10-bit read register, and an input relay from the TTY. The data and control input waveforms illustrate the loading of input from the TTY to the CPU (figures 4-6, 4-7, and 4-8). For these waveforms, assume that the TC has been initialized; the TTY has just begun to transmit a character; and relay K1 is beginning to deenergize. During the start bit, the input is controlled by the following sequence (figure 4-6).

The read portion of the TC is supplied a 50-percent duty cycle clock of 220 Hz (RCLP+). RCLP+ goes to the RSCL+1 one-shot to form an 80-nanosecond clock pulse.

Character reading is initiated by TTRX+ going low, which produces a high set output of the RDDX+ flip-flop. RDDX+ high releases the RRCX- and RSCX+ flip-flops for clocking and the RCLP+ for cycling. When RDDX+ is released, RCLP+ goes high and fires the FSCL+1 one-shot (3V3). The read ready clock enable flip-flop (RSCX+) reset inhibits the first RSCL+ pulse, generating RSCP+. However, RRCP- is generated because RRCX-

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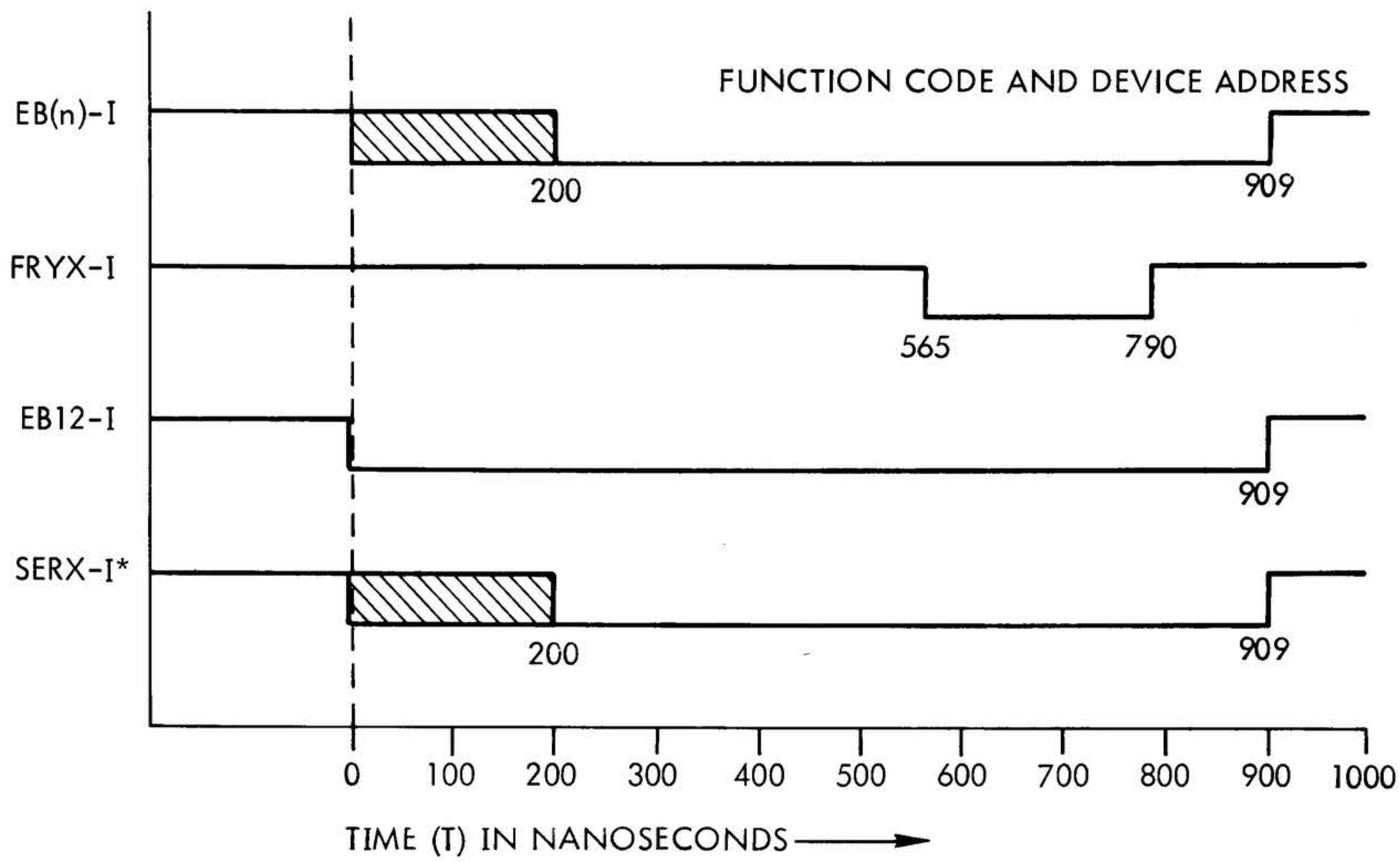

T = 0 is the start of the execute phase of the sense instruction.

Logic levels: true = 0V dc,
false = +3V dc.

▨ = time when signal is settling.

* SERX-I is normally on at T = 200; it must be on by T = 340.

VT11-0402A

Figure 4-5. Sense Response Timing

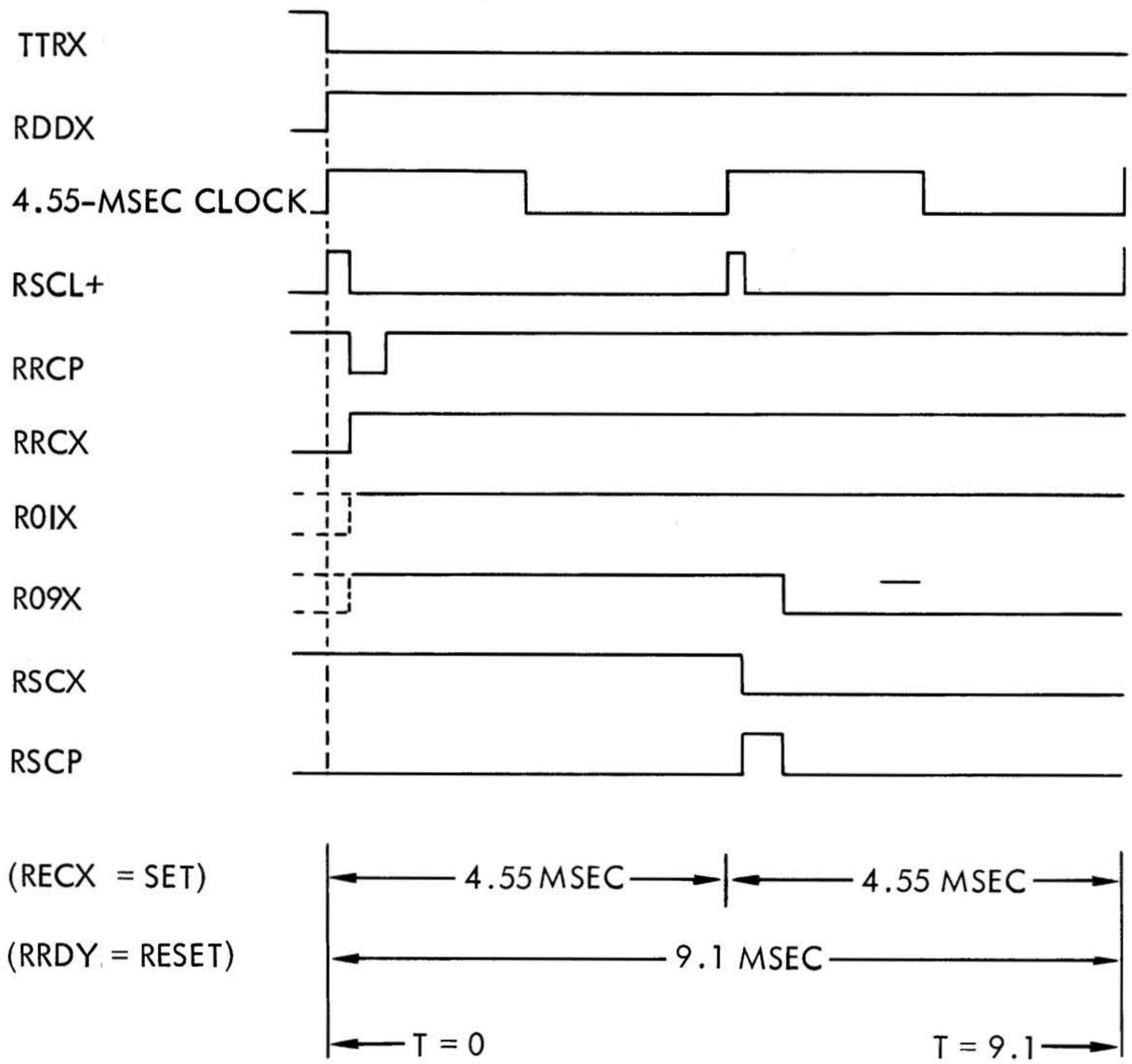

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Figure 4-6. Input Start Bit Timing

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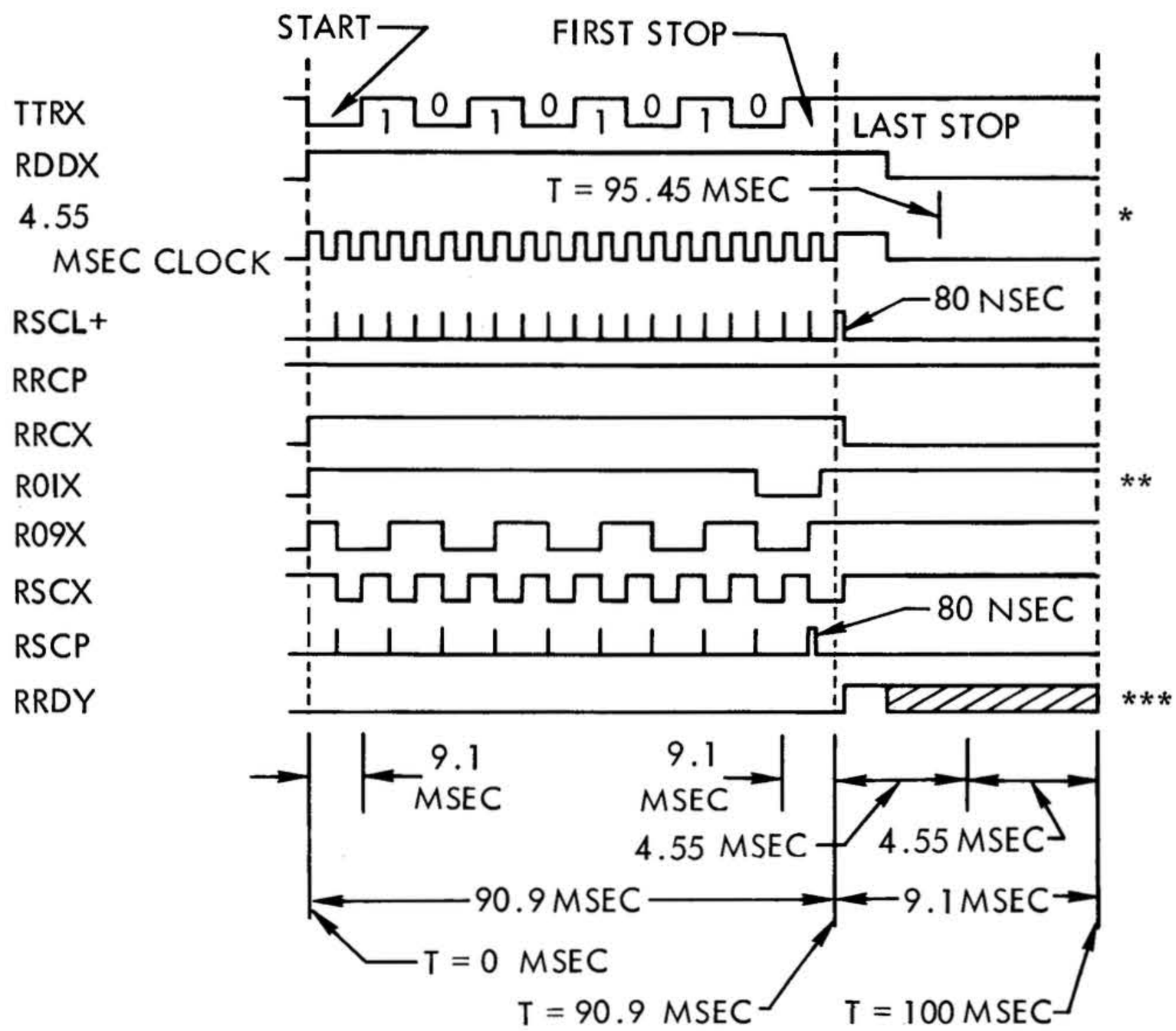

*The 4.55 msec clock may be restarted and synchronization established any time after T = 95.45 msec.

**R01X is set if lsb is a one bit, reset if lsb is a zero bit.

***RRDY is set (enabling sense response) until the CPU issues an input command. The CPU must respond before a new start bit is transferred through the TC or the input character is lost.

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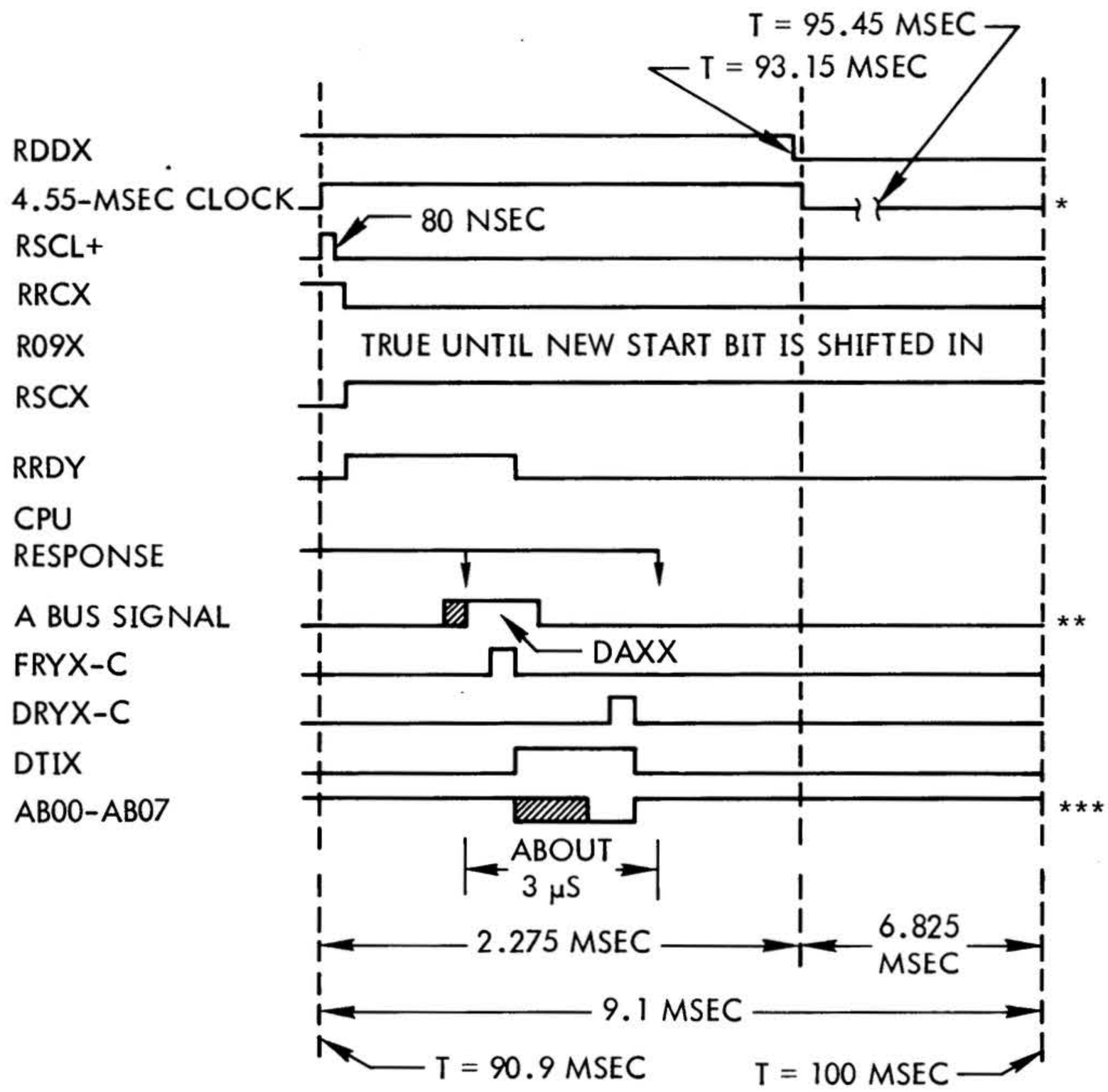
Figure 4-7. Input from the TTY to the TC Timing



*New start bit can occur any time after T = 95.45 msec, and synchronization with the TTY is maintained. Data transfer to the CPU must occur before a new start bit or the character in the receive register is lost. If a new start bit occurs before T = 95.45 msec, clock synchronization with the TTY will be lost.

**A bus signals are for device address (normally device 01).

***The AB00-AB07 lines are enabled directly from the CPU.

VT11-1003

Figure 4-8. Data Transfer In Timing

(3U4) is reset. Note that RRCP- (3S5) presets the first flip-flop of the read register (R09X+) (4T4) and parallel-loads ones into the other eight bits to clear the register.

In addition, the first RSCL+ pulse toggles both RRCX- and RSCX+ (3U4), so that on subsequent RSCL+ pulses the RRCP- clear pulse is inhibited and RSCP+ is enabled on alternate pulses. This occurs during the clocking of data into the read register and while RSCX+ is toggling to select the RSCL+ pulse occurring in the center of the 9.1-millisecond bit period. Clocking continues until the zero start bit is clocked into R01X+. The K input of RDDX+ goes high and the J input of the read ready flip-flop becomes true. On the next RSCP+ clock, RRDY+ goes high (3U5) and RRDX+ resets, again disabling the oscillator output (RCLP+). RDDX+ reset clears the RRCX- and RSCX+ flip-flops to prevent further register clocking.

4.6.1 Load Input Register

At the end of the start bit sequence, the TTY transmits the first data bit. The TC has shifted the start bit into flip-flop R09X and is ready to receive the eight data bits. At the end of the second 4.55-millisecond clock, RSCL+ resets flip-flop RSCX+, enabling RSCP+. RSCP+ shifts the first data bit into flip-flop R09X+ and the start bit into R08X of the shift register.

This two-clock-period sequence is repeated for each data bit. Flip-flop RSCX+ is triggered every 4.55 milliseconds, enabling RSCP+ in the center of each bit so that sampling and shifting can occur.

When the eighth data bit is accepted, an end-of-character sequence begins in the center of the bit. When the last data bit is shifted into flip-flop R09X+, the start bit resets shift register bit R01X. Two clock periods later, in the center of the first stop bit, RSCP+ resets flip-flop RDDX+. This pulse also shifts the start bit out of the shift register and shifts the first stop bit into flip-flop R09X+. At this time, the character is completely in the R register, the TC is preparing to enable character transfer to the CPU, and the TTY is transmitting the second half of the first stop bit.

At the end of the clock period in which the first stop bit ends (T = 90.9 milliseconds), the signal at pin 8 of W3 and FF set signal RDDX+ low reset flip-flop RRCX+. Shift register output (R01X-) partially enables the resetting of flip-flop RDDX+. which stops the 4.55-millisecond clock. Before RRDX+ is reset, R01X- high sets flip-flop RRDY+. This enables a read/read sense response to the CPU. The clock continues to run for one more period. Halfway through this period, RRDX+ resets, removing the clock start enable.

NOTE

The 4.55-millisecond clock does not recover until T = 95.45 milliseconds. Prior to this time it cannot be accurately restarted with a new start bit from the TTY. If a new start bit from the TTY occurs earlier, the resulting out-of-sync condition causes erroneous data sampling and errors.

At the end of the first stop bit (T = 90.9 milliseconds), flip-flop RRDY + sets to enable a sense-ready-to-read response in the CPU (figure 4-5). The waveforms shown in figure 4-5 occur after the sequence in figure 4-4. With these waveforms, assume that data bits of the character have been shifted into the R register, the TC is receiving the last stop bit, and the CPU issues an input command. The time from T = 90.9 milliseconds to T = 93.175 milliseconds is shown extended for clarity.

NOTE

At a continuous rate of 10 cps (100 milliseconds per character), the CPU has less than 9.1 milliseconds to read the character out of the R register. If an input data command is not issued before 9.1 milliseconds, the character is lost. The start bit of the next character resets flip-flop RRDY +, preparing the R register for a new character.

The CPU issues an input data command after sensing the read-ready condition (IUBB-I). With DAxx + high at the end of FRYX-C, flip-flop DTIX sets, and flip-flop RRDY + resets. DTIX + high enables the A bus gates driven by the R register. The character is on the A bus lines to the CPU when DRYX-C occurs. When DRYX-C goes low, flip-flop DTIX + resets, and input to the CPU is complete.

Character transfer to the CPU must occur before the start bit of a new character to avoid losing the character. The TC waits for a new start bit. Until a new start bit occurs, relay K1 remains energized, and the 4.55-millisecond clock and flip-flop RDDX remain off.

4.7 MNEMONICS

The mnemonics used in the TC are listed alphabetically in table 4-1. A brief description of each signal's function and proper signal name is given under the description column. Except where noted, the source column lists the sheet numbers of the TC logic diagram 91D0219.

Table 4-1. Mnemonic Definitions

Mnemonic	Source	Description
AB00-C to AB05-C	1.0	A bus bits for device address select.
AB06-08, 11, 13, 14	1.0	Function, sense, and reset commands between the CPU and the TC.
CLRRDY	3.0	Clear read ready flip-flop.
DAXX	1.0	Device address decodes the device address from A bus bits.
DRYX + 1	1.0	Inverted from DRYX-C.
DRYX-C	1.0	Data ready pulse from CPU that gates data in and out of the TC.
DSYNC	2.0	Set input to WSYNC flip-flop.
DTIO	1.0	Data transfer in or out signal to reset DTIX or DTOX flip-flops and enable FDRY.
DTIX	1.0	Data transfer in flip-flop stores the occurrence of an input command from the CPU; gates receive data onto A bus.

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
DTOX	1.0	Data transfer out flip-flop stores the occurrence of an output command from the CPU. Puts write (send) register in parallel load mode.
ESERX1	1.0	ANDed output to enable sense response for write ready data.
ESERX2	1.0	ANDed output to enable sense response for read ready data.
EXCX	1.0	Enables initialization signal.
FDRY	1.0	Clocks the DTIX and DTOX flip-flops.
FRDX	1.0	ANDed output of DAXX+ and FRYX+1.
FRYX+1	1.0	Inverted from FRYX-C.
FRYX-C	1.0	Function ready pulse from the CPU that enables data transfer to or from the TC.
H10, H11	All sheets	+5V dc from resistor chip R3- pins 5,6.
INZX	1.0	Initialization control flip-flops.
IUAA-I	2.0	Interrupt line to signify the output register is ready for data from the CPU.
IUAX-C	2.0	Interrupt acknowledge enables device address; enables use of TC.
IUBB-I	3.0	Interrupt line to signify the input register has data for the CPU.

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
JDTIX	1.0	Set input to DTIX flip-flop.
JDTOX	1.0	Set input to DTOX flip-flop.
RCLP	91C0209 (5.0)	Output clock pulse from TTY read clock.
RDDX	3.0	Read detect flip-flop stores the start of a teletype transmittal; enables input timing.
RRCP	3.0	Read register control pulse sets R register flip-flops prior to input.
RRCX	3.0	Read register control flip-flop stores the activation of the R register.
RRDY	3.0	Read ready flip-flop stores the loaded condition of the R register.
RSCL	3.0	80-nanosecond clock pulse.
RSCP	3.0	Read shift clock pulse controls shifting of input character bits into R register.
RSCX	3.0	Read shift clock flip-flop stores end of each 4.55-millisecond clock period; generates read shift clock pulses.
R01X through R08X	4.0	R register flip-flop stores input data or control bit.

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
R09X	4.0	First serial input bit to read register.
SERX + 1	1.0	ORed output of ESERX1 and ESERX2.
SERX-C	1.0	Sense response indicates TC is ready to respond to CPU input or output command.
SRRDY	3.0	Set input to the RRDY flip-flop.
SYRT-C	1.0	System reset generates initialize signal when the SYSTEM RESET switch is pressed.
TTDO	91C0209 (5.0)	Energize and deenergize K2 during data transmission to TTY.
TTRX-I	91C0209 (5.0)	Receive output from teletype via E1 of TTY interface, to TC.
TTRX-T	91C0209 (5.0)	Energize and deenergize K1 during data reception from TTY.
TTSR-T	91C0209 (5.0)	Teletype return for teletype input and output.
TTXX-T	91C0209 (5.0)	Transmit input to teletype via K2 of TTY interface, from TC.
TY00 through TY07	1.0	Transmit data input inverted from A bus to parallel load W register.
TY08, TY11, TY13, TY14	1.0	Sense, command, and initialize signals.
WCKP	91C0209 (5.0)	Output clock pulse from TTY write clock.

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
WCMP	1.0	WRDY flip-flop set enable when TC is ready to accept the next character.
WIRE01	1.0	ORed with SYRT-C for the initialized condition.
WIRE02	1.0	ORed with FRDX for clocking the flip-flops DTIX and DTOX.
WLDX	4.0	Write load gates A bus contents into W register.
WOCXA, B, C	2.0	Decode of output character to determine acceptance of next character.
WOSX	2.0	Set output of 9.1-millisecond flip-flop.
WRCP	2.0	Write ready clock pulse for flip-flop WRDY.
WRDY	2.0	Write ready flip-flop stores the readiness of the TC to accept an output character; enables output timing.
WRDY-1	2.0	Reset output of flip-flop WRDY for setting flip-flop WSYNC and presetting flip-flop WSEX.
WSCP	2.0	Write shift clock pulse controls shifting of output character into W register.
WSEX	2.0	Write shift flip-flop stores the start of a load W register sequence.
WSYNC	2.0	Set output of the flip-flop that syncs the TTY write clock with the 9.1-millisecond flip-flop.

Table 4-1. Mnemonic Definitions *(continued)*

Mnemonic	Source	Description
W00X	4.0	Output control flip-flop for W register.
W01X through W08X	4.0	W register flip-flop stores output data or control bit.
W09X, W10X	4.0	Input control flip-flops for W register.

4.8 PROGRAMMING CONSIDERATIONS

The user writes the programs that use the TC. The TC can be programmed directly under CPU control (with or without interrupts).

The additional 620/i-type TCs operate with the BIC, freeing the CPU to use the I/O bus for other operations. Refer to the 620/i TTY controller manual (document number 98 A 9902 161) when programming these TCs.

The TC can supply interrupts (write ready and read ready) to the PIM when this option is included in the computer system, saving computing time and simplifying software since programmed delay and sense loops can be avoided. With this feature, the program running in the CPU is interrupted at the proper time.

The software initializes the TC (as does pressing the RESET switch on the control panel). The TC is then ready to accept output from the CPU and is also capable of accepting an input character from the TTY. The software normally issues a sense command and, if a sense-ready condition exists, follows it with a read (input) or load (output) command to enable the data transfer of one character between the TC and the CPU.

Except for interrupts, the TC operates within the following general timing restrictions.

Output Maximum data transfer rate is 10 characters per second (cps). There is no minimum rate. The CPU can output a single character, discontinue output for an indefinite period of time (longer than 100 milliseconds), and then output another character without loss of data or synchronization.

Input Maximum data transfer rate is 10 cps (100 milliseconds per character). The CPU must read the input character transferred from the TTY by the TC during the last (second) 9.1-millisecond stop-bit period. If the CPU fails to read the character input during this time and before the TTY inputs again, the character is lost.

4.9 DESCRIPTION OF COMMANDS

The TC and the TTY respond to the commands listed in table 4-2. Appendix A lists the American Standard Code for Information Interchange (ASCII) and the corresponding TTY symbols.

The initialize command performs the same function as the RESET switch on the computer console. The TC is prepared to accept CPU output and to monitor TTY input. This command should not be issued while the TC is communicating with the TTY.

The sense commands are the sense ready to read and the sense ready to write commands, which enable the CPU to determine TC status. If the sense condition is met, a data transfer can proceed. If the sense condition is not met, the CPU must wait to perform data transfer. A sense command can be issued at any time and normally precedes any data transfer command.

The data transfer commands are the read (input) and load (output) commands, which transfer data between the CPU and the TC through the read and write registers. Issuing a read or load command at the wrong time results in incorrect data transfer.

Table 4-2. TC and TTY Commands

Mnemonic	Octal Code	Functional Description
External Control		
EXC 0401	100401	Initialize
Transfer		
OAR 01	103101	Transfer the A register to the W register
OBR 01	103201	Transfer the B register to the W register
OME 01	103001	Transfer the memory address to the W register
INA 01	102101	Transfer the R register to the A register
INB 01	102201	Transfer the R register to the B register
IME 01	102001	Transfer the R register to the memory register
CIA 01	102501	Transfer the R register to the cleared A register
CIB 01	102601	Transfer the R register to the cleared B register
Sense		
SEN 0101	101101	W register ready
SEN 0201	101201	R register ready

Table 4-2. TC and TTY Commands *(continued)*

Mnemonic	Octal Code	Functional Description

TTY Command Codes

Function	Symbol	Code	Typed As
Print Enable	SOM	201	Control and A
Print Suppress	EOT	204	Control and D
Reader On	XON	221	Control and Q
Punch On	TAPE	222	Control and R
Reader Off	XOFF	223	Control and S
Punch Off	TAPE OFF	224	Control and T

SECTION 5
MAINTENANCE

5.1 GENERAL

TC maintenance consists of running test programs, troubleshooting, and making repairs if required. The test executive program (part number 92A0107-001) and TTY test program (part number 92A0107-004), described in the 620 test program manual (document number 98 A 9908 960), in conjunction with the 620/f maintenance manual, help isolate an error condition. Troubleshooting is facilitated by familiarization with the operation of the TC and use of the logic diagram. This section provides troubleshooting data, program tests, and a list of reference documents to be used as maintenance aids.

5.2 EQUIPMENT

The following is a list of recommended test equipment and tools for maintaining the TC.

a. Oscilloscope, Tektronix type 547

b. Multimeter, Triplett type 630

c. DM265 Extender Card, part number 44P0437

5.3 TEST PROGRAMS

The condition of the TTY unit should be periodically checked using program tests. These tests for TC and TTY are provided as part of the regular troubleshooting package for the 620/f computer.

NOTE

One section of the TTY test program for ASR models includes a print suppression test. The 33 ASR does not perform this function, so this test program should be bypassed when testing the 33 ASR (refer to the 620 test program manual, 98 A 9908 960).

The TTY is a good diagnostic aid because the data being sent are printed out and can be analyzed. Also, known input patterns can be generated (via keyboard or paper tape) and data can be analyzed in the computer or returned to the TTY for printed analysis. If for some reason, such as PTR failure, the test program tapes cannot be read, a simple input/output program for verification and troubleshooting of the TTY-TC operation can be entered through the computer control panel. This program (table 5-1) tests keyboard input and printer output:

a. Enter the program through the control panel.

b. Turn the TTY to ON-LINE.

c. Program starts at location 000000.

d. Any character input from the TTY is transferred back to the TTY as an output from the CPU-TC almost immediately. Various character patterns and functions of the TTY can be checked by this echo method.

Table 5-1. Basic Input/Output Test Program

Location	Command	Description
00000	101201	Sense read ready.
00001	000004	If yes, jump to 00004.
00002	001000	Jump back to 00000.
00003	000000	
00004	102501	Clear and input TTY character to A register.
00005	101101	Sense write ready.
00006	000011	If yes, jump to 00011.
00007	001000	
00010	000005	
00011	103101	Output A register (to TC).
00012	001000	Jump back to 00000.
00013	000000	

5.4 CLOCK ADJUSTMENTS

The time settings of the 4.55-millisecond (receive) clock and the 9.1-millisecond (transmit) clock should be periodically checked and adjusted. The time period of the clocks can be monitored and adjusted (if required) while running TTY tests or using the following procedure:

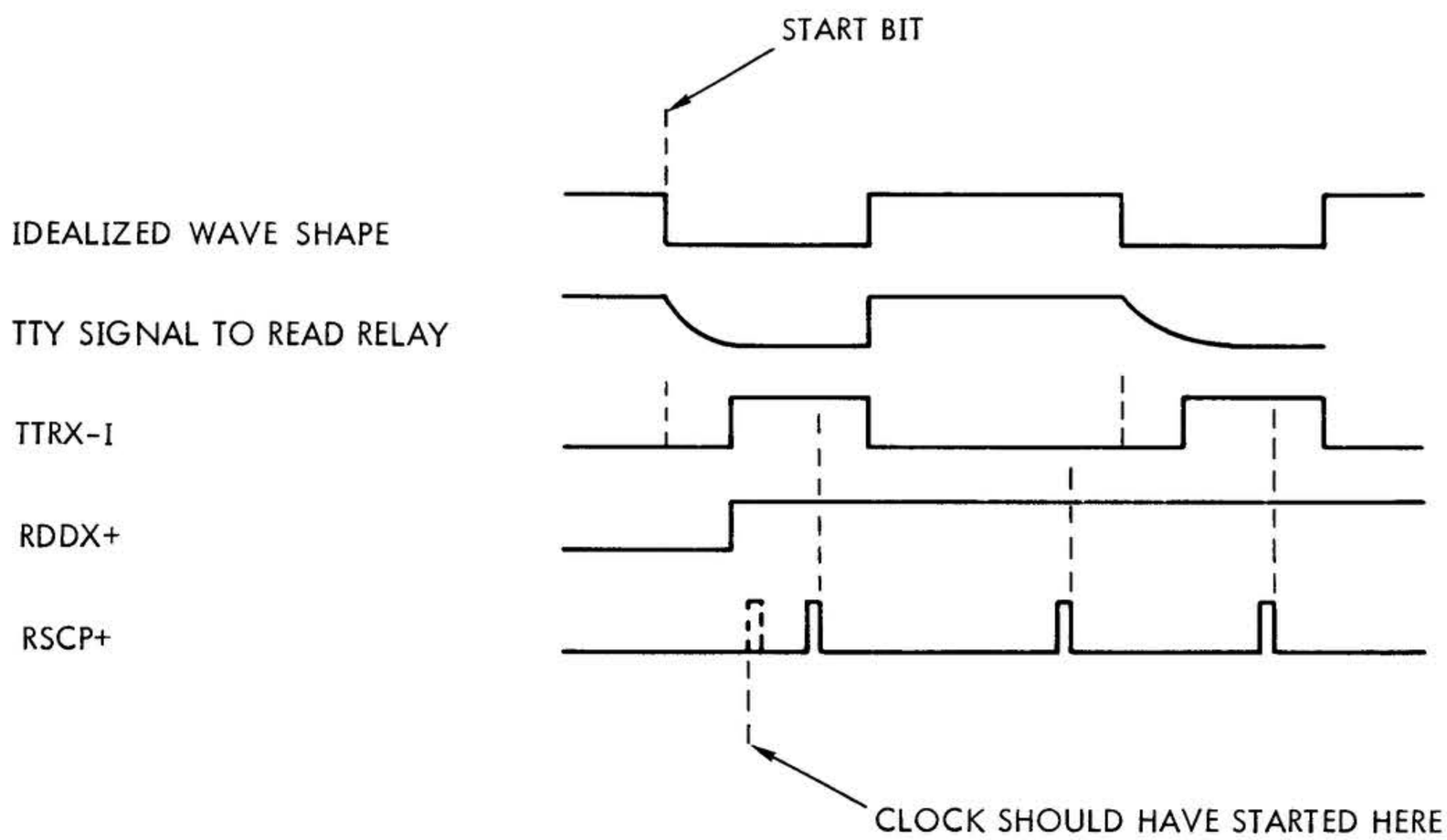
a. Place the TTY motor ON/OFF switch in OFF.

b. Turn the CPU off.

c. Extend the CPU tray out the front and connect an extender cable between CPU tray connectors P1A, P2A, and P3A and backplane connectors J8, J9, and J10. The CPU tray is held firmly to the mainframe with a tray extender assembly. After removing the card retainer bar, the DM274 TC card is accessible for troubleshooting by installing it in a DM265 extender card (44P0437). Turn on the CPU.

In addition to the TTY read clock frequency adjustment potentiometer, the one-shot that compensates for character distortion because of the slow pull in time of the read relay and the inherent TTY distortion can also be adjusted. The distortion, totaling approximately 2 nanoseconds, delays the enabling of the read clock (RDDX+), which, in turn, delays the shift clock pulse to the read register (RSCP+) (figure 5-1).

This delay error can be corrected by shortening the first clock period (RCLP+) of the read clock (for each input character). The following sequence occurs: the read relay is de-energized and TTRX+ goes low, dc-setting RDDX+. RDDX+ high fires the one-shot, which shortens the first RCLP+ clock.



VTII-1191

Figure 5-1. Shift Clock Pulse (RSCP+) Delay Adjustment

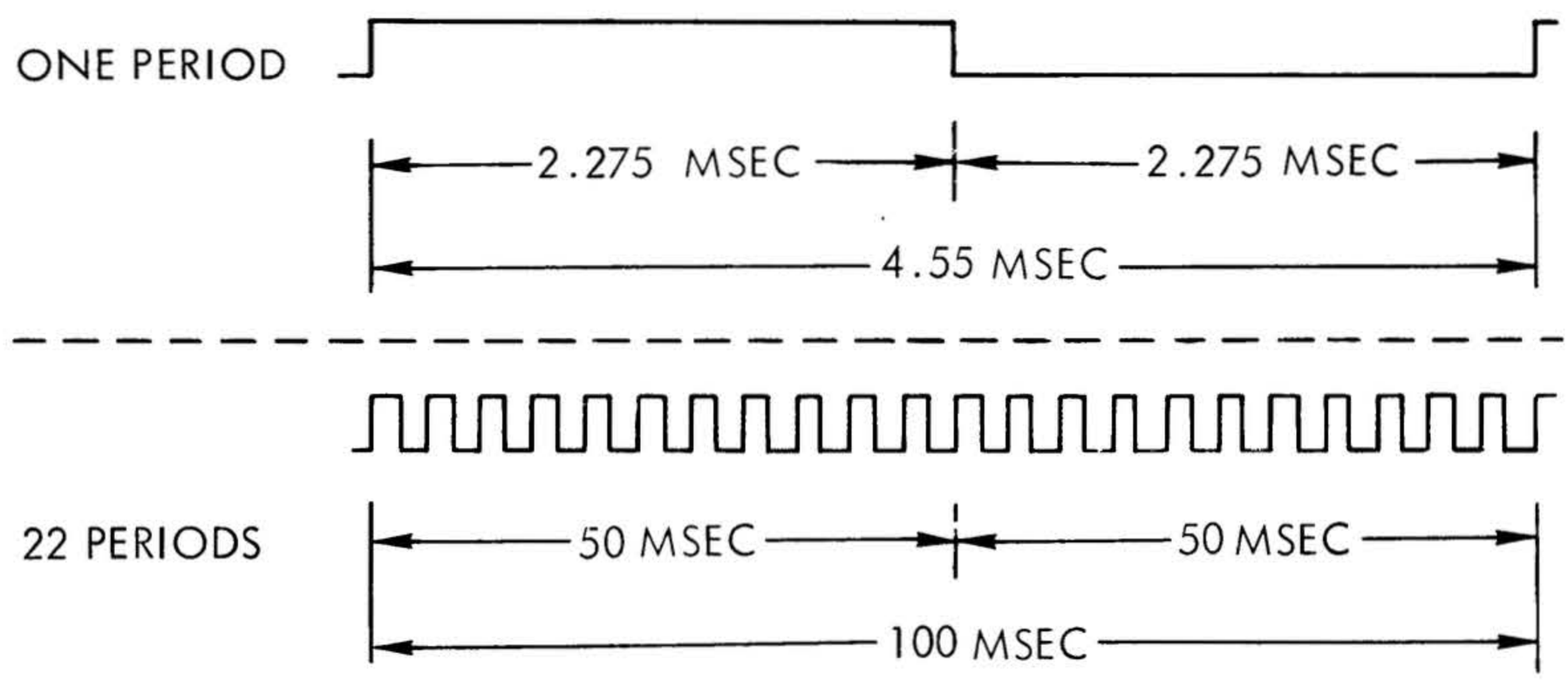
5.4.1 Input Clock Adjustment

Temporarily enable the 4.55-millisecond clock input by grounding TTRX + at pin 13 of T4. The clock will run until the RESET switch on the control panel is pressed.

Oscilloscope setup:	Set TIME to 1 or 2 msec/cm. Set SYNC to positive internal. Set voltage amplitude to (0.2) 2 or (0.5) 5 V/cm.

Place the oscilloscope probe at the junction of pin 8 of W3. Adjust the oscilloscope to obtain one full square-wave period. This should have a time duration of 4.55 milliseconds. If it does not, adjust potentiometer R12 on the DM253 clock card in slot 11 until the correct period is obtained; then switch the scope to observe 22 periods (exactly 100 milliseconds). This will allow fine timing adjustment (figure 5-2). After completing adjustment, the 4.55-millisecond clock can be stopped by removing the temporary jumper and pressing the RESET switch.

Next, with the computer in step mode, place one oscilloscope probe at the junction of pin 10 of T5 (TTRX +) and a second probe at the junction of pin 6 of U4 (RSCX +).



VTI1-0557A

Figure 5-2. Waveforms for Receive Clock Adjustment

Oscilloscope setup: Set TIME to 1 or 2 msec/cm.

Set SYNC to trigger (−) on TTRX+.

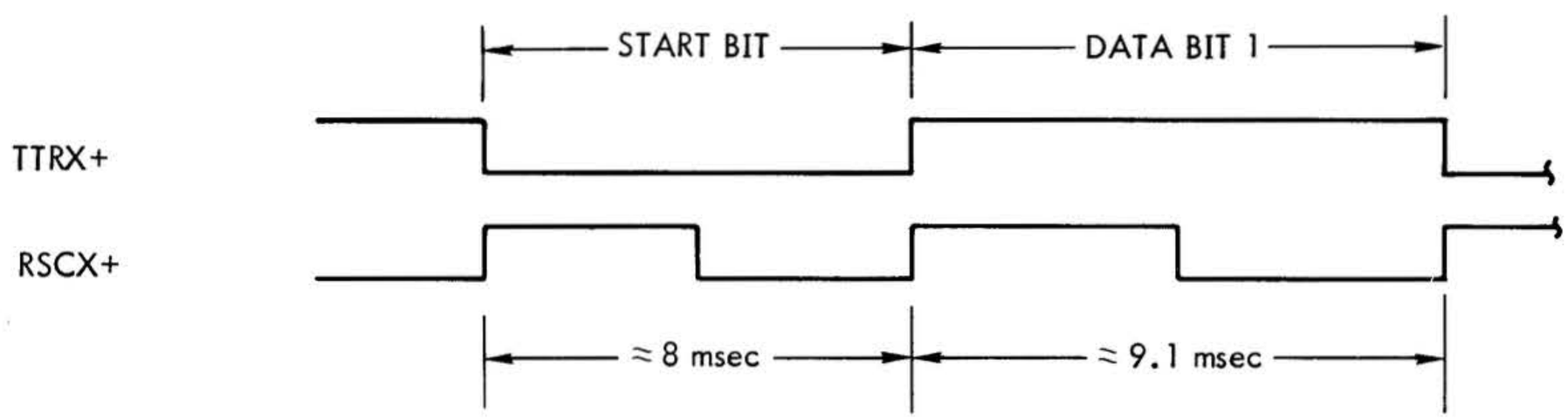
Set voltage amplitude of both probes to (0.2)2 or (0.5)5 V/cm.

Press the REPT on the TTY, then the 1 character momentarily. Keep REPT depressed and observe the waveforms illustrated in figure 5-3. Adjust potentiometer R31 on the DM253 clock card in slot 11 until the high-to-low transition of RSCX+ is centered in the middle of the TTRX+ start bit.

5.4.2 Output Clock Adjustment

The 9.1-millisecond clock runs continuously.

Oscilloscope setup: Set TIME to 1, 2, 5, or 10 msec/cm.
Set SYNC to positive internal.
Set voltage amplitude to (0.2) 2 or (0.5) 5 V/cm.



VTII-1192

Figure 5-3. RSCX+ Centering Adjustment

Place the oscilloscope probe at the junction of pin 3 of X5. Adjust the oscilloscope to obtain one full squarewave period of 9.1 milliseconds. If this period does not occur, adjust potentiometer R2 on the DM253 clock circuit card until the correct period is obtained; then switch the oscilloscope time base to observe 11 periods (exactly 100 milliseconds).

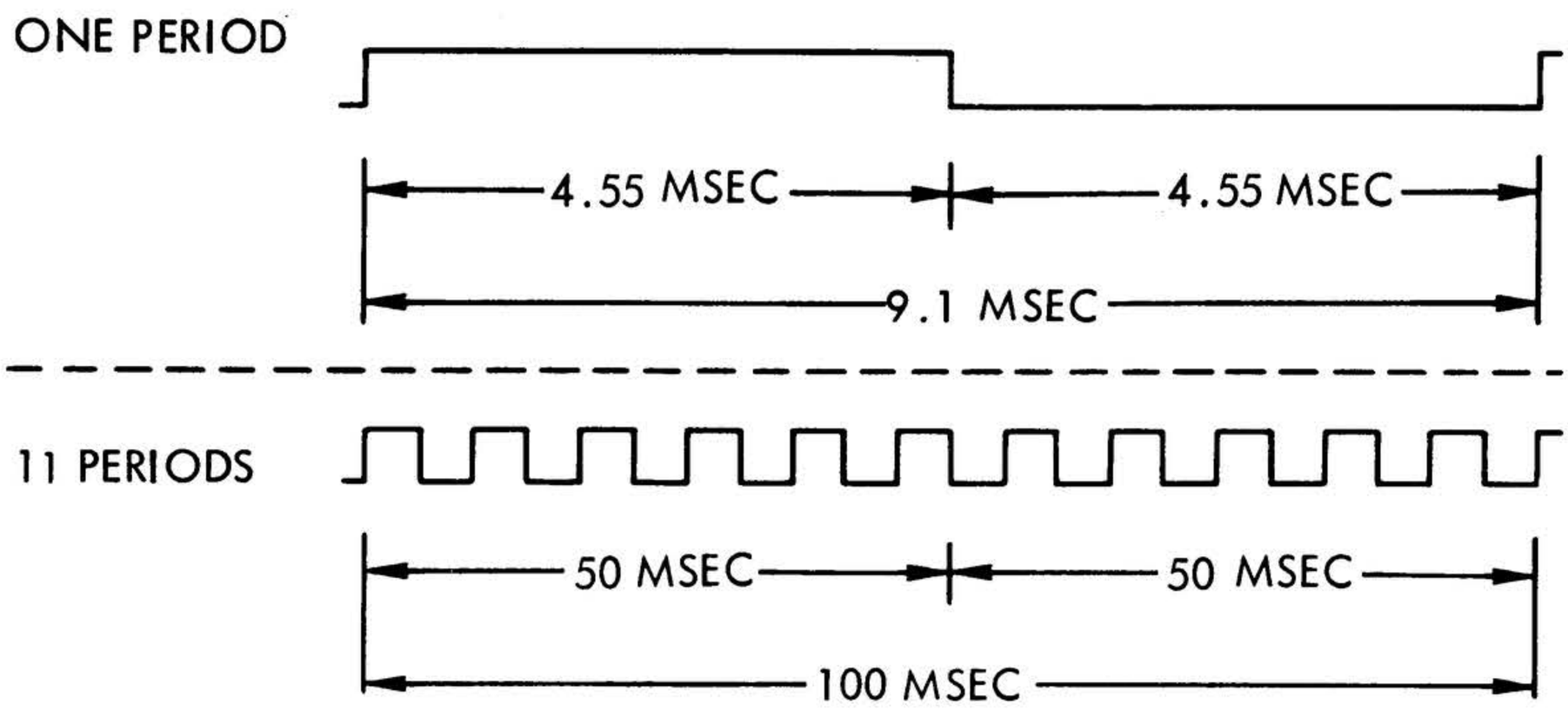
Switch the scope to observe 22 periods. This should take exactly 200 milliseconds. Switching the scope to observe many periods is important because adjustment of the 9.1-millisecond clock is critical. Observing many periods allows the adjustment to be more accurately timed (figure 5-4).

5.5 TC/TTY TROUBLESHOOTING

The TTY units are normally trouble-free and require little attention; however, if operation is faulty, the following troubleshooting procedures are suggested. Visually inspect for broken belts, loose cams or components, loose or poorly seated connectors, blown fuses, or burned-out components.

NOTE

The TTY casework is cast and, therefore, somewhat fragile. Exercise care when removing and reinstalling it.



VT11-0566A

Figure 5-4. Waveforms for Transmit Clock Adjustment

5.5.1 Garbling

The following are possible sources of intermittent character change (printing or sending wrong characters).

TTY	Incorrect power supply output
TTY	Incorrect motor speed
TTY	Incorrect range adjustment
TC	Incorrect 9.1- or 4.55-millisecond clock frequency
TTY-TC	Incorrect loop current (too low or too high)

5.5.2 Motor Speed Check

The TTY character output rate must be 100 milliseconds per character. The motor speed, which is not adjustable, can be checked as follows.

a. Check RDDX (T4, pin 2) with an oscilloscope. Set oscilloscope SYNC to positive internal and set scope time to 10 or 20 msec/cm.

b. Hold down the RUBOUT and REPEAT keys on the TTY keyboard. Adjust oscilloscope to observe the RRDX waveform. RDDX should set on every start bit and remain set until stop-bit time, resetting on each new start bit. The time from set to set should be exactly 100 milliseconds. Switch the oscilloscope to observe that 10 characters occur each second. If single character time is off by more than 2 milliseconds, the TTY motor may require change, overhaul, readjustment, or other maintenance.

5.5.3 Range Adjustment

The TTY receive section has a compensating RANGE knob (model 35) or lever (model 33) that may require occasional adjustment. The purpose of range adjustment is to compensate for receive loop distortion and to position the receiving loop mechanism for optimum sampling of the incoming signal. Before attempting range adjustment, verify proper TC output character length.

Full range adjustment is from 0 to 120. Factory-modified TTY model 33 ASR optimum range adjustment is at or near the center, normally 60 to 65. If range adjustment is required, send an alternate pattern such as period. . .from the CPU. Loosen the range set

screw (model 33) or pull out the range knob (model 35) and slowly vary the setting of the knob or lever while observing the pattern being printed. When the characters begin to change (garble), one end of the effective range has been reached. Note the location of this point on the adjustment knob or lever. Move the adjustment in the opposite direction. The printed characters should clear up and then begin to garble when the other end of the range is reached.

Note the position of this point on the adjustment knob or lever, and position the range knob or lever midway between the observed range limit points. Tighten the set screws, if applicable.

Range adjustment and motor speed should be checked if intermittent failures occur or after any major overhaul of the TTY.

5.5.4 Signal Checks

The TC/TTY interface signals can be checked at P3 of clock circuit card DM253 with an oscilloscope. To check receive relay K1 when the TC is receiving from the TTY, connect oscilloscope common to P3 pin 36 and oscilloscope probe to P3 pin 34. To check send relay K2 when the TC is sending to the TTY, connect oscilloscope common to P3 pin 36 and oscilloscope probe to P3 pin 30. In each case, the bit pattern observed on the oscilloscope should be essentially rectangular and free from distortion. These signals can also be checked with a voltmeter at P3 (table 5-2).

Table 5-2. TC/TTY Interface Voltages

Setup Conditions		DC Meter Connections to Clock Card DM253		
Computer Power	TTY Mode	Common	Hot	Approximate Voltage
ON	On-line	P3,pin 36	P3,pin 30	0V dc
(K2 relay contacts closed)		P3,pin 36	P3,pin 30	45V dc
	Off-line	P3,pin 36	P3,pin 30	30V dc
OFF	On-line TTY running open	P3,pin 36	P3,pin 30	0-2V dc
(K2 relay contacts open)		P3,pin 36	P3,pin 30	42V dc
	Off-line	P3,pin 36	P3,pin 30	42V dc

5.5.5 Test Points

Table 5-3 lists some common test points on the TC. When signal synchronization is required, the following points can be used.

a. For output to the TTY, the start bit of output character begins when WSEX goes high.

   Sync positive on S4-9.

b. For input from the TTY, the start bit of input character begins when RDDX + goes high.

   Sync positive on T4-2.

c. For input to the CPU, the input character sequence can begin any time after RRDY + goes high.

   Sync negative on U5-3.

d. For output from the CPU, the output loading can begin any time after WRDY + goes high.

   Sync positive on S4-5.

Table 5-3. Common TC Test Points

Circuit	Signal	Test Point
Output	WRDY (9.1-msec clock)	S4-5
	WSCP	N2
	Output to TTY (TTDO)	W5-6
	WLDX	S-5
	WSEX	S4-9 or X5-2
	W00X	W4-2
TC/CPU	DAXX	M3-1

Table 5-3. Common TC Test Points *(continued)*

Circuit	Signal	Test Point
	FRYX-C	M5-13
	DRYX-C	M5-11
	SERX-C	R4-8
	DTOX	M2-6
	DTIX	M2-2
	EXCX	M3-11
Input	RRDY (4.55-msec clock)	U5-2
	RSCP	N3-6
	RRCP	S5-11
	RDDX	T4-2
	RRCX	U4-13
	TTRX (TTY input data)	T4-13
	Input from TTY (TTRX-I)	T5-11

5.5.6 Troubleshooting Check List

If the TC and TTY are not operating:

a. Check voltages.

b. Check cable connections and board seating.

c. Check that the 4.55-millisecond clock oscillator starts and stops and that the 9.1-millisecond oscillator runs.

d. Check that relays K1 and K2 are energized in normal static nonoperating condition. If not, the source of the problem may be the TTY, the relay loop supply, or a relay.

If the TC and TTY have intermittent problems:

a. Check voltages.

b. Check cable connections and board seating.

c. Remove and inspect the TC board for loose components, poor solder connections, and wrong-value components.

d. Check the 9.1- and 4.55-millisecond clock timing and, if necessary, adjust it.

e. Observe the send and receive signals across the TTY relay lines.

NOTE

The K1 and K2 relays occasionally fail. Symptoms are excessive contact bounce and degraded make-break characteristics. Loop current provided by the TTY can be too high or too low. Loop current should be checked and should be about 20 mA.

5.6 REFERENCE DOCUMENTS

In addition to this manual, the documents listed below are be useful as aids to understanding and maintaining the TC.

a. 620/f Reference Handbook (98 A 9908 001)

b. 620 Test Program Manual (98 A 9908 960)

c. 620/f Maintenance Manual (98 A 9908 050)

d. DM274 Logic Diagram (91D0219)

e. DM253 Clock Assembly Drawing, (91C0209)

SECTION 6
DRAWINGS AND PARTS LISTS

This section contains logic schematics and parts information for the TC and clock circuitry.

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. THIS DRAWING CONSISTS OF THE FOLLOWING SHEETS:
   1.0, 2.0, 3.0, 4.0, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0, 11.0

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C 37	C1, 2, 5, 6 C13-23
P3	P2

REFERENCE DRAWINGS	
44D0451	ASSEMBLY
44P0451	PARTS LIST
95W0606	WIRE LIST
40D0458	P.W. BOARD
97D0538	ARTWORK
97D0539	SILKSCREEN (COMP)
97D0540	SILKSCREEN (CKT)
97D0542	SOLDER MASK

DR	MANCARELLA	4-21-71
CHK	WGD	4/30/71
DSGN	—	
ENGR	R C DRUMM	10/13/70
APPD	D BROCKETT	10/13/70
APPD	D MARTIN	10/13/70

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TITLE
LOGIC DIAG,
TTY/ABL CONT.

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE	620/F-15	SHEET	1.0

SOURCE	SIGNAL	DIST. POINT
N3-7	GNDM2	M2-7
M3-7	GNDN2	N2-7
U3-7	GNDU3	U3-2, U3-1
V3-7	GNDV3	V3-2, V3-1

SOURCE	SIGNAL	DIST. POINT
M3-14	VCCM2	M2-14
N3-14	VCCN2	N2-14
U2-14	VCCU2	U2-8

POWER AND GRD WIRED DISTRIBUTION

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 4.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8

CONNECTOR P1

PINS	FUNCTION	SHEET
1	+5V	
2	GRD	
3	+5V	
4	GRD	
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
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28		
29		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		

CONNECTOR P1

PINS	FUNCTION	SHEET
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
55	AB00-C	11.0
56	AB01-C	11.0
57	AB02-C	11.0
58	AB03-C	11.0
59	AB04-C	11.0
60	AB05-C	11.0
61	AB06-C	11.0
62	AB07-C	11.0
63		
64		
65		
66		
67		
68		
69		
70		
71		
72		
73		
74		
75		
76		
77	+5V	
78	GRD	
79	+5V	
80	GRD	

CONNECTOR P2

PINS	FUNCTION	SHEET
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		

CONNECTOR

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 5.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8

CONNECTOR P3

PINS	FUNCTION	SHEET
1	+5V	
2	GRD.	
3	+5V	
4	GRD.	
5		
6		
7		
8		
9	RDDX+	9.0
10	SDTØX-	9.0
11	WRDY-	8.0
12	RCLP+	9.0
13		
14	AB11-C	7.0
15		
16		
17	IUAX-C	7.0
18	DRYX-C	7.0
19		
20	FRYX-C	7.0
21		
22		
23	TTRX-I	11.0
24		
25		
26	WCKP+	8.0
27		
28		
29		
30		
31		
32		
33		
34	SERX-C	7.0
35	AB13-C	7.0
36	AB14-C	7.0
37	AB08-C	7.0
38	SYRT-C	7.0
39		
40		
41		

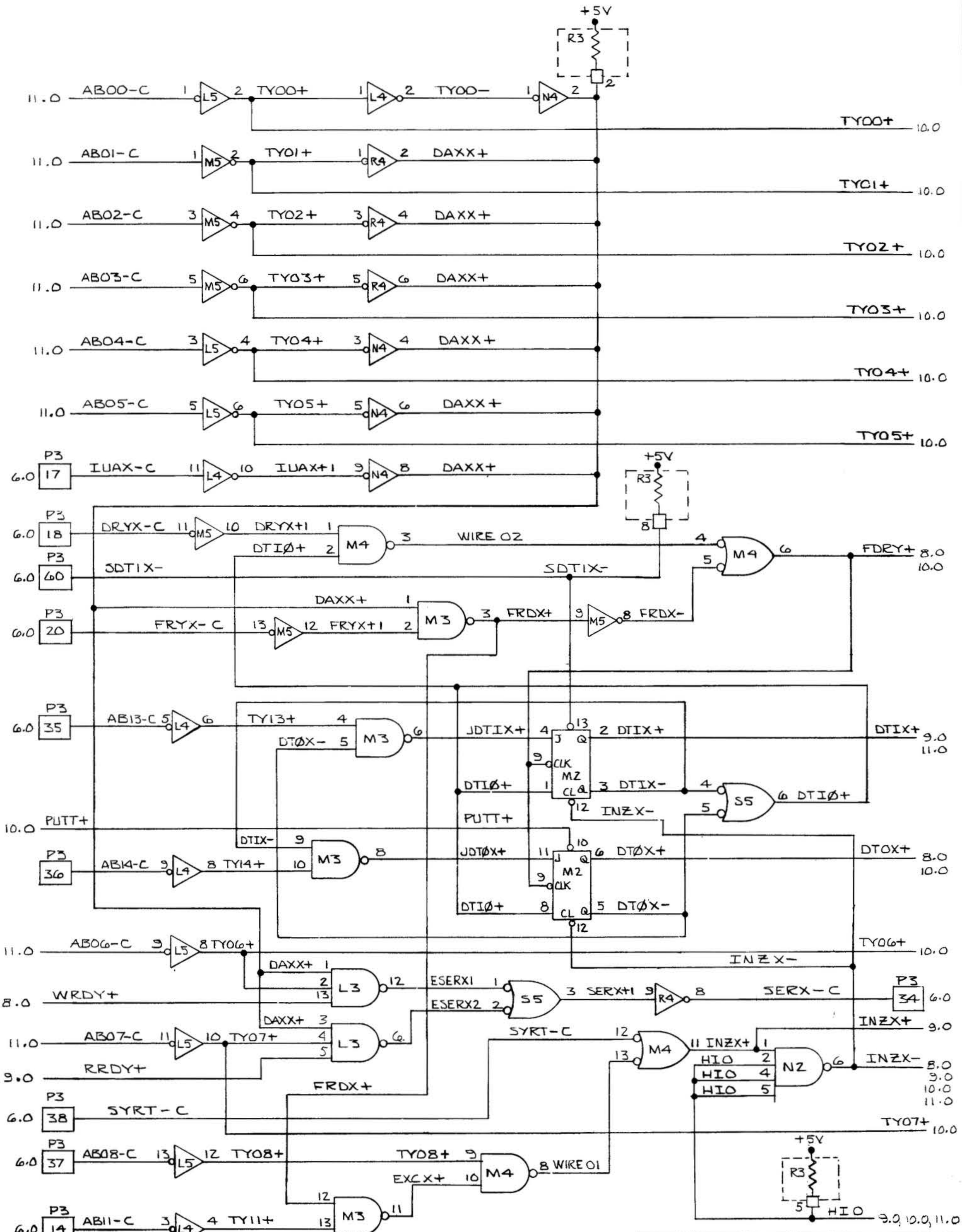
CONNECTOR P3

PINS	FUNCTION	SHEET
42		
43		
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
55		
56		
57		
58		
59		
60	SDTIX-	7.0
61		
62		
63		
64		
65		
66		
67		
68		
69	IUAA-I	8.0
70	IUBB-I	9.0
71		
72		
73		
74		
75	TTDØ-	10.0
76		
77	+5V	
78	GRD.	
79	+5V	
80	GRD.	

CONNECTOR

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 6.0	

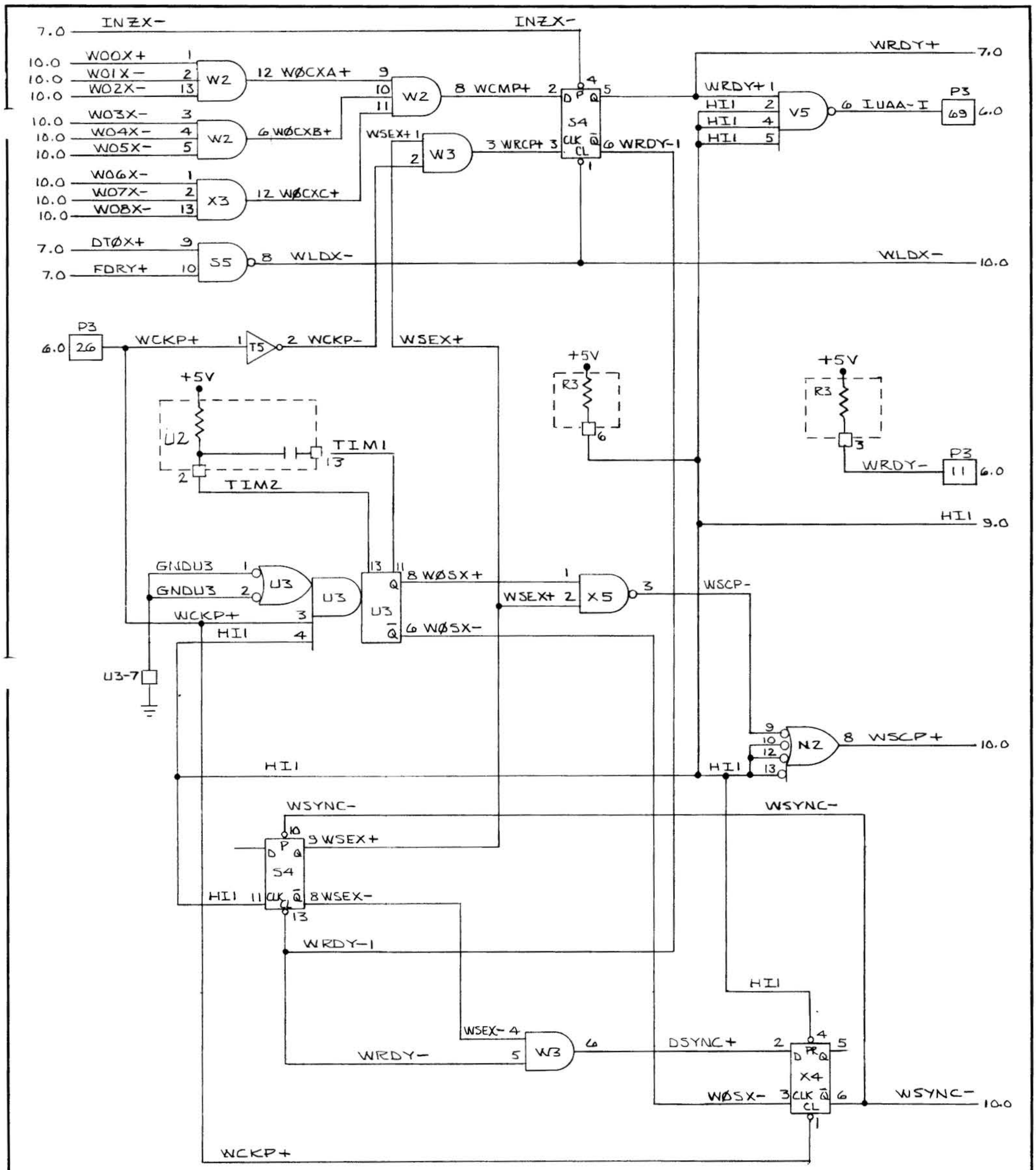
1/70 DIETERICH-POST CLEARPRINT 1000H-8



CONTROL LOGIC AND SENCE RESPONSE

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 7.0	

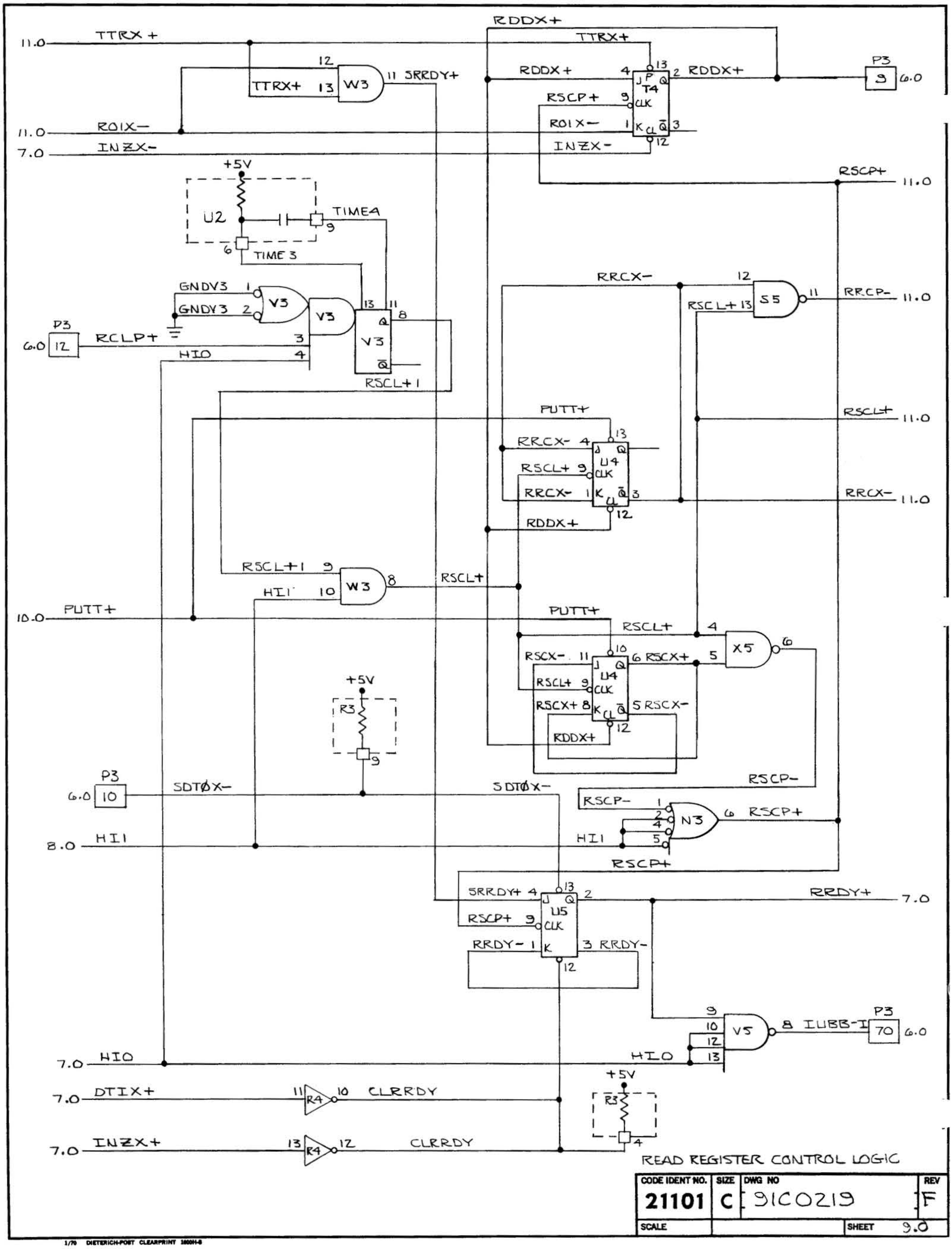
1/70 DIETERICH-POST CLEARPRINT 1000H-8



WRITE REGISTER CONTROL LOGIC

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 8.0	

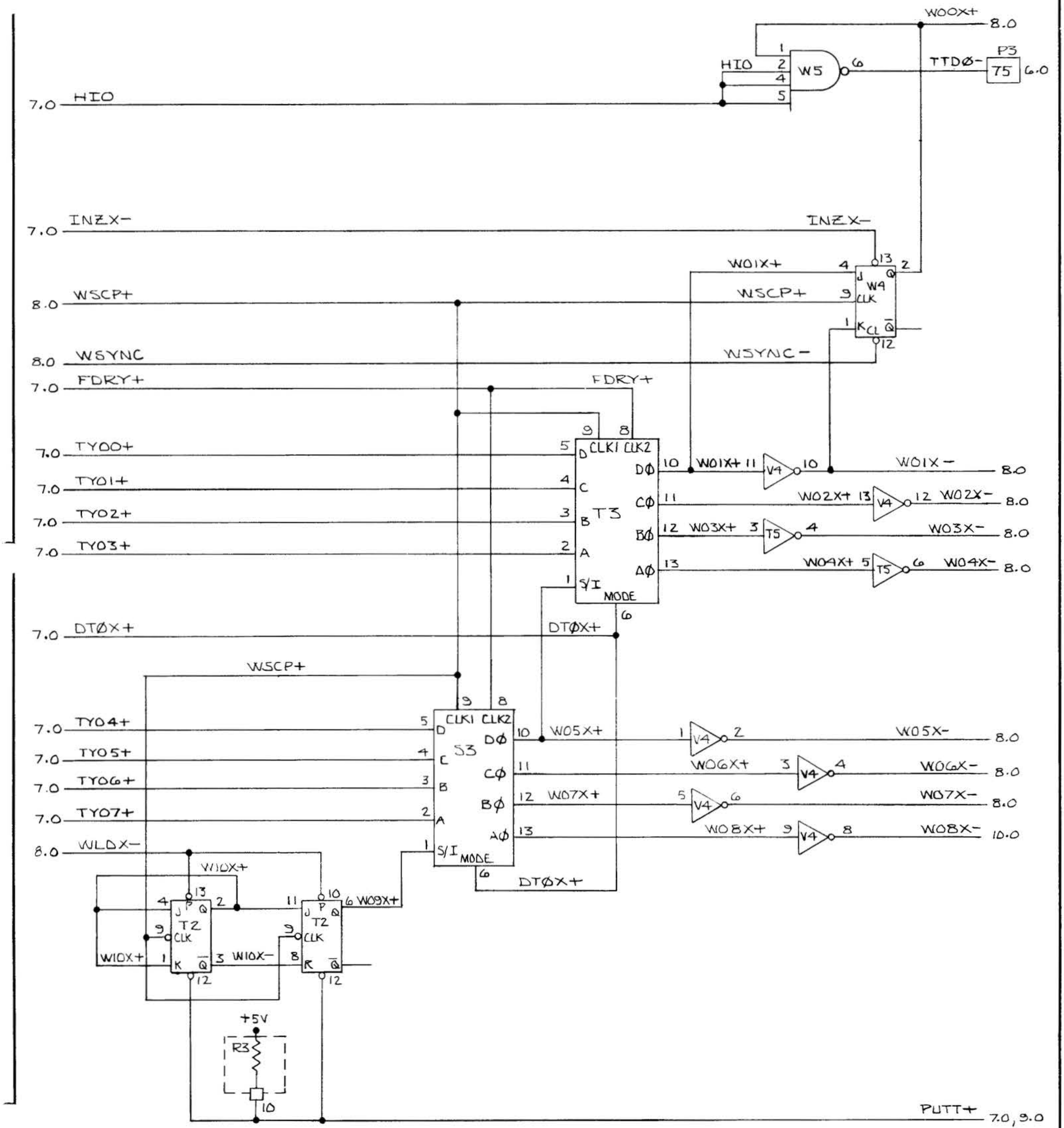
1/70 DIETERICH-POST CLEARPRINT 1000H-B



READ REGISTER CONTROL LOGIC

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9C0219	F
SCALE		SHEET 9.0	

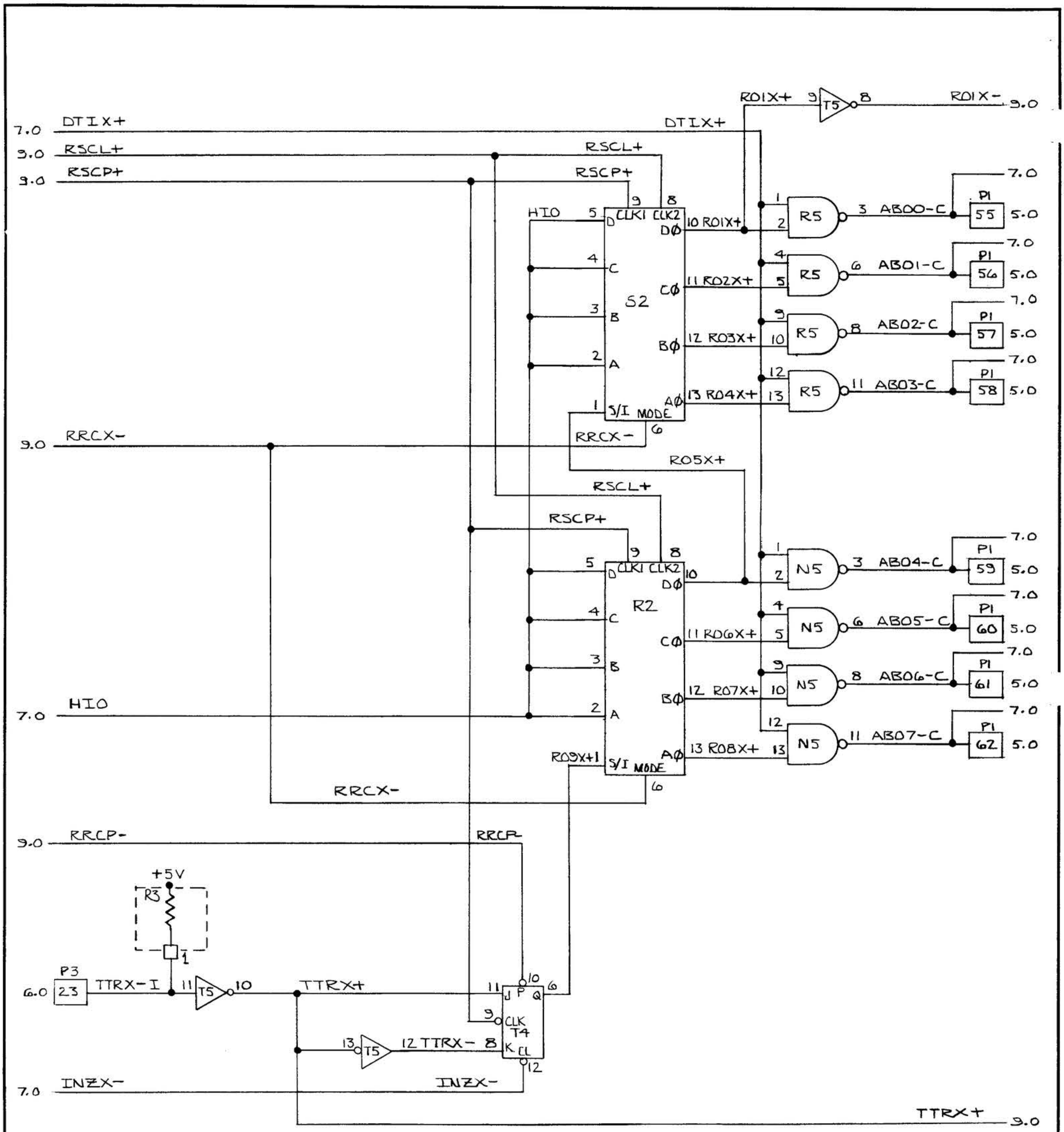
1/70 DIETERICH-POST CLEARPRINT 1000H-8



WRITE REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0219	F
SCALE		SHEET 10.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8



READ REGISTER

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	9C0219	F
SCALE		SHEET 11.0	

1/70 DIETERICH-POST CLEARPRINT 1000H-8

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DWG. NO. 44P0451

PARTS LIST

CODE IDENT 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				REF	REF	REF	–	44D0451 E	ASSEMBLY		
				REF	—	REF	–	95W0606 E	WIRE LIST		
				REF	REF	—	–	95W0723 A	WIRE LIST		
				REF	—	REF	–	91C0219 F	LOGIC DIAGRAM		
				REF	REF	—	–	91C0261 A	LOGIC DIAGRAM		
				1	1	1	1	40D0458-000	P.W. BOARD		
				31	14	18	2	71A0009-003	CAPACITOR .1 μf		
				6	3	4	3	71N0200-225	CAPACITOR 2.2 μf		
				6	–	6	4	49A0099-000	I.C. SN74H108N		
				2	–	2	5	49A0019-000	I.C. SN74H40N		
				6	2	4	6	49A0090-001	I.C. SN7495N		
				3	1	2	7	49A0022-000	I.C. SN74H11N		
				1	–	1	8	49A0009-000	I.C. SN15862N		
				3	1	2	9	49A0104-000	I.C. MC3001P		
				2	1	1	10	49A0025-000	RESISTOR ASSY		
				2	–	2	11	49A0524-000	I.C. U6E960129		
				6	2	4	12	49A0040-000	I.C. SN7404N		
				1	–	1	13	49A0039-000	I.C. SN74H00N		

NEXT ASSY 01A0951 MODEL NO 620/f-15 APPD [illegible]

REV	A	B	C	D	E	F	G	H
EN NO	4847	4913	5007	5082	5152	5246	5269	5340
DATE	10-10-[illegible]	11-23-70	1-11-71	1-11-71	1-11-71	4-21-71	4-21-71	4-21-71
DR	J.Z.	GRL	DM	D.W.	DW	JM	JM	JM
CHK	B.B.	RAD	RAD	RAD	RAD	WKO 4/29/71	WKO 4/29/71	WKO 4/29/71

TITLE: PARTS LIST
TTY/ABL CONTROLLER ASSY

DWG NO 44P0451 REV H

SHEET 1 OF 2

96A0017-000B

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DWG. NO. 44P0451

PARTS LIST

CODE IDENT: 21101

QUANTITY REQ'D PER DASH NO							FIND NO	PART NUMBER	DESCRIPTION	REMARKS	ZONE
				002	001	000					
				4	2	2	14	49A0575-000	I.C. SN7405J		
				4	2	2	15	49A0012-000	I.C. SN7474N		
				1	-	1	16	49A0023-000	I.C. SN74H04N		
				9	7	2	17	49A0081-001	I.C. SN7403N		
				2	-	2	18	49A0010-000	I.C. SN6006N		
				3	1	2	19	49A0007-000	I.C. SN7400N		
				1	-	1	20	01C0995-000	COMPONENT ASSY		
				59	22	37	21	58A0060-000	SOCKET, 14 PIN		
				2	2	-	22	58A0060-001	SOCKET, 16 PIN		
							23				
				174	72	174	24	58A0062-002	POST, WIRE WRAP		
				1	1	1	25	16S1057-061	CARD HANDLE		
				0	0	0	26	53A0333-040	WIRE, KYNAR, YEL	30 AWG	
				1	1	1	27	16S1057-056	CARD HANDLE		
				2	2	-	28	49A0112-000	I.C. SN7493N		
				1	1	-	29	49A0041-000	I.C. SN74H51N		

NOTES:

DWG NO 44P0451

REV H

SHEET 2 OF 2

96A0017-001B

TELETYPEWRITER ASCII CODES

Character	ASCII	Character	ASCII
@	300	X	330
A	301	Y	331
B	302	Z	332
C	303	[	333
D	304	\	334
E	305	]	335
F	306	↓	336
G	307	←	337
H	310	blank	240
I	311	!	241
J	312	"	242
K	313	#	243
L	314	$	244
M	315	%	245
N	316	&	246
O	317	'	247
P	320	(	250
Q	321	)	251
R	322	*	252
S	323	+	253
T	324	,	254
U	325	–	255
V	326	.	256
W	327	/	257

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