INDEX - SYSTEM MAINTENANCE MANUAL

	SECTION	CONTENTS
1.	System Data	Documentation Record Manual Listing System Memo (s) Systems Arrangement Drawing
2.	Engineering Specifications	Engineering Description PPS (s), SPS (s), Maintenance Aid
3.	Test Data	Memory Schmoo Diagram
4.	Circuit Boards	Assembly Drawing Logic Diagrams Parts Lists
5.	Power Supply	Procurement Spec. or Assy. Dwg. Vendor or VDM Schematic Parts Lists
6.	Wire Lists	All wire lists
7.	Option Documentation	Option and Controller documentation matched to the revision level (s) of the equipment.
8.	Change Notices	All EN's affecting any of the supplied documentation contained in this manual.

Please note the above is a standard index. Each System Maintenance Manual is assembled to meet specific system requirements and may not require all documentation shown on the index. Please be assured all maintenance documentation required to service this system has been included.

additional routing

alesman # 2420
D. Bryant
R. Douglas
M. Drees (2)
M. Peralta
~~Prod. Control~~
Q.C.
Sales Admin. (2)
C. Stark (2)
Job File

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2722 michelson drive / irvine / california / 92664 / (714) 833-2400

Note: Please forward along with other documentation.

system memo V73

DF-1046-s.c.

customer: Sperry Systems Management

sales order: 64490

charge number: 64490

date: February 21, 1975

from: D. Frazen D.E.F.

Please reference Systems Arrangement Drawing No. 93E0831X

V-73

INDEX:

1.0 Equipment Summary

This is a 32K SC Memory V73 Computer System.

- V73, 14" Chassis, Power Supply, Console, DMA, PMA, PFR, RTC, HM/D, TTY, Memory Protect (E3520)
- 32K SC Memory with Data Save (73-2500 - 73-3200)
- Disc ABL
- WCS and Power Supply (73-4001 - 73-4009)
- Floating Point Processor (73-3400)
- 1 each I/O Chassis (73-9004) w/I/O Expander Board.
- 1 each I/O Chassis (73-9005)
- 1 each I/O Expander (73-9006)
- 3 each PIM (73-3101)
- 3 each BIC (73-3102)
- 1 each TTY ASR 33 (70-6100)
- 1 each MT Master (70-7102)
- 1 each Disc (70-7600)
- 2 each Buffered I/O Controllers (70-8301)
- 1 each Digital Input Module (70-8410)
- 4 each Digital Input Expansion (70-8411)
- 3 each cabinets 9202 (one 2 Bay, one 1 Bay)
- VORTEX (MT9) (70-9500)
- Maintain II (70-9570)

V70

MANUAL LISTING

V73 HANDBOOK	9809906-010
PROCESSOR	9809906-023
* CORE MEMORY	9809906-031
* SEMI CONDUCTOR MEMORY	9809906-040
OPTION BD.	9809906-051
POWER SUPPLY	9809906-063
TEST PROGRAMS	9809952-061
MICROPROGRAMMING	9809906-073
BIC	9809902-115
PIM	9809902-426
BUFFERED I/O	9809902-625
WCS	9809906-082
WCS POWER SUPPLY	9809910-000
VORTEX INST. MANUAL	9809952-250
VORTEX REF.	9809952-103
FLOATING POINT PROCESSOR	9809906-110

NOTE: * Manual shipped only for the type memory used.

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DOCUMENTATION RECORD

CUSTOMER SPERRY SYST. MANAGEMENT JOB ORDER NO. 64490

MODEL NO. V-73

SYS. SERIAL NO. 605

UNIT	DOCUMENTATION NO	REV	S/N	DESCRIPTION
	44P0656	S	200	WCS BOARD
	83P0044	G	236	WCS POWER SUPPLY
	83P0044	G	235	WCS POWER SUPPLY
	44P0670	F	535	I/O PARTY LINE EXPANDER
	44P0683	A	344	PIM
	44P0683	A	305	PIM
	44P0683	A	515	PIM
	44P0689	N	1142	BIC
	44P0689	N	1144	BIC
	44P0689	N	1145	BIC
	44P0674	B	173	BUFFERED I/O CONTROLLER
	44P0674	B	187	BUFFERED I/O CONTROLLER
		-	006	ASR 33 TTY
		-	6541	MAG TAPE TRANSPORT
	44P0657	B	139	MAG TAPE CONTROLLER
	44P0658	C	154	MAG TAPE CONTROLLER
		-	3746	DISC DRIVE
	44P0676	E	184	DISC CONTROLLER
	44P0686	C	120	TERM SHOE
	44P0723	H	027	FLOATING POINT PROCESSOR
	44P0628	G	095	DATA SAVE BOARD
	01P1373	C	090	DATA SAVE POWER SUPPLY
	83P0035	S	517	POWER SUPPLY
	44P0670	F	558	I/O EXPANDER
	44P0684	A	104	TERM SHOE

PREPARED BY _____ DATE _____ NOTE:

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DOCUMENTATION RECORD

CUSTOMER SPERRY SYST. MANAGEMENT JOB ORDER NO. 64440

MODEL NO. V70

SYS. SERIAL NO. 605

UNIT	DOCUMENTATION NO	REV	S/N	DESCRIPTION
	98A0879	--	-----	Parts List
	98A0887	--	-----	Micro Word Flowcharts
	49A0195	--	-----	Control Store Code Listing
	81L1709-001	--	-----	Central Control Store Listing
	(44P0614) 91B0378	BK	605	Processor Bd.
	(44P0619) 91B0401	BP	316	Option Bd.
	(44P0613) 91C0377			Core Memory
	(44P0613) 91B0377			Core Memory
	(44P0613) 91B0377			Core Memory
	(44P0645) 91B0406	P	503	Display Bd.
	(44P0625) 95D0940	A	1595	Term Shoe
	(44P0625) 95D0940	A	1583	Term Shoe
	(44P0664) 95D0970	A	1598	Term Shoe
	(44P0664) 95D0970	A	164	Term Shoe
	(44P0608) 95D0911			Back Plane
	(44P0609) 95D0912	L	527	Back Plane
	(01P1320) 95E0923	N	408	Power Supply
	(44P0610) 95C0918	E	623	Reg. Bd.
	(44P0611) 91D0388	H	413	Reg. Bd.
	(44P0679) 91D0451	D	266	Reg. Bd.
	(44P0615) 95D0932	F	408	Heat Sink Bd.
	(44P0617) 95E0941	K	489	Power Supply Bd.
	(44P0623) 91D0387	L	629	Power Fail Bd.
	83P0035	S	568	Exp. Power Supply
	(44P0618) 91C0397	AE	118	Semi Cond. Memory
	(44P0618) 91C0397	AE	033	Semi Cond. Memory
	(44P0618) 91C0397	AE	191	Semi Cond. Memory
	(44P0618) 91C0397	AE	192	SEMI COND. MEMORY

PREPARED BY _____ DATE _____ NOTE:

PIM PIN ASSIGNMENT

The PIM (1 to 8 AC External Interrupts) are brought into PIM Board via Front Pins or via J1 or J2 "EDGE" connectors on the later model PIM Board.

FUNCTION	FRONT PINS	J1 or J2
ILOO-	108	3
R	107	4
ILO1-	114	13
R	113	14
ILO2-	104	9
R	103	10
ILO3-	110	15
R	109	16
ILO4-	102	11
R	101	12
ILO5-	88	5
R	87	6
ILO6-	112	1
R	111	2
ILO7-	86	7
R	85	8

NOTE: ILOO- is highest priority; IL07- is lowest priority

PIM = DM124

Input Levels = +5V = OFF = No Int.

= Ov = ON = INT.

I/O jumpers for PIM Interrupt Addresses:

100-117 = 74 - 63, 80 & 106 = Open
120 - 137 = 74, 80 & 106 = Open
140-157 = 106-74, 74 - 63, 80 = Open
160 - 177 = 106 - 63, 74 & 80 = Open

SIGNAL NAME	FROM	TO	REMARKS
(097	A-097	B-097	
X098	A-098	B-098	
X099	A-099	B-099	
X101	A-101	B-101	
X102	A-102	B-102	
X103	A-103	B-103	
X104	A-104	B-104	
X105	A-105	B-105	
X106	A-106	B-106	
X107	A-107	B-107	
X108	A-108	B-108	
X109	A-109	B-109	
X110	A-110	B-110	
X111	A-111	B-111	
X112	A-112	B-112	
X113	A-113	B-113	
X114	A-114	B-114	
X115	A-115	B-115	

WIRE LIST No. 001 | By | CODE IDENT 21101 | WL 95W0271 | REV A

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SHEET 2 | DATE

SIGNAL NAME	FROM	TO	REMARKS
X063	A-063	B-063	Use 30 AWG
X064	A-064	B-064	Single Strand
X065	A-065	B-065	White Wire
X066	A-066	B-066	
X067	A-067	B-067	
X068	A-068	B-068	
X069	A-069	B-069	
X070	A-070	B-070	
X071	A-071	B-071	
X072	A-072	B-072	
X073	A-073	B-073	
X074	A-074	B-074	
X075	A-075	B-075	
X076	A-076	B-076	
X077	A-077	B-077	
X078	A-078	B-078	
X079	A-079	B-079	
X080	A-080	B-080	
X081	A-081	B-081	
X082	A-082	B-082	
X083	A-083	B-083	
X084	A-084	B-084	
X085	A-085	B-085	
X086	A-086	B-086	
X087	A-087	B-087	
X088	A-088	B-088	
X089	A-089	B-089	
X090	A-090	B-090	
X091	A-091	B-091	
X092	A-092	B-092	
X093	A-093	B-093	
X094	A-094	B-094	
X095	A-095	B-095	
X096	A-096	B-096	

VIRE LIST No. 001 | By

CODE IDENT 21101 | WL 95W0271 | REV A

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SHEET 1 | DATE

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Log No. _____

Page of _ _

Test Date 3-27-75

P.O. No. _____

Pkg Slip No. _____

Quantity _____

Account No. 67490

TEST REPORT

Part or Material V73 SYSTEMS

Manufacturer VDM

Ser. No. 605

SPERRY SYSTEMS

TEST REQUIREMENTS:

Test Category: Rec. ☐ Mfg. ☒ Other _____

Perf. Spec.: Enclosed ☐ Reference _____

TEST RESULTS:

ACCEPT ☒ REJECT ☐

Did ☒ Did Not ☐ Meet Manufacturers or applicable purchase specs.

Comments: V73 WITH DMA, PMA, PFR, RTC, HM/D, TTY + CONTROLLER, MEMORY PROTECT, 32 K IC MEMORY, DATA SAVE, WCS + POWER SUPPLY, FLOATING POINT PROCESSOR, FPP POWER SUPPLY 2 I/O EXPANSION CHASSIS, 2 I/O POWER SUPPLIES, 2 I/O EXPANDERS, 3 PIMS, 3 BIC'S, MAG TAPE + CONTROLLERS, DISK, ABL (DISK), 2 BUFFERED I/O'S, 1 DIM, 4 DIMES, VORTEX (MTS)

Disposition: _____

CONDUCTED BY:

1. Signed Thomas A. Bentley
   Date 3-27-75 Stamp T5

2. Signed _____
   Date _____ Stamp _____

3. Signed _____
   Date _____ Stamp _____

APPROVAL:

A. Signed _____
   Title Test Specialist
   Date 3/27/75 Stamp T 48

B. Signed _____
   Title _____
   Date _____ Stamp _____

S. O. 4472 S/N _____ DATE _____

V73 ADD-ON OPTIONS	Final	Retest After Q. C.
1. EXPANSION CHASSIS (2)	T5	T5
2. POWER SUPPLY (2)	T5	T5
3. PIM 3	T5	T5
4. BIC 3	T5	T5
5. READER CONTROLLER		
6. BUFFERED I/O 2	T5	T5
7. I/O EXPANDER	T5	T5
8. 9 TRACK M. T. U. AND CONTROLLERS	96L	T5
9. 7 TRACK M. T. U. AND CONTROLLERS		
10. REMEX READER		
11. FACIT PUNCH		
12. ASR 33	T5	96L
13. ASR 35		
14. KSR 35		
15. MODEM ( )		
16. RELAY I/O		
17. CARD READER AND CONTROLLER		
18. DISC AND CONTROLLER ( )	96L	T5
19. VRC DRUM AND CONTROLLER		
20. UASC		
21. LINE PRINTER AND CONTROLLER ( )		
22. DAC		

TEST DATA SHEET
V73 FINAL ACCEPTANCE

4490 Processor# _____ Date 2/20

Reference Test Procedure 98A0923

Para.	Test Description	Required Parameter	Actual	Stamp
4.0	Voltage checks V73 chassis and I/O expansion chassis	+5 VDC ± 1%		T5
		+5 M ± 1%		T5
		+20.6 VDC ± 1%		T5
		+20 VDC ± 1%		T5
		-12 VDC ± 1%		T5
		+22.5 VDC ± 1%		T5
		+12 VDC ± 1%		T5
		-5 VDC ± 1%		T5
	LFRTC+ Check	24 VRMS ± 20%	T5	T5
	SPFA- Check	High - Low	T5	T5
	SHST- Check	High - Low	T5	T5
.0	Console Tests	No failures	T5	T5
.1	Basic CPU Operation			
.5	Tests	No failures	T5	T5
.6	Machine Cycle Check	655 ns ± 5		
		325 ns ± 5	T5	T5
.7	Inst. Test Programs	No failures	T5	T5
	Memo Test Programs	No Failures	96	T5
	IPU Test Program	No Failures	T5	96

TEST DATA SHEET
V73 FINAL ACCEPTANCE

Reference Test Procedure 98A0923

Para.	Test Description	Required Parameter	Actual	Stamp
7.0	I/O Test	No failures	T5	T5
8.0	Standard DMA Test	No failures	T5	T5
9.0	High Speed DMA Test	No failures	—	—
10.0	Basic Interrupt Test	No failures	T5	T5
11.0	Memory Wrap Around	No failures	T5	T5
12.0	Power Fail/Restart	No failures	T5	T5
13.0	Real Time Clock	No failures	T5	T5
14.0	Memory Protect	No failures	T5	T5
15.0	Priority Memory Access	No failures	T5	T5
[illegible]	Processor/Option Margins	Inst. 1 4.75 VDC	T5	T5
		Inst. 2 5.25 VDC	T5	T5
16.2	Memory Margins	Step 1	96L	T5
		Step 2	—	T5
		Step 3	96L	T5
		Step 4	96L	T5
		Step 5		
		Step 6		
		Step 7		
		Step 8		
17.0	High Temperature Burn-In	No failures 72 hrs.		

V73 ADD-ON ORDERS	Final	Retest After Q. C.
23. ADC		
24. DIGITAL PLOTTER AND CONTROLLER		
25. CARD PUNCH AND CONTROLLER		
26. MEMORY MODULE ( )		
27. ABL ( )		T5
28. DCM		
29. VORTEX		T5
30. VTAM		
31. PROCESSOR		
32. OPTION BOARD ( )		
33. DISPLAY PANEL ( )		
34. MEMORY EXPANSION CHASSIS		
35 [illegible]	T5	T5
36 [illegible]	T96	T5
37. [illegible]	T96	[illegible]
38 [illegible]	T5	T5
39 [illegible]	T5	T5
40 [illegible]		

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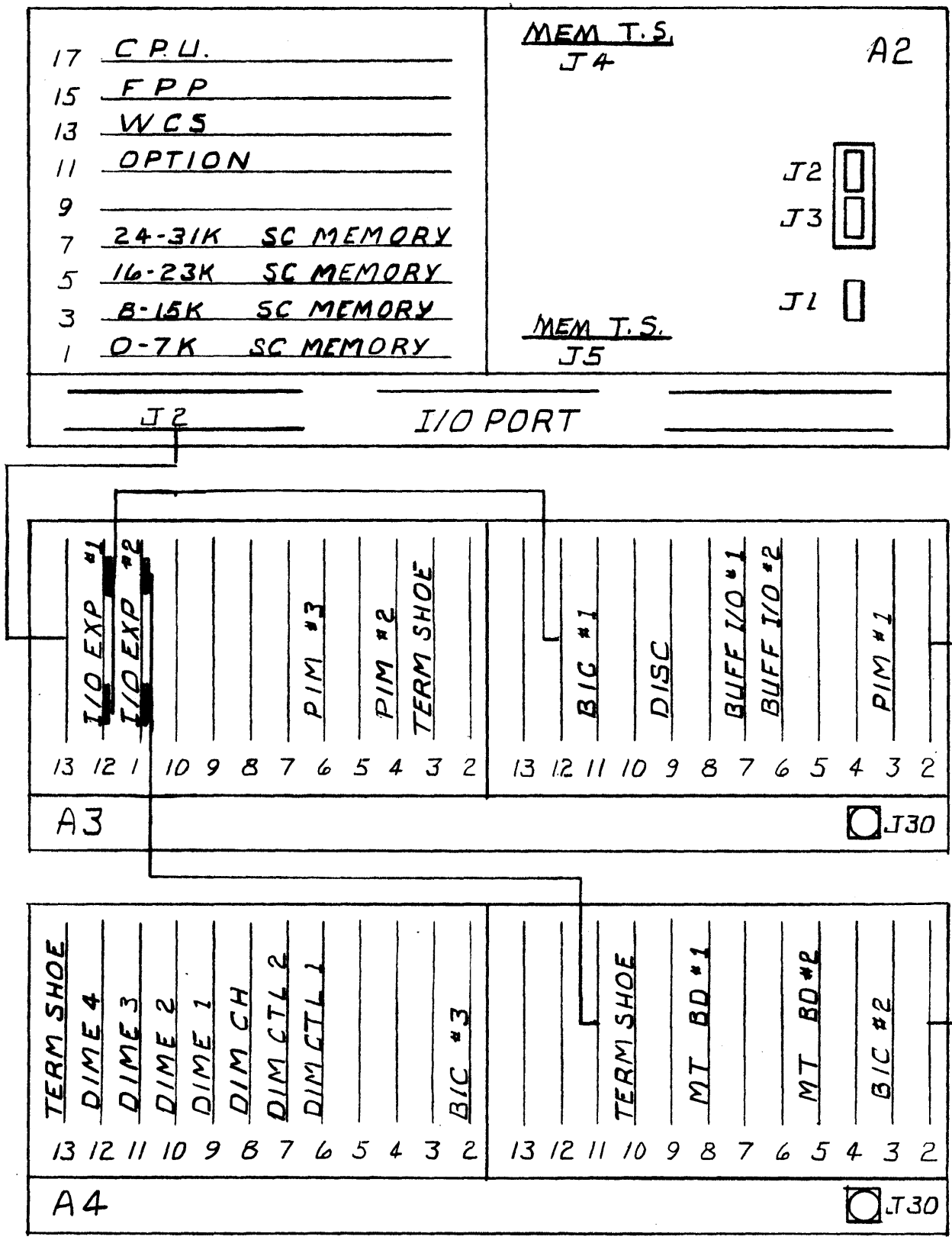
SH 3 OF 3

REV

96A0039-000B

BOARD LAYOUT



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96A0039-000B

96A0039-000B

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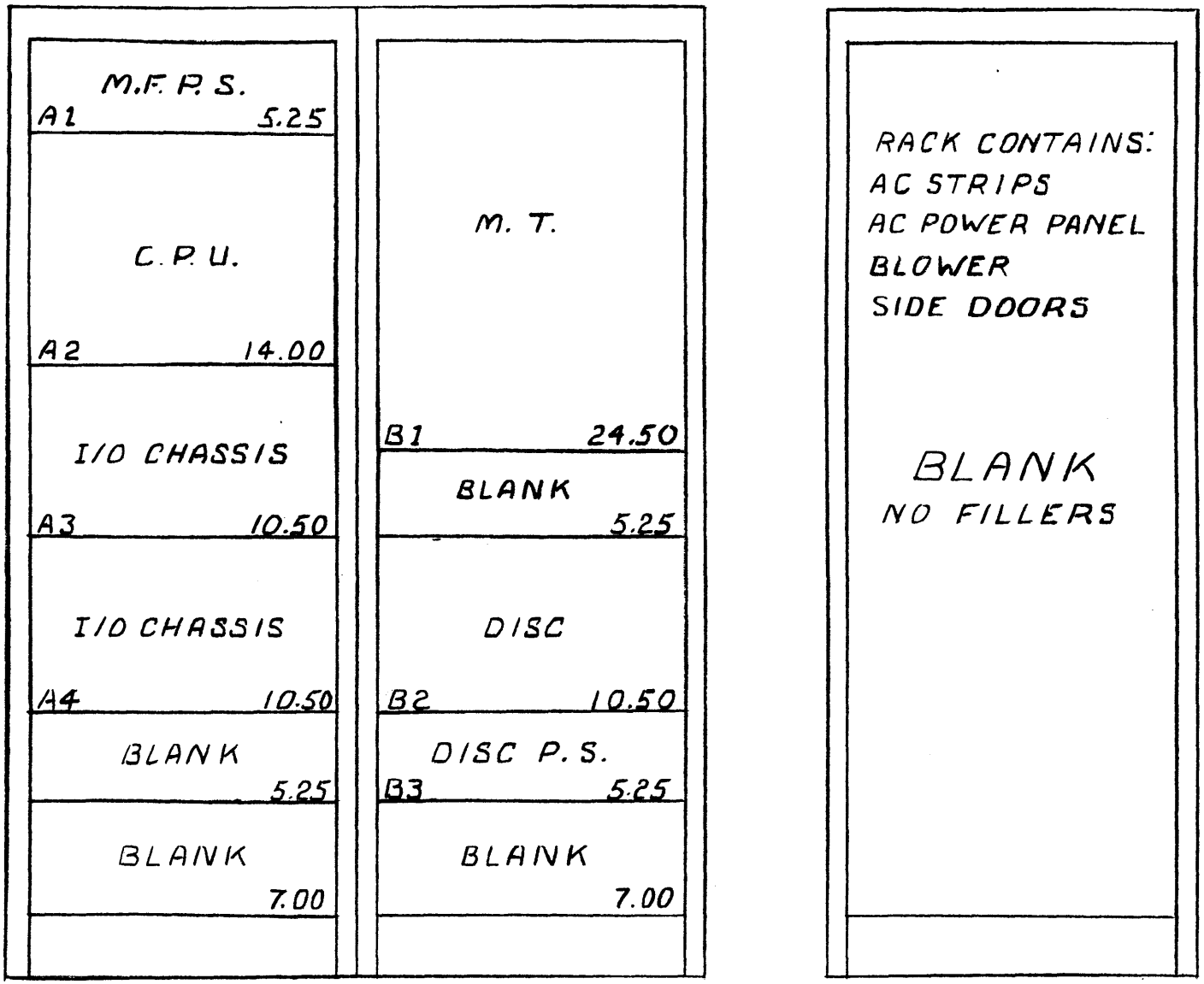
CODE IDENT NO. 21101

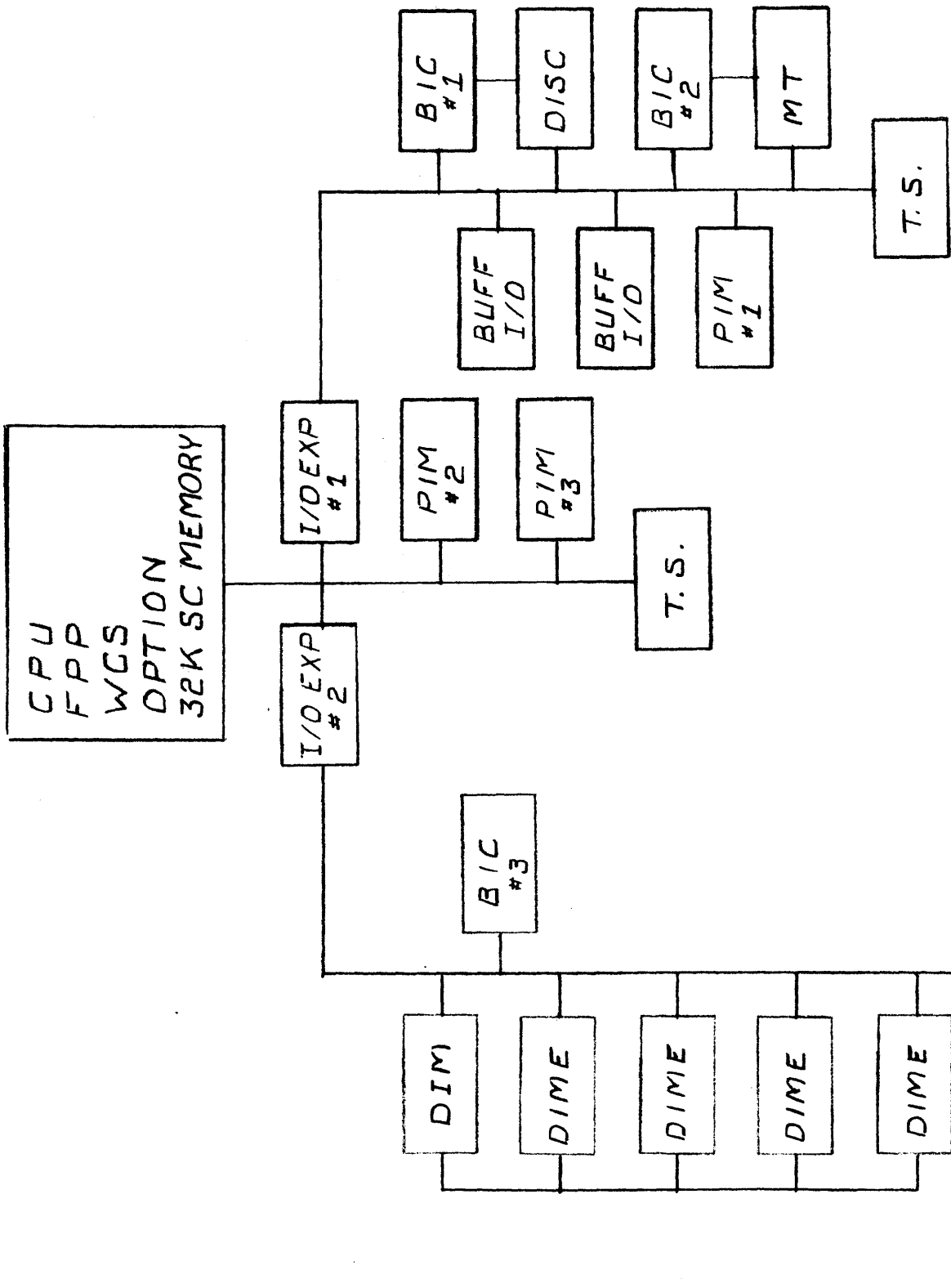
SH

OF

REV

CABINET LAYOUT





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SH OF REV

3.0 System Power Requirement

The system main power is 115 VAC, 60 HZ, 1 phase.

3.1 System Power

a. 1 each 30 amp circuits for cabinets -- mating connector is Hubbell 2610

b. 1 each 4 amp circuit for TTY

Mating connector for b is standard 3 wire "U" ground

4.0 Controller Board Slot Assignment

Refer to System Arrangment Drawing.

Chassis A2

Slot	17	Processor
	15	Floating Point
	13	WCS
	11	Option
	7	24-31K SC Memory
	5	16-23K SC Memory
	3	8-16K SC Memory
	1	0-7K SC Memory

Chassis A3 RH (Rear View)

Slot	2	I/O Cable
	3	PIM #1
	6	Buffered I/O #2
	7	Buffered I/O #1
	9	Disc
	11	BIC #1
	12	I/O Expander Cable #1

3-3 1473 360 55

4.0 Controller Board Slot Assignment (Continued)

Chassis A3 LH (Rear View)

Slot	3	Term Shoe
	4	PIM #2
	6	PIM #3
	11	I/O Expander #2
	12	I/O Expander #1
	13	I/O Cable

Chassis A4 RH (Rear View)

Slot	2	I/O Cable
	3	BIC #2
	5	M.T. Board #2
	8	M.T. Board #1
	10	Term Shoe
	11	I/O Expander Cable #2

Chassis A4 LH (Rear View)

Slot	2	BIC #3
	6	DIM Control #1
	7	DIM Control #2
	8	DIM Channel Card
	9	DIME 1
	10	DIME 2
	11	DIME 3
	12	DIME 4
	13	Term Shoe

5.0 PIM PRIORITY ASSIGNMENTS

PIM # 1

Device Address 40
Interrupt Address 100-117
Priority Levels:

1. Reserved
2. BIC #1
3. BIC #2
4. BIC #3
5. Reserved
6. Disc "0" Seek Complete
7. Disc "1" Seek Complete
8. MT Motion Complete

Switched See page 14 VA

PIM # 2

Device Address 41
Interrupt Address 120-137
Priority Levels:

1.
2.
3.
4.
5.
6.
7.
8.

PIM # 24

Device Address 43
Interrupt Address 160-177
Priority Levels:

1.
2.
3.
4.
5.
6.
7. TTY Read
8. TTY Write

4/14/75 JHS 100

BIC ASSIGNMENTS

BIC # 1

Device Address 20
Controller Assignments:

1. Disc DA = 16
2.
3.
4.
5.

BIC # 2

Device Address 24
Controller Assignments:

1. M.T. DA = 10
2.
3.
4.
5.

BIC # 3

Device Address 26
Controller Assignments:

1. DIM DA = 60
2.
3.
4.
5.

BIC

Device Address
Controller Assignments:

1.
2.
3.
4.
5.

BIC

Device Address
Controller Assignments:

1.
2.
3.
4.
5.

BIC

Device Address
Controller Assignments:

1.
2.
3.
4.
5.

6.0 System Wiring Requirements

6.1 System Priority

See Sections 6.1.1, 6.1.2, and 6.1.3.

SYSTEM PRIORITY ASSIGNMENTS

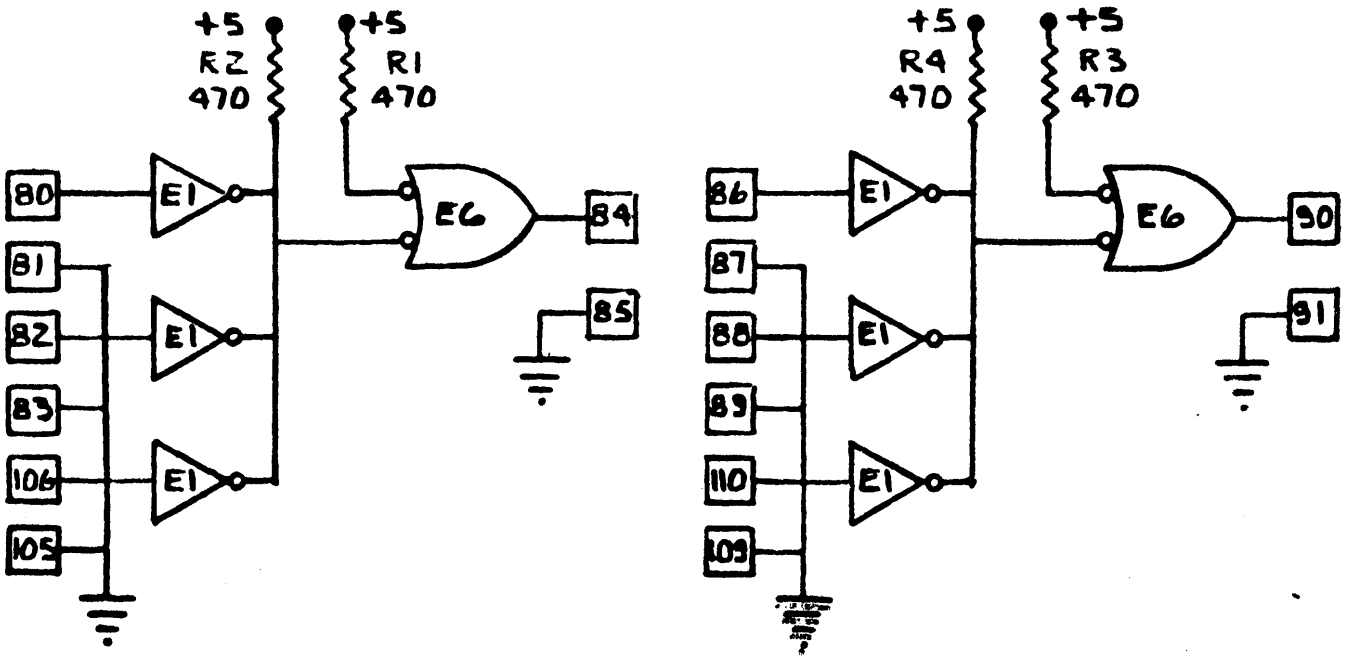
1.	Memory Protect	9.	PIM #2
2.	PFR	10.	PIM #3
3.	BIC #1	11.	Console
4.	BIC #2	12.	
5.	BIC #3	13.	
6.	RTC	14.	
7.	FPP	15.	
8.	PIM #1		

Priority Look Ahead Required? X Yes ____ No

The system priority network is long enough to incorporate "priority look ahead". The look ahead feature insures that the end of the priority line is made aware of an interrupt at the beginning of the line without having to wait for propagation delays through the priority network.

The priority look ahead is installed on the I/O Expander slot 12 LH rear view chassis A3.

The following components are on the I/O Exp. as indicated per 91C0435.



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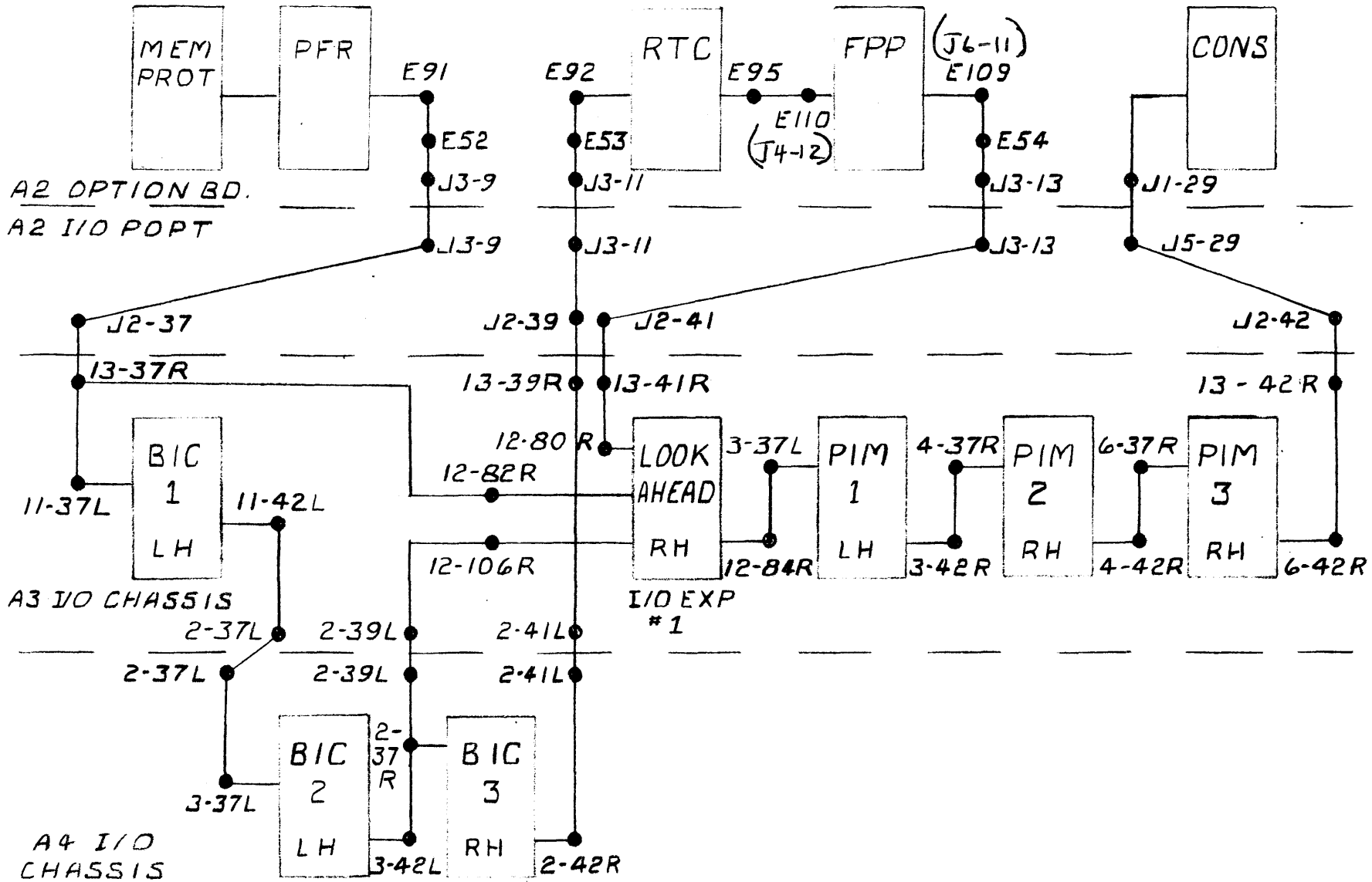
6.1.2 SYSTEM PRIORITY WIRING



6.1.3 Priority Wiring (Front View)

Chassis A2 (Option Board)

From	To
E91	E52
E92	E53
E95	E110
E109	E54

Note: If E 109 and E110 are not on Option Board, connect E95 to J4-12, and connect E54 to J6-11 (Refer to 01A1682).

Chassis A2 (I/O Port)

From	To
J2-37	J3-9
J2-39	J3-11
J2-41	J3-13
J2-42	J5-29

Chassis A3 (Use 30 AWG Twisted Pair)

Signal

From	To
13-37 RH	11-37 LH
13-38 RH	11-38 LH
13-37 RH	12-82 RH
13-39 RH	2-41 LH
13-40 RH	2-40 LH
13-41 RH	12-80 RH
13-42 RH	6-42 RH
13-40 RH	6-40 RH

Signal

From	To
12-84 RH	3-37 LH
12-85 RH	3-38 LH
12-106 RH	2-39 LH
12-105 RH	2-40 LH
3-42 LH	4-37 RH
3-40 LH	4-38 RH
4-42 RH	6-37 RH
11-42 LH	2-37 LH
11-40 LH	2-38 LH

Chassis A4 (Use 30 AWG Twisted Pair)

Signal (Green)		Ground (Black)	
From	To	From	To
2-37 LH	3-37 LH	2-34 LH	3-34 LH
2-39 LH	3-42 LH	2-36 LH	3-38 LH
2-39 LH	2-37 RH	2-36 LH	2-34 RH
2-41 LH	2-41 RH	2-38 LH	2-38 RH

6.2 Device Address Assignments

DA	DEVICE	DA	DEVICE
		040	PIM #1 IA = 100 - 117
01	TTY	041	PIM #2 IA = 120 - 137
02		042	
03		043	PIM #3 IA = 166 - 177
04		044	All PIM Enable/Disable
05		045	MP
06		046	
07		047	RTC
010	M.T.	050	
011		051	
012		052	
013		053	
014		054	
015		055	
016	DISC	056	
017		057	
020	4/17/75 VA	060	DIM (CC1)
021		061	DIM (CC2)
022	BIC #1	062	BUFF I/O #1
023		063	BUFF I/O #2
024	BIC #2	064	
025		065	
026	BIC #3	066	
027		067	
030		070	
031		071	
032		072	
033		073	
034		074	WCS
035		075	
036		076	
037		077	

6.2.1 Device Address Wiring

Chassis A3 LH (Front View)

PIM #1	Wiring
Slot 3	64-66
DA 40	67-69
IA 100-117	63-74
	70-72

Buff I/O #1	Wiring
Slot 7	65-66
DA = 62	67-69
	71-72
	74-75
	76-78

Buff I/O #2	Wiring
Slot 6	64-66
DA 63	67-69
	71-72
	74-75
	76-78

Disc	Wiring
Slot 9	65-66
DA 16	67-69
	70-72

BIC #1	Wiring
Slot 11	65-~~68~~ 69
DA ~~22,23~~ 20, 21	70-72
	~~59-69~~
	115-118

4/17/75 VA

Chassis A3 RH

PIM #2	Wiring
Slot 4	64-65
DA 41	67-69
IA 120-137	70-72

PIM #3	Wiring
Slot 6	65-64
DA 43	70-72
IA 160-177	63-106
	67-68

Chassis A4 LH

BIC #2	Wiring
Slot 3	65-69
DA 24,25	70-71
	59-72
	115-118

M.T.	Wiring
Slot 8	Hardwired on
DA 10	Board #1

Chassis A4 RH

BIC #3	Wiring
Slot 2	65-68
DA 26,27	70-71
	59-72
	69-72
	115-118

DIM (CC1)	Wiring	DIM (CC2)	Wiring
Slot 6	65-66	Slot 7	64-66
DA 60	68-69	DA 61	68-69
	71-72		71-72
			74-75
			76-78

6.3 PIM Interrupt Wiring (Use 30 AWG Twisted Pair)

PIM #1 DA = 40 IA = 100-117

Signal	From		To	Function
IL00 R	Spare			
IL01	A3 LH Slot 11- 75		A3 LH Slot 3-114	BIC #1 Complete
R	A3 LH Slot 11- 76		A3 LH Slot 3-113	
IL02	A4 LH Slot 3- 75		A4 LH Slot 2- 75	BIC #2 Complete
R	A4 LH Slot 3- 76		A4 LH Slot 2- 76	
IL02	A4 LH Slot 2- 75	(via cable)	A3 LH Slot 2- 75	
R	A4 LH Slot 2- 76	(via cable)	A3 LH Slot 2- 76	
IL02	A3 LH Slot 2- 75		A3 LH Slot 3-104	
R	A3 LH Slot 2- 76		A3 LH Slot 3-103	
IL03	A4 RH Slot 2- 75		A4 LH Slot 2- 77	BIC #3 Complete
R	A4 RH Slot 2- 76		A4 LH Slot 2- 78	
IL03	A4 LH Slot 2- 77	(via cable)	A3 LH Slot 2- 77	
R	A4 LH Slot 2- 78	(via cable)	A3 LH Slot 2- 78	
IL03	A3 LH Slot 2- 77		A3 LH Slot 3-110	
R	A3 LH Slot 2- 78		A3 LH Slot 3-109	
IL04 R	Spare			

Signal	From		To	Function
IL05	A3 LH Slot 9- 75		A3 LH Slot 3- 88	Disc "0" Seek Complete
R	A3 LH Slot 9- 76		A3 LH Slot 3- 87	
IL06	A3 LH Slot 9- 77		A3 LH Slot 3-112	Disc "1" Seek Complete
R	A3 LH Slot 9- 78		A3 LH Slot 3-111	
IL07	A4 LH Slot 8-103		A4 LH Slot 2- 63	MT Motion Complete
R	A4 LH Slot 8-104		A4 LH Slot 2- 64	
IL07	A4 LH Slot 2- 63	(via cable)	A3 LH Slot 2- 63	
R	A4 LH Slot 2- 64	(via cable)	A3 LH Slot 2- 64	
IL07	A3 LH Slot 2- 63		A3 LH Slot 3- 86	
R	A3 LH Slot 2- 64		A3 LH Slot 3- 85	

PIM #2 DA = 41 IA = 120-137

Signal	From	To	Function
IL00 thru IL07	Spares		

PIM #3 DA = 43 IA = 166-177

Signal	From	To	Function
IL00 thru IL05	Spares		

IL06	A2 (I/O Port) J3-3		A2 (I/O Port) J2-75	TTY Read
R	A2 (I/O Port) J3-4		A2 (I/O Port) J2-76	
IL06	A2 (I/O Port) J2-75	(via cable)	A3 RH Slot 13-75	
R	A2 (I/O Port) J2-76	(via cable)	A3 RH Slot 13-76	
IL06	A3 RH Slot 13-75		A3 LH Slot 4-112	
R	A3 RH Slot 13-76		A3 LH Slot 4-112	
IL07	A2 (I/O Port) J3-5		A2 (I/O Port) J2-77	TTY Write
R	A2 (I/O Port) J3-6		A2 (I/O Port) J2-78	
IL07	A2 (I/O Port) J2-77	(via cable)	A3 RH Slot 13-77	
R	A2 (I/O Port) J2-78	(via cable)	A3 RH Slot 13-78	
IL07	A3 RH Slot 13-77		A3 LH Slot 4-86	
R	A3 RH Slot 13-78		A3 LH Slot 4-85	

6.4 BIC Delete Wiring (Front View)

Delete the BIC wiring Chassis A4 LH, Slots 9 to 10 and slots 2 to 3, pins 49, 50, 52, 54, 56, 58 and 60.

6.5 Mag Tape Wiring

Install mag tape interboard wiring into Chassis A4 LH, Slots 5 to 8 per wire list #95W0271 contained in the Appendix, Section 9.0.

6.6 Digital Input Wiring

6.6.1 Card/Channel Selection Wiring

		A4 R/H Slots					
Signal	From	To	To	To	To	To	To
Blanking		7- 42	8- 42	9- 42	10- 42	11- 42	12- 42
Chan. Sel. A		7- 86	8- 86	9- 86	10- 86	11- 86	12- 86
" " B		7- 85	8- 85	9- 85	10- 85	11- 85	12- 85
" " C		7- 84	8- 84	9- 84	10- 84	11- 84	12- 84
" " D		7-102	8-102	9-102	10-102	11-102	12-102
" " E		7-104	8-104	9-104	10-104	11-104	12-104
" " F		7-105	8-105	9-105	10-105	11-105	12-105
" " G		7- 90	8- 90	9- 90	10- 90	11- 90	12- 90
Chan. Sel. H		7- 92	8- 92	9- 92	10- 92	11- 92	12- 92
Enable	6-83		8- 83	9- 83	10- 83	11- 83	12- 83
DTIS	6-89		8- 89	9- 89	10- 89	11- 89	12- 89
Busy	6-75	7-101	8-101	9-101	10-101	11-101	12-101

6.6.2 To enable Channel 1-4, jumper the following:
8-100, 8-95, 8-94, 8-93, 8-91, 8-73 and 8-77.

6.6.3 To enable Channel 5-8, jumper the following:
9-100, 9-95, 9-94, 9-93, 9-78 and 9-77.

6.6.4 To enable Channel 9-12, jumper the following:
10-100, 10-94, 10-93, 10-91, 10-78 and 10-77.

6.6.5 To enable Channel 13-16, jumper the following:
11-100, 11-94, 11-93, 11-78 and 11-77

6.6.6 To enable Channel 17-20, jumper the following:
12-100, 12-95, 12-93, 12-91, 12-78 and 12-77

6.7 Mainframe Wiring

6.7.1 Central Processor Wiring - refer to 01A1331

1. Install "Processor to Memory A " Jumpers.
2. Memory protect is installed, so jumper Pins F to F.
3. Clock source is WCS clock, jumper Pins J2 to J3
4. Memory Wraparound is for 32K ADD JUMPERS 22C TO 21B & A29 TO GND.

6.7.2 Control Console - refer to 01A1335

1. Control Disable - to disable all switches, install jumpers between Pins C and E.
2. ABL - RMD ADD jumpers between A TO A & B TO B

6.7.3 Option Board Wiring - refer to 01A1332

1. PFR — Option to be enabled, remove jumpers between E7 and E8, E9 and E10.
2. RTC — FRC=100μS, ADD jumper between E13 TO E18
   IIC =10KC, ADD jumper E13 TO E14
   Disable RTC interrupts on a J MARK instruction. Jumper between E11 and E12. (REMOVE TO RUN DIAGNOSTIC)
3. Memory Parity — DISable this option, INSTALL jumper clip between Pins E61 to E62.
   Interrupt Address= _____
   Jumper _____
   Parity Memory Bus _____
   Jumper _____
4. Memory Protect — Memory Bus Selection INSTALL jumpers for " A " bus selection. ENable this option, INSTALL jumper clips E98 to E99 and E100 and E101. Memory Map is _____ system.
5. Interrupt Clock — Setup for interrupt rate of 990. ADD jumpers between Pins E2 and E3, E4 and E5.
6. TTY — ENable TTY DELETE jumper E96 to E97. Setup TTY for BPS 110,2 Stop Bits. Install jumpers as follows:

   DELETE: E44 to E45

   ADD: E20 to E21, E24 to E25, E28 to E29, E30 to E31, E32 to E33, E36 to E37, E38 to E39, E40 to E41, E42 to E43, E107 to E108

7.	Memory Time Out Logic	Install JUMPERS BETWEEN B50 & B51, A25 & B49
8.	PMA	Data Transfer Mode = 620 compatible mode. ADD: Jumpers E73-E74, E75-E76, E77-E78, E79-E80. Hog Mode: NOT USED ~~will control Hog~~ Mode: DELETE jumper A27 - B27. PMA Memory Request - Jumper B25-C25 B Port NOT shared between PMA and CPU ADD E89-E90.
9.	PMA Address Bits 9-15	ADD Jumpers B11-C11 B13-C13 B15-C15 B17-C17 B19-C19 B21-C21 B23-C23

DISC — CHANGE CONTROLLER WIRING SO REMOVEABLE PACK IS "0", FIXED IS "1".

REMOVE B8-9 — B8-13

ADD B8-9 — B8-12

4/15/75

VARIAN SERVICE REP

6.7.4 WCS Wiring - refer to 01A1444

1. Device Address - 74, 75. Install jumper clips between E2 and E3, E4 and E5.
2. Page Address - 1. Install jumper clips between E9 and E10, E11 and E12.
3. Fine Clock Output - Install jumper clip between E34 and E35.
4. Memory Request Disable for Micro Step Mode - Install jumper clip between E36 and E37.
5. Page Select Signal - Install jumper clips between E15 and E16.
6. Module 1 Enable - Install jumper clip between E21 and E22.
7. Decoder RAM NOT Present ADD jumper clip between E23 and E24.
8. Control Store Data Driver NO jumper NOT enable interlock control.
9. BCS Entry Table - Setup for 32 words NO jumper clips between E31 and E32, E28 and E29, E25 and E26.
10. Memory Port Selection - Install jumper clips for " A " Port select.
11. Memory DONE YDNM - Install jumper clip between B3-C3
12. Address 15 MAY 15 - Install jumper clip between B1-C1
13. Memory Lockout Control ADD jumper C4-B4
14. Address 15 Control - Install jumper clip between E17 and E18.
15. WCAEN - True is Decoder ROM is Selected - Install jumper clip between E61 and E62.
16. WXCSEN - True if CCS ROM is Selected - Install jumper clip between E27 and E30.

6.7.5 MOS Memory - Refer to 01A1323

For bank address selection wiring, refer to attached memory jumper configuration sheets (see Section 9.0)

Memory Bank #1	=	0- 7K	Slot #1	Mainframe Chassis A2
Memory Bank #2	=	8-15K	Slot #3	
Memory Bank #3	=	16-23K	Slot #5	
Memory Bank #4	=	24-31K	Slot #7	

6.7.6 Floating Point Processor

Time Out Enable	-	Jumper B4C-10 to B5B-13
+5V Control	-	Jumper P1A-6 to J7-1
Add Wire List 95W1100	-	Jumper B4C

6.8 Miscellaneous Special Wiring

1. Delete all voltage wiring to Slot 2 lh (Front View). Chassis A4, Slot 13 RH (Front View) Chassis A3
2. Delete all I/O wiring Slot 13 LH to Slot 2 RH, Chassis A3 Pins 1-60.
3. Add Data Guard Wiring:

A2 (I/O Port) J3-7		A2 (I/O Port) J2-115
A2 (I/O Port) J2-115	(via cable)	A3 RH Slot 13-115
A3 RH Slot 13-115		A3 LH Slot 9-113
A3 LH Slot 9-113		A3 RH Slot 3-115

4. Disable BIMES

BIC 1 - Jumper A3 LH Slot 11-93 to Pin 73
BIC 2 - Jumper A4 LH Slot 3-93 to Pin 73
BIC 3 - Jumper A4 RH Slot 2-93 to Pin 73

7.0 SPECIAL SYSTEM INFORMATION

1. Install Data Save on Power Supply
2. Setup buffered I/O as follows:

Pulse Width 10 usec R10 = 3.9K C37 - .001 MFD

Bit Configuration 16 Bits

8.0 CABLE IDENTIFICATION

CABLE DESIGN.	FROM	TO	PART NUMBER	CABLE LENGTH	FUNCTION
X1	A1 J1	A2 J1	53P0658	48"	Fan Power
X2	A1 J4	A2 J2	53P0659	48"	DC Power
X3	A1 J3	A2 J3	53P0673	48"	DC Power
X4	A1 J1	A6 PS	53P0685	60"	AC Sequence
X5	A6 PS	A7 PS	53P0696	60"	AC Sequence
X6	A5 Captive	A3 J30	53P0686	30"	I/O Exp. Power
X7	A6 Captive	A4 J30	53P0686	30"	I/O Exp. Power
X8	A2 P2 (CPU)	A2 P2 (Flt Pt) A2 P2 (WCS)	53P0674-004		WCS
X9	A2 P3 (DCA)	A2 P3 (Opt)	53P0675-007	MODIFIED	Aux I/O
X10	A2 P3 (CPU)	A2 P3 (Flt Pt) A2 P3 (WCS)	53P0674-004	MOD	WCS
X11	A2 P4 (Flt Pt)	A2 P4 (Opt)	53P0674-006	MOD.	Processor
X12	A2 P5 (DCA)	A2 P5 (Opt) A2 P5 (CPU)	53P0676-003	MOD.	I/O
		A2 P5 (WCS) A2 P5 (Flt Pt) A2 P1 (CONS)			
X13	A2 P6 (CPU)	A2 P6 (Flt Pt) A2 P6 (WCS) A2 P6 (Opt)	53P0674-006		WCS
X14	A2 J2 (DCA)	A3 RH Slot 13	53P0715	24"	I/O
X15	A2 P8 (Opt)	C1 (TTY)	53P0777	240"	TTY
X16	A7 P/S	A2 (WCS)	53P0703	48"	FPP Power
X17	A8 P/S	A2 (Flt Pt)	53P0703	48"	WCS Power
X18	A3 RH Slot 12	A3 LH Slot 12	53P0665	60"	I/O Expander Cable
X19	A3 RH Slot 11	A4 LH Slot 11	53P0665	60"	I/O Expander Cable

8.0 CABLE IDENTIFICATION

CABLE DESIGN.	FROM	TO	PART NUMBER	CABLE LENGTH	FUNCTION
X20	A3 LH Slot 9 P1 and P2	Disc B2	53P0739	180"	Disc
X21	A3 LH Slot 2	A4 LH Slot 2	53P0547	12"	I/O
X22	A4 LH Slot 8 P1, Slot 5 P2	B1 MT (Mstr)	53P0425	240"	Mag Tape
X23	A2 P4 (Proc.)	A 2P 4A(Flt Pt)	53P0816-007		FPP

9.0 APPENDIX

1. Board Layout
2. Cabinet Layout
3. Semiconductor Memory Configuration Sheets (4)
4. PIM Pin Assignment Sheet
5. W/L No. 95W0271 - REV. "A"

mMc - DT
Attachments