

Additional routing

varian data machines / a varian subsidiary
2722 michelson drive / irvine / california / 92664 / (714) 833-2400



Salesman # 2491

D. Bryant

R. Douglas

M. Drees (2)

M. Peralta

Note: Please forward along with other documentation.

system memo ^{v73} JM-106 I-s.c.

Q.C.

Sales Admin. (2)

C. Stark (2)

Job File

customer: Sperry Systems Management

sales order: 64489

charge number: 64489

date: February 27, 1975

from: J. Merina

Please reference Systems Arrangement Drawing No. 93D0836X.

V-73

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TEST DATA SHEET
V73 FINAL ACCEPTANCE

S. O. # 64489

Processor# _____

Date _____

Reference Test Procedure 98A0923

Para.	Test Description	Required Parameter	Actual	Stamp
4.0	Voltage checks V73 chassis and I/O expansion chassis	+5 VDC $\pm$ 1%	T19	
		+5 M $\pm$ 1%	T19	
		+20.6 VDC $\pm$ 1%	T19	
		+20 VDC $\pm$ 1%	T19	
		-12 VDC $\pm$ 1%	T19	
		+22.5 VDC $\pm$ 1%	T19	
		+12 VDC $\pm$ 1%	T19	
		-5 VDC $\pm$ 1%	T19	
		LFRTC+ Check	T19	
		SPFA- Check	T19	
		SRST- Check	T19	
5.0	Console Tests	No failures	T19	
6.1	Basic CPU Operation			
-6.5	Tests	No failures	T19	
6.6	Machine Cycle Check	655 ns $\pm$ 5	T19	
		325 ns $\pm$ 5		
6.7	Inst. Test Programs	No failures	T19	
	Memo Test Programs	No Failures		
	TTY Test Program	No Failures	T19	

Test Machines

21101

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**TEST DATA SHEET
V73 FINAL ACCEPTANCE**

Reference Test Procedure 98A0923

Para.	Test Description	Required Parameter	Actual	Stamp
7.0	I/O Test	No failures	T ₃₉	
8.0	Standard DMA Test	No failures	T ₃₉	
9.0	High Speed DMA Test	No failures		
10.0	Basic Interrupt Test	No failures	T ₁₂₅	
11.0	Memory Wrap Around	No failures	T ₁₂₅	
12.0	Power Fail/Restart	No failures	T ₁₉	
13.0	Real Time Clock	No failures	T ₃₉	
14.0	Memory Protect	No failures	T ₁₂₅	
15.0	Priority Memory Access	No failures	T ₃₉	
1	Processor/Option Margins	Inst. 1 4.75 VDC	T ₁₂₅	
		Inst. 2 5.25 VDC	T ₁₂₅	
16.2	Memory Margins	Step 1	T ₁₃	
		Step 2	T ₁₃	
		Step 3	T ₁₃	
		Step 4	T ₁₃	
		Step 5	T ₁₃	
		Step 6	T ₁₃	
		Step 7	T ₁₃	
		Step 8	T ₁₃	
17.0	High Temperature Burn-In	No failures 72 hrs.		



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V73 ADD-ON OPTIONS

Final

Retest
After Q. C.

1.	EXPANSION CHASSIS (<u>2EA</u>)	T39	
2.	POWER SUPPLY (<u>2EA</u>)	T39	
3.	PIM <u>2EA</u>		
4.	BIC <u>2EA</u>	T39	
5.	READER CONTROLLER		
6.	BUFFERED I/O <u>1EA</u>	T39	
7.	I/O EXPANDER <u>2EA</u>	T39	
8.	9 TRACK M. T. U. AND CONTROLLERS <u>M+S</u>	T125	
9.	7 TRACK M. T. U. AND CONTROLLERS		
10.	REMEX READER		
11.	FACIT PUNCH		
12.	ASR 33	T39	
13.	ASR 35		
14.	KSR 35		
15.	MODEM ()		
16.	RELAY I/O		
17.	CARD READER AND CONTROLLER		
18.	DISC AND CONTROLLER (<u>7510</u>)	T13	
19.	VRC DRUM AND CONTROLLER		
20.	UASC <u>1EA</u>	T125	
21.	LINE PRINTER AND CONTROLLER (<u>E2200</u>)	T125	
22.	DAC		


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SH 2 OF 3 REV

V73 ADD-ON ORDERS

Final

Retest
After Q. C.

23. ADC	-----		
24. DIGITAL PLOTTER AND CONTROLLER	-----		
25. CARD PUNCH AND CONTROLLER	-----		
26. MEMORY MODULE (³² 32 K MOS)	-----	T13	
27. ABL (DISC)	-----	T13	
28. DCM	-----		
29. VORTEX ^{9+K 32K}	-----	T13	
30. VTAM	-----		
31. PROCESSOR	-----		
32. OPTION BOARD ()	-----		
33. DISPLAY PANEL ()	-----		
34. MEMORY EXPANSION CHASSIS	-----		
35. WCS + PS		T125	
36. BTC		T39	
37. FPP + PS		T13	
38. DATA SALES PS		T13	
39. 244n Burr			
40.			
41.			

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SH 3 OF 3

REV

DOCUMENTATION RECORD

CUSTOMER SPERRY SYSTEM MANAGEMENT JOB ORDER NO. 64487
MODEL NO. V70
SYS. SERIAL NO. 620

UNIT	DOCUMENTATION NO	REV	S/N	DESCRIPTION
	98A0879	--	-----	Parts List
	98A0887	--	-----	Micro Word Flowcharts
	49A0195	--	-----	Control Store Code Listing
	81L1709-001	--	-----	Central Control Store Listing
	(44P0614) 91B0378	<u>BJ</u>	<u>720</u>	Processor Bd.
	(44P0619) 91B0401	<u>BP</u>	<u>364</u>	Option Bd.
	(44P0613) 91C0377	AC	1631	Core Memory
	(44P0613) 91B0377			Core Memory
	(44P0613) 91B0377			Core Memory
	(44P0645) 91B0406	<u>P</u>	<u>522</u>	Display Bd.
	(44P0625) 95D0940	<u>A</u>	<u>1412</u>	Term Shoe
	(44P0625) 95D0940	<u>A</u>	<u>1374</u>	Term Shoe
	(44P0664) 95D0970	<u>A</u>	<u>1862</u>	Term Shoe
	(44P0664) 95D0970	<u>A</u>	<u>073</u>	Term Shoe
	(44P0608) 95D0911			Back Plane
	(44P0609) 95D0912	<u>L</u>	<u>500</u>	Back Plane
	(01P1320) 95E0923	<u>D</u>	<u>773</u>	Power Supply
	(44P0610) 95C0918	<u>E</u>	<u>750</u>	Reg. Bd.
	(44P0611) 91D0388	<u>H</u>	<u>1047</u>	Reg. Bd.
	(44P0679) 91D0451	<u>D</u>	<u>959</u>	Reg. Bd.
	(44P0615) 95D0932	<u>G</u>	<u>847</u>	Heat Sink Bd.
	(44P0617) 95E0941	<u>M</u>	<u>1065</u>	Power Supply Bd.
	(44P0623) 91D0387	<u>L</u>	<u>501</u>	Power Fail Bd.
	83P0035	<u>S</u>	<u>602</u>	Exp. Power Supply
	(44P0618) 91C0397	<u>AE</u>	<u>208</u>	Semi Cond. Memory
	(44P0618) 91C0397	<u>AE</u>	<u>207</u>	Semi Cond. Memory
	(44P0618) 91C0397	<u>AE</u>	<u>137</u>	Semi Cond. Memory

PREPARED BY Walter Gollis DATE 3-15-75 NOTE:

V70
MANUAL LISTING

V73 HANDBOOK	9809906-010
PROCESSOR	9809906-023
* CORE MEMORY	9809906-031
* SEMI CONDUCTOR MEMORY	9809906-040
OPTION BD.	9809906-051
POWER SUPPLY	9809906-063
TEST PROGRAMS	9809952-061
MICROPROGRAMMING	9809906-073
BIC	9809902-115
PIM	9809902-426
BUFFERED I/O	9809902-625
VORTEX INST.	9809952-250
VORTEX REF.	9809952-103
WCS	9809906-082
WCS POWER SUPPLY	9809910-000
FLOATING POINT PROC.	9809906-110

NOTE: * Manual shipped only for
the type memory used.

TEST REPORT

Test Date 3-28-75

P.O. No. _____

Pkg Slip No. 64489

Quantity _____

Account No. _____

Part or Material V-73

Manufacturer VDM

Ser. No. _____

TEST REQUIREMENTS:

Test Category: Rec. ☐ Mfg. ☒ Other _____

Perf. Spec.: Enclosed ☐ Reference _____

TEST RESULTS:

ACCEPT ☒ REJECT ☐

Did ☒ Did Not ☐ Meet Manufacturers or applicable purchase specs.

Comments: V73 w/ 32K SC memory, 14" CHASSIS, POWER SUPPLY, CONSOLE, DMA
NA PFR, CTC, HM/D, TTY, MEM PROT, DATA SAVE, DISC ABL,
WCS & PWR SUPPLY, F.P.P. & P.S., I/O CHASSIS, w/ P.S., I/O EXPANDER &
CABLES, I/O CHASSIS, w/ P.S. & CABLES, 1 EA. B.T.C., 2 EA P.I.M., 2 EA.BIC,
1 EA. VASC, 1 EA. TTY, ABR 33, 1 EA. EXT. BD., 1 EA L.P., 1 EA M.T. MASTER,
1 EA M.T. SLAVE, 1 EA. DISC, 1 BUFF. I/O CONTROLLER, 1 EA DISC ABL,
1 EA. CABINETS, -3BAY, VORTEX (MT9), MAINTAIN II

Disposition: _____

CONDUCTED BY:

1. Signed James H Robinson
Date 3-28-75 Stamp (113)

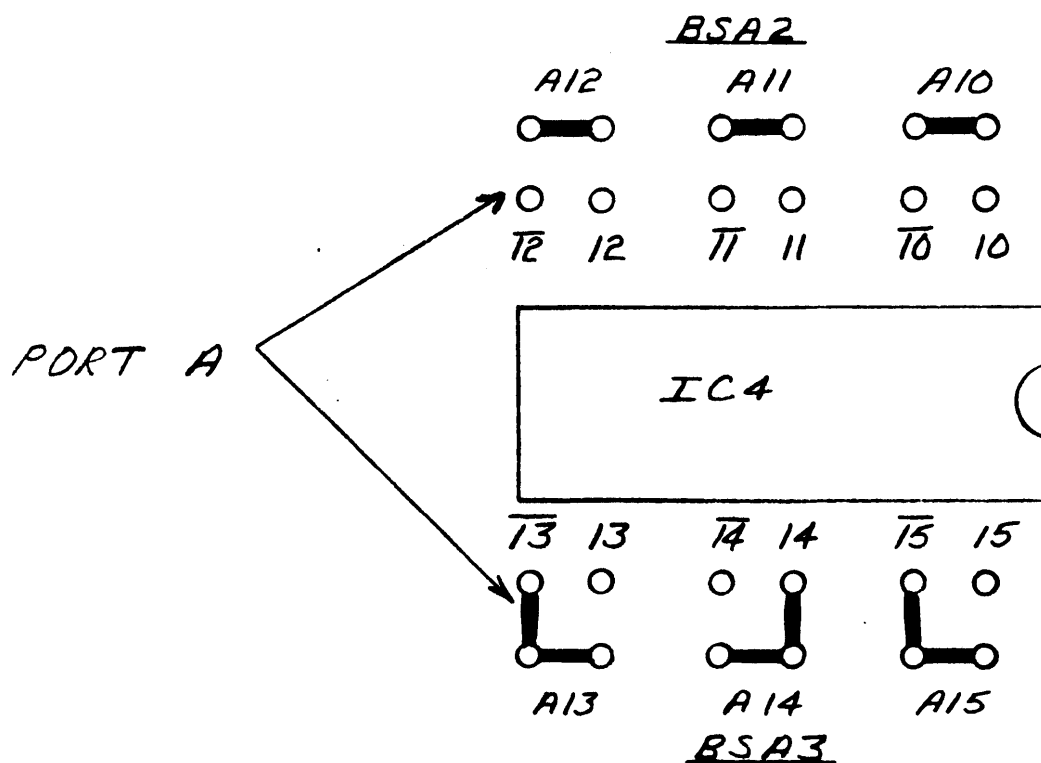
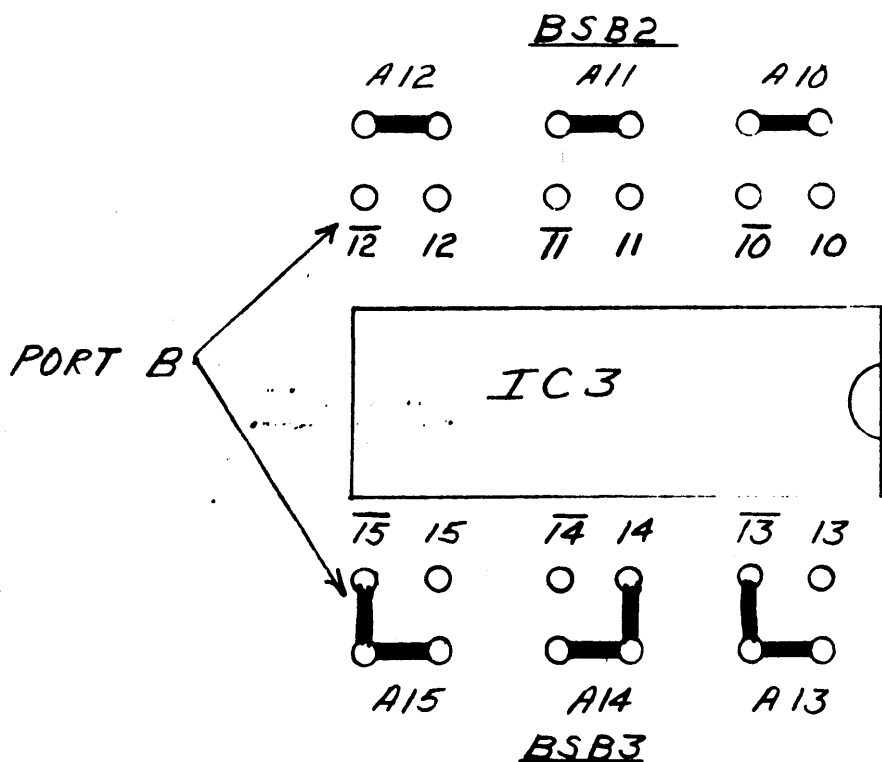
2. Signed _____
ite _____ Stamp _____

3. Signed _____
Date _____ Stamp _____

APPROVAL:

A. Signed F. L. Terenguy
Title V-70's Systems Lead
Date 28 March 75 Stamp (158)

B. Signed _____
Title _____
Date _____ Stamp _____



Memory Bank Size	8K
Memory Bank Address	16-23K



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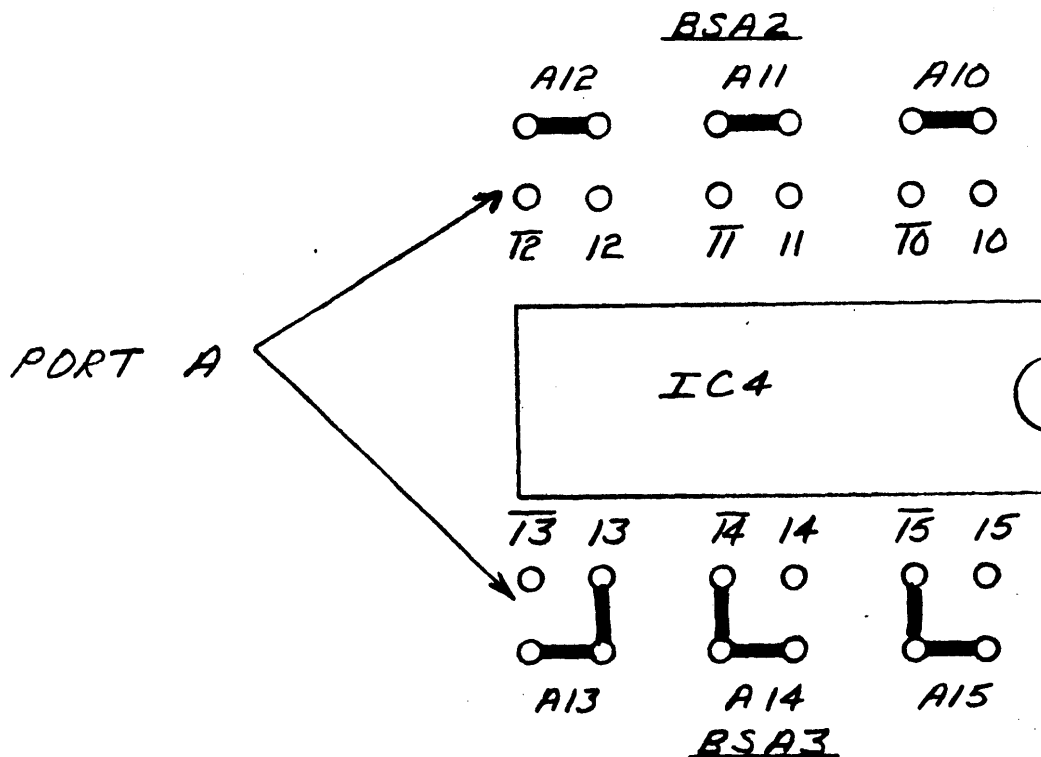
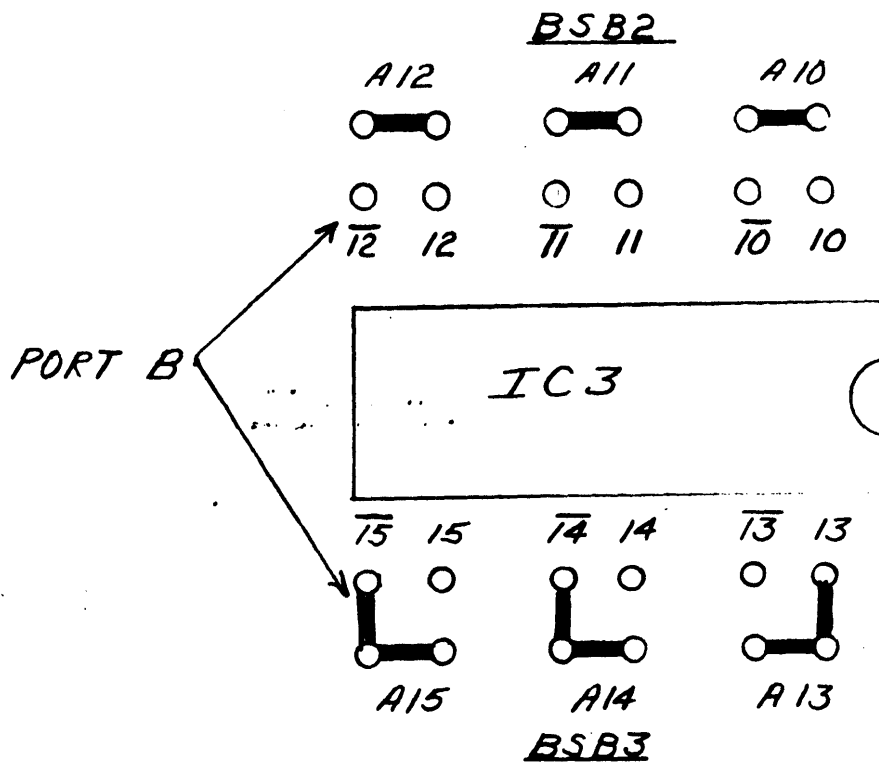
CODE
IDENT NO.
21101

Semi-Conductor
Memory Configuration

SH

OF

REV



Memory Bank Size BK
 Memory Bank Address B+5K



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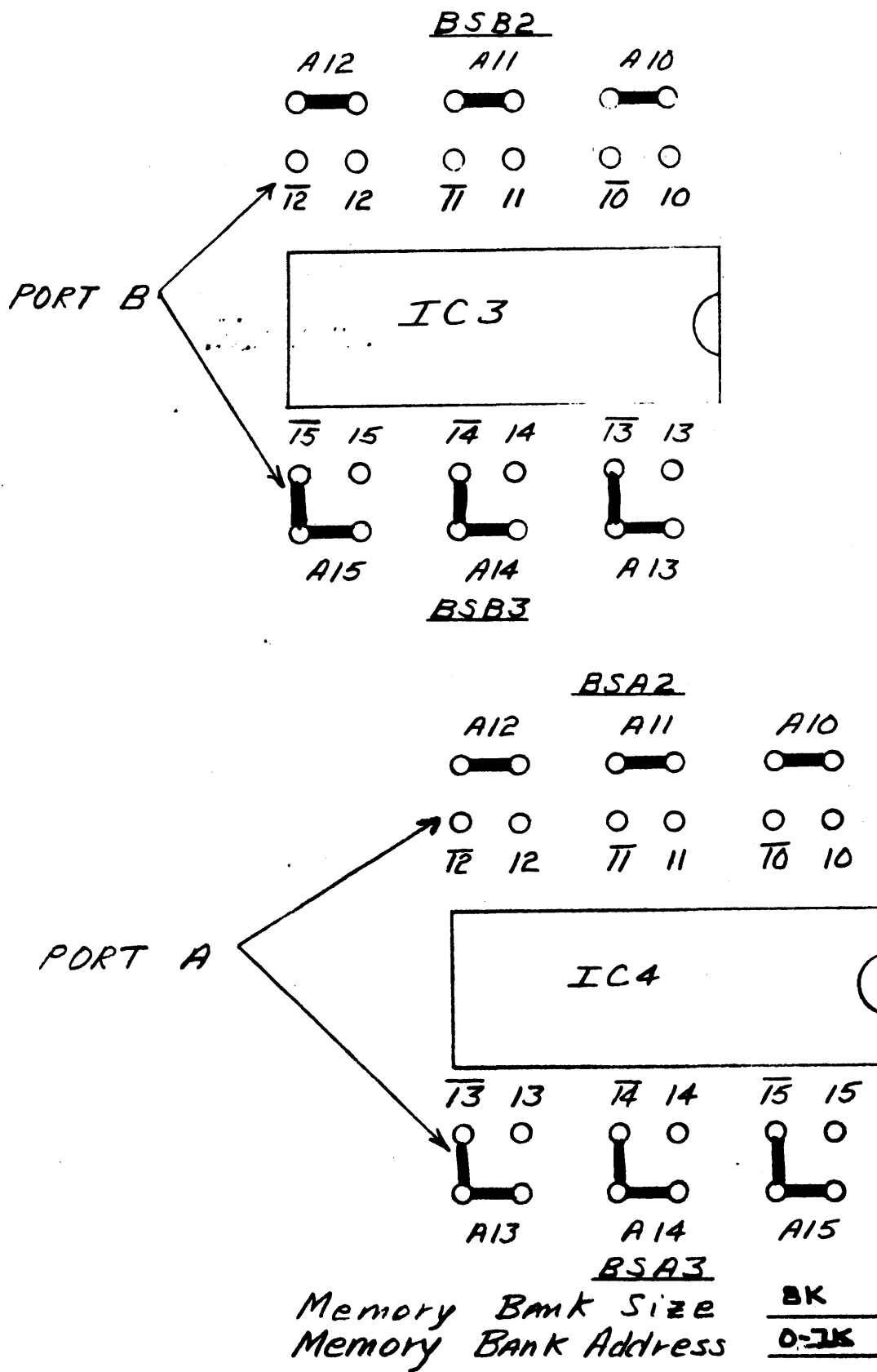
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Memory Configuration

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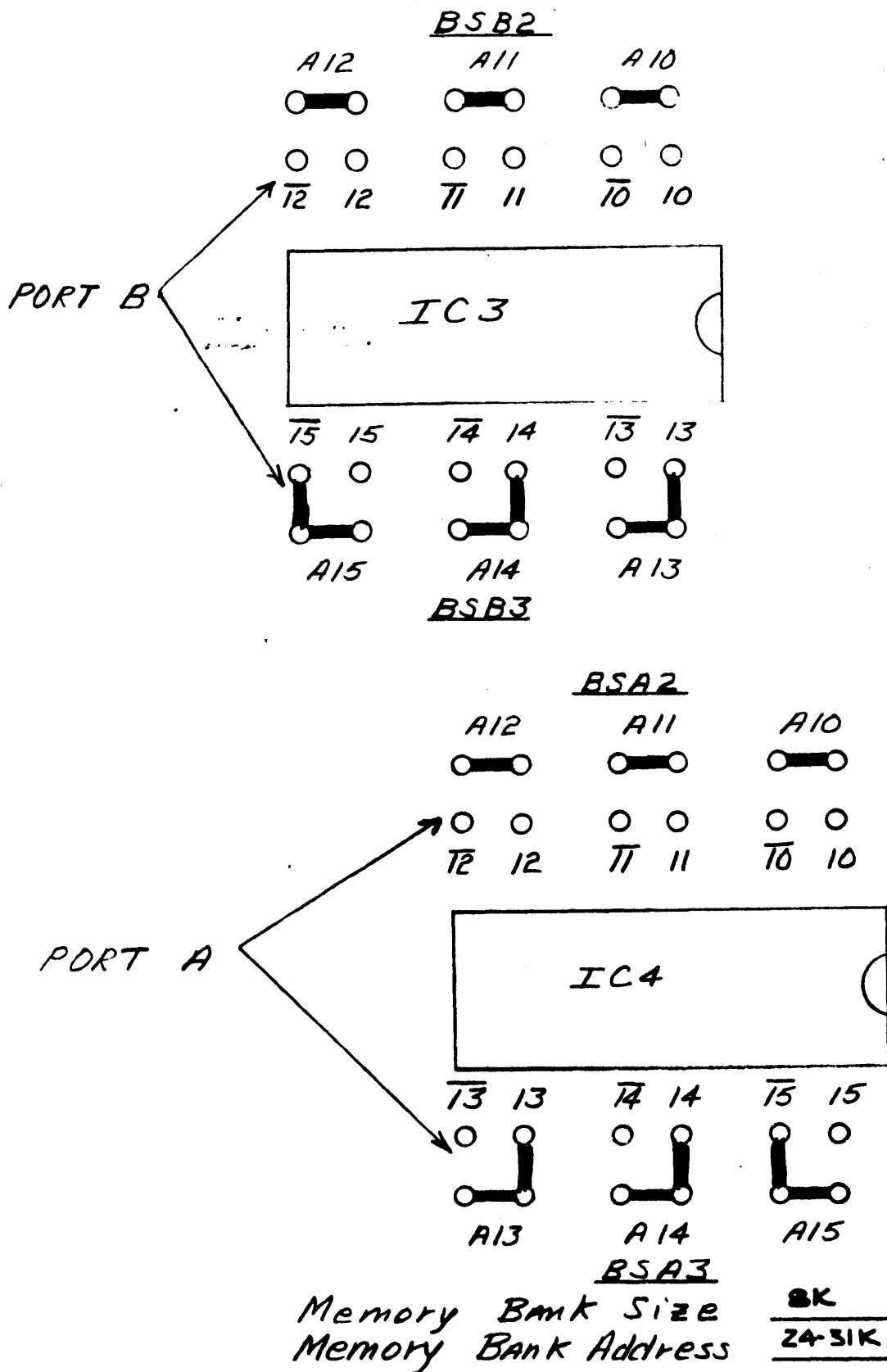
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Memory Configuration

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Semi-Conductor
Memory Configuration

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ASSEMBLY LAYOUT

MAINTENANCE PEG		
A1	5.00	
CPU		
A2	14.0	
I/O CHASSIS		
A3	10.5	
I/O CHASSIS		
A4	10.5	
BLANK		
	5.25	
BLANK		
	7.0	
MAG TAPE SLAVE		
B1	24.5	
BLANK		
	10.5	
BLANK		
	10.5	
BLANK		
	7.0	
MAG TAPE MASTER		
B2	24.5	
BLANK		
	10.5	
BLANK		
	10.5	
BLANK		
	7.0	



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CODE
IDENT NO.
101101

CARPET LAYOUT

MAINFRAME 25		
A1	5.25	
CPU		
A2	14.0	
I/O CHASSIS		
A3	10.5	
I/O CHASSIS		
A4	10.5	
BLANK		
	5.25	
BLANK		
	7.0	
MAG TAPE SLAVE		
B1	24.5	
BLANK		
	10.5	
BLANK		
	10.5	
BLANK		
	7.0	
MAG TAPE MASTER		
B2	24.5	
BLANK		
	10.5	
BLANK		
	10.5	
BLANK		
	7.0	



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SH OF REV

The PIM (1 to 8 AC External Interrupts) are brought into PIM Board via Front Pins or via J1 or J2 "EDGE" connectors on the later model PIM Board.

FUNCTION	FRONT PINS (Both Models)	J1 or J2
IL00 -	108	3
R	107	4
IL01 -	114	13
R	113	14
IL02 -	104	9
R	103	10
IL03 -	110	15
R	109	16
IL04 -	102	11
R	101	12
IL05 -	88	5
R	87	6
IL06 -	112	1
R	111	2
IL07 -	86	7
R	85	8

NOTE: IL00 - is highest priority; IL07 - is lowest priority.

Input Levels	=	+5V	=	OFF	=	No Ini.
	=	0V	=	ON	=	Int.

I/O jumpers for PIM Interrupt Addresses:

100-117 = 74-63, 80 & 106 = Open
140-157 = 106-74, 74-63, 80 = Open

120-137 = 74, 80 & 106 = Open
160-177 = 106-63, 74 & 80 = Open



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PIM EXTERNAL INTERRUPTS

SH

OF

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SIGNAL NAME	FROM	TO	REMARKS
X063	A-063	B-063	Use 30 AWG
X064	A-064	B-064	Single Strand
X065	A-065	B-065	White Wire
X066	A-066	B-066	
X067	A-067	B-067	
X068	A-068	B-068	
X069	A-069	B-069	
X070	A-070	B-070	
X071	A-071	B-071	
X072	A-072	B-072	
X073	A-073	B-073	
X074	A-074	B-074	
X075	A-075	B-075	
X076	A-076	B-076	
X077	A-077	B-077	
X078	A-078	B-078	
X079	A-079	B-079	
X080	A-080	B-080	
X081	A-081	B-081	
X082	A-082	B-082	
X083	A-083	B-083	
X084	A-084	B-084	
X085	A-085	B-085	
X086	A-086	B-086	
X087	A-087	B-087	
X088	A-088	B-088	
X089	A-089	B-089	
X090	A-090	B-090	
X091	A-091	B-091	
X092	A-092	B-092	
X093	A-093	B-093	
X094	A-094	B-094	
X095	A-095	B-095	
X096	A-096	B-096	

WIRE LIST No. 001

By

CODE
IDENT

WL 95W0271

REV
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SHEET

1

DATE

DWG NO. 95W1131

REVISIONS

REV	EN	CHG CODE	DESCRIPTION	DR	APPD
A	83455	—	PRODUCTION RELEASE	<i>gm</i>	<i>gk</i>

NEXT ASSEMBLY
01P1564



varian data machines / a varian subsidiary
2722 michelson drive / irvine / california / 92664

DR	<i>Manca</i>	<i>3-14-74</i>
CHK	<i>W. Brown</i>	<i>5-21-74</i>
DSGN		
ENGR	<i>A Jung</i>	<i>11/14/74</i>
APPD	<i>W. Brown</i>	<i>1/3/75</i>
APPD		

CODE
IDENT NO. **21101**

THIS DOCUMENT MAY CONTAIN
PROPRIETARY INFORMATION AND
SUCH INFORMATION MAY NOT BE
DISCLOSED TO OTHERS FOR ANY
PURPOSE OR USED TO PRODUCE
THE ARTICLE OR SUBJECT, WITH-
OUT PERMISSION FROM VDM.

TITLE
WIRE LIST, SPECIAL BACKPLANE
CDS DISC WITH PMA/BTC
CONFIGURATION

SIZE A	DWG NO. 95W1131	REV A
------------------	--------------------	-----------------

SHEET 1 OF 4

WIRING INSTRUCTIONS

1. Refer to systems memo for slot locations.

Card slot J "X" = CDS Disc Cont. Board #1 $\Delta = X$

Card slot J "Y" = CDS Disc Cont. Board #2 $\Delta = Y$

Card slot J "Z" = PMA/BTC $\Delta = Z$

2. Whenever possible, slot locations should be located at the end of the I/O bus to simplify deletions.
3. Delete the following wires: (Ref. Figure 1 below)

At card slot J "X" - Delete all wires from the following pins:
3, 5, 7, 9, 22, 23, 24, 25, 32 thru 42, 45, 46, 47, 51 and 63.

Note: If breaking into a daisy-chain string, be sure to wire across to assure continuity of the I/O bus.

4. Add wires per wire list on pages 3 and 4.

I/O SLOTS

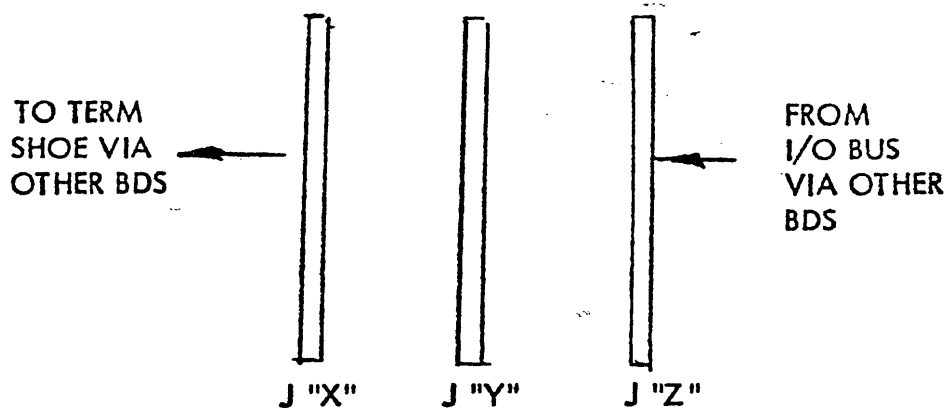


Figure 1

EXP CHASSIS FRONT VIEW



5. Backplane wiring where (X) and (Y) are specified by Systems Memo.



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95W1131

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SIGNAL NAME	FROM	TO	REMARKS
C00-	J "Z"-80	J "X"-32	
C01-	▲ -81	▲ -33	
C02-	-82	-34	
C03-	-83	-35	
C04-	-84	-36	
C05-	-85	-37	
C06-	-86	-38	
C07-	-87	-39	
C08-	-88	-40	DATA BUS
C09-	-89	-41	
C10-	-90	-42	
C11-	-91	-45	
C12-	-92	-46	
C13-	-93	-47	
C14-	-94	-51	
C15-	-95	-63	
CREQ-	-97	-03	
CGO-	-99	-07	
CREAD-	-102	-09	
CACK-	-104	-05	
BCDX-P	-106	-25	CONTROL SIGNALS
CDCX-P	-108	-22	
DCEX-P	-110	-23	
DESX-P	▼ -112	▼ -24	
RESHOG-	J "Z"-114	J "X"-74	
CYSEL +	JX-77	JY-77	△ 5
CSEL+	JX-95	JY-95	
WIRE LIST No. 001		By	CODE IDENT
 varian data machines a varian subsidiary newport beach/california		21101	WL 95W1131
			REV A
		SHEET 3 OF 4	DATE

SIGNAL NAME	FROM	TO	REMARKS
DDR+	J "X" -73	J "Y" -73	
SCCR-	▲ -75	▲ -75	
RCCI-	-76	-76	
WDAT-	-78	-78	
COMSEL+	-81	-81	
DIFSEL+	-82	-82	
HSEL+	-83	-83	
DA00+	-84	-84	
DA01+	-85	-85	
DA02+	-86	-86	
DA03+	-87	-87	
DA04+	-88	-88	
DA05+	-89	-89	
DA06+	-90	-90	
DA07+	-91	-91	
BCDXE1-	-92	-92	
CO-	-93	-93	
DO-	-94	-94	
BRDY-	-96	-96	
SRBR-	-97	-97	
BPSP-	-98	-98	
SSREN-	-99	-99	
SR15+	-101	-101	
CC15+	-102	-102	
SDET+	-103	-103	
PRCC-	-104	-104	
PRLD-	-105	-105	
SYBP-	-106	-106	
BRCLK+	-107	-107	
EX+	-109	-109	
OL+	-110	-110	
OCYL-	-111	-111	
SKER+	▼ -112	▼ -112	
RDONLY-	J "X" -108	J "Y" -108	

WIRE LIST No. 001		by	CODE IDENT	WL 95W1131	REV A
 varian data machines a varian subsidiary newport beach / california			21101	DISC INTERBOARD WIRING	
			SHEET 4 OF 4		DATE

NOTES: UNLESS OTHERWISE SPECIFIED

1. Reference Drawings

01P1682 Floating Point Processor Option Parts List

01A1682 Floating Point Processor Option

2. This wire list converts standard configuration F.P.P. for use with WCS
(Port A).



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95W1100

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REV

DEVICE ADDRESS WIRING TABLE A

Last Digit	Wire Pin 72 To	Wire Pin 69 To	Wire Pin 66 To
0	71	68	65
1	71	68	64
2	71	67	65
3	71	67	64
4	70	68	65
5	70	68	64
6	70	67	65
7	70	67	64

DEVICE ADDRESS WIRING TABLE B

Device	Address	Wire
BIC	20-21	65-69, 70-72, 115-118 (+5V), 73-93 (SPECIAL PULLUP)
BIC	22-23	65-68, 59-69, 70-72, 115-118 (+5V)
BIC	24-25	65-69, 59-72, 70-71, 115-118 (+5V)
BIC	26-27	65-68, 59-69, 69-72, 70-71, 115-118 (+5V)
L.P. Cont.	35	87-78, 82-76, 84-77, 64-66, 68-69, 70-72
PTR 150 CPS	37	64-66, 67-69, 70-72, 82-76, 84-77, 87-78
PIM	40 (IA 100-117)	64-66, 67-69, 70-72, 63-74
PIM	41 (IA 120-137)	63-66, 64-65, 67-69, 70-72 ←
PIM	42 (IA 140-157)	63-69, 64-66, 67-68, 70-72, 63-74, 74-106 ←
PIM	43 (IA 160-177)	63-66, 66-69, 64-65, 67-68, 70-72, 63-106 ←
MUX, DIM	70	65-66, 68-69, 71-72, 73-75, 76-78
Relay I/O	70	65-66, 68-69, 71-72,

DIM-124 ONLY

PIM Device Address Wiring - Two Types

Type 1

<u>Device Address</u>	<u>Wiring</u>
40	64-66, 67-69, 70-72
41	63-66, 64-65, 67-69, 70-72
42	63-69, 64-66, 67-68, 70-72
43	63-66, 66-69, 64-65, 67-68, 70-72

Type 2 Board Assembly # 44D0683
DM 398

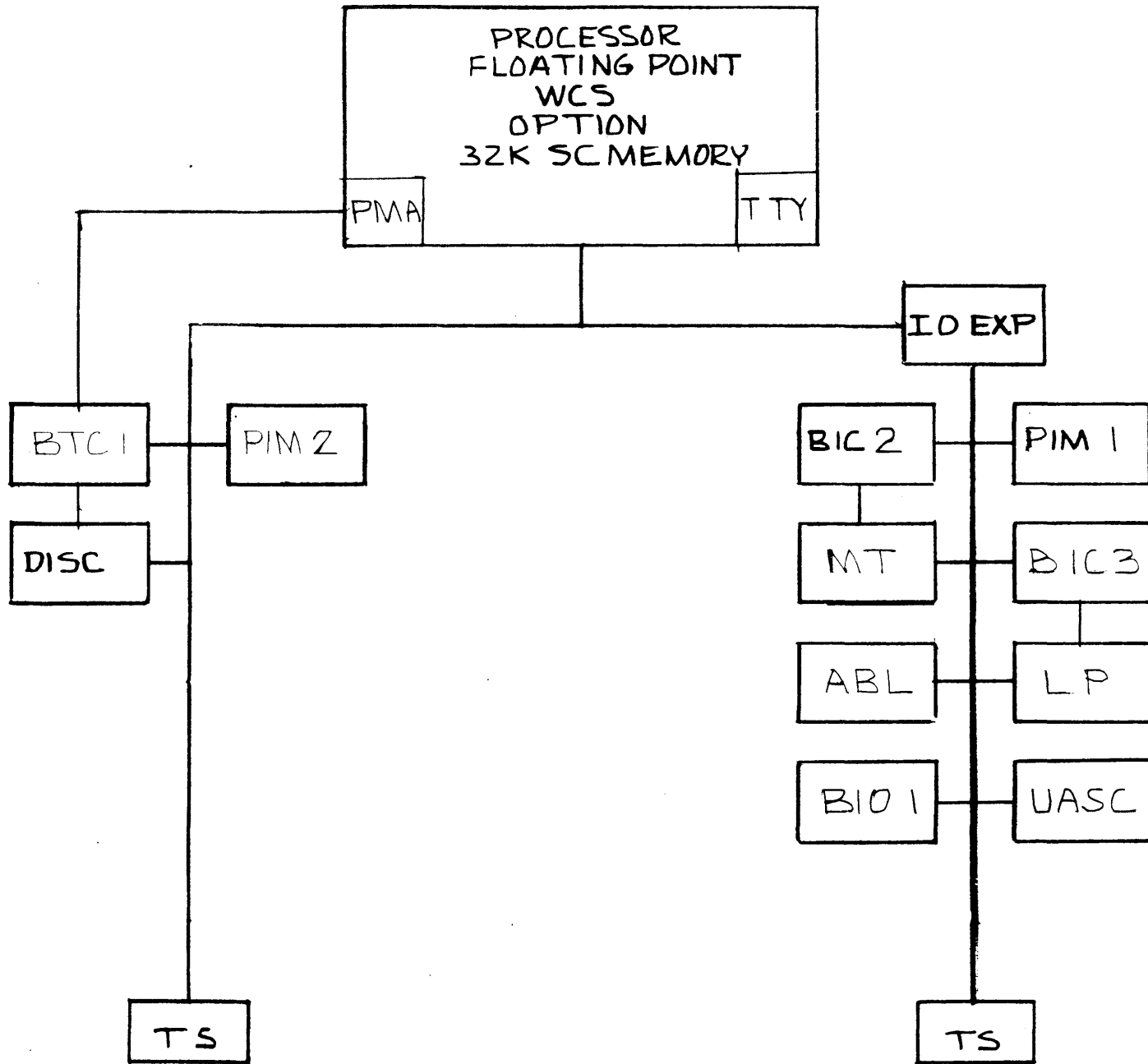
<u>Device Address</u>	<u>Wiring</u>
40	64-66, 67-69, 70-72
41	64-65, 67-69, 70-72
42	64-66, 67-68, 70-72
43	64-65, 67-68, 70-72

1.0 EQUIPMENT SUMMARY

This is 32K SC Memory V-73 Computer System.

- V-73, 14" Chassis, Power Supply, Console, DMA, PMA, PFR, RTC, HM/D, TTY, Memory Protect (E3520B)
- 32K SC Memory with Data Save (73-2500 - 73-3200)
- Disc ABL (73-3004)
- WCS and Power Supply (73-4004 + 73-4090)
- Floating Point Processor and Power Supply (73-3400 + 73-4090)
- 1 each - I/O Chassis (73-9004) includes Power Supply, I/O Expander and Cables
- 1 each - I/O Chassis (73-9005) includes Power Supply and Cables
- 1 each - BTC (73-3100)
- 2 each - PIM (73-3101)
- 2 each - BIC (73-3102)
- 1 each - UASC (70-5601)
- 1 each - TTY ASR33 (70-6100)
- 1 each - Extender Board (70-9951)
- 1 each - LP (E-2200)
- 1 each - MT Master (70-7102)
- 1 each - MT Slave (70-7103)
- 1 each - Disc (70-7510)
- 1 each - Buffered I/O Controller (70-8301)
- 1 each - Disc ABL (73-3004)
- 1 each - Cabinets - 3 Bay (70-9202)
- VORTEX (MT9) (70-9500)
- MAINTAIN II (70-9570)

2.0 SYSTEM BLOCK DIAGRAM



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3.0 SYSTEM POWER REQUIREMENT

The system main power is 115VAC, 60HZ, 1 phase.

3.1 System Power

- a. 1 each - 30 Amp circuits for cabinets - mating connector is Hubbell 2610
- b. 1 each - 4 Amp circuit for TTY
- c. 1 each - 7 Amp circuit for Line Printer

Mating connector for "b" and "c" is standard 3-wire "U" ground.

3.2 Disc Power

- a. 1 each - 20 Amp, 208VAC, 3-phase circuit for disc; mating connector is Hubbell 3520.

4.0 CONTROLLER BOARD SLOT ASSIGNMENT

Refer to System Arrangement Drawing No. 93D0836X.

Chassis A2

Slot

17	Processor
15	Floating Point
13	WCS
11	Option
7	24-31K SC Memory
5	16-23K SC Memory
3	8-16K SC Memory
1	0-7 K SC Memory

Chassis A3 RH

Slot

13	I/O Cable
12	I/O Expander
9	BTC #1
6	Disc Board #2
3	Disc Board #1

Chassis A3 LHSlot

13	PIM #2
12	Term Shoe
11	I/O Expander
10	BIC #2
8	ABL
5	BIO #1
4	UASC
3	PIM #1
2	I/O Cable

Chassis A4 LHSlot

2	I/O Cable
5	M.T. Board #2
8	M.T. Board #1

Chassis A4 RHSlot

2	BIC #3
4	LP
13	Term Shoe

5.0 PIM / BIC ASSIGNMENTS

5.1 PIM PRIORITY ASSIGNMENTS

PIM # 1

Device Address 40
Interrupt Address 100-117
Priority Levels:

PIM

Device Address _____
Interrupt Address _____
Priority Levels:

PIM # 2

Device Address 43
Interrupt Address 160-177
Priority Levels:

- 100
102
104
106
108
110
112
114
0. BTC #1 D
 1. RESERVED D
 2. BIC #2 D
 3. BIC #3 D
 4. RESERVED D
 5. DISC SEEK COMP →
 6. SPARE D
 7. MT MOTION COMP

0. _____
1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____

0. _____
1. _____
2. _____
3. _____
4. LIASC REAL RT
5. VASC WRITE RT
6. TTY REAL RT
7. TTY WRITE RT

5.2 BIC ASSIGNMENTS

BIC # 1

Device Address 20, 21
Controller Assignments:

1. DISC DA=15
2. _____
3. _____
4. _____
5. _____

BIC

Device Address _____
Controller Assignments:

1. _____
2. _____
3. _____
4. _____
5. _____

BIC # 2

Device Address 24, 25
Controller Assignments:

1. MT DA=10
2. _____
3. _____
4. _____
5. _____

BIC # 3

Device Address 26, 27
Controller Assignments:

1. LP DA=35
2. _____
3. _____
4. _____
5. _____

BIC

Device Address _____
Controller Assignments:

1. _____
2. _____
3. _____
4. _____
5. _____

BIC

Device Address _____
Controller Assignments:

1. _____
2. _____
3. _____
4. _____
5. _____

6.0 System Wiring Requirements

6.1 System Priority

See Sections 6.1.1, 6.1.2, and 6.1.3.

6.1.1

SYSTEM PRIORITY ASSIGNMENTS

1. MEM PROT
2. PFR
3. BIC #2
4. BIC #3
5. RTC
6. FPP
7. PIM #1
8. PIM #2

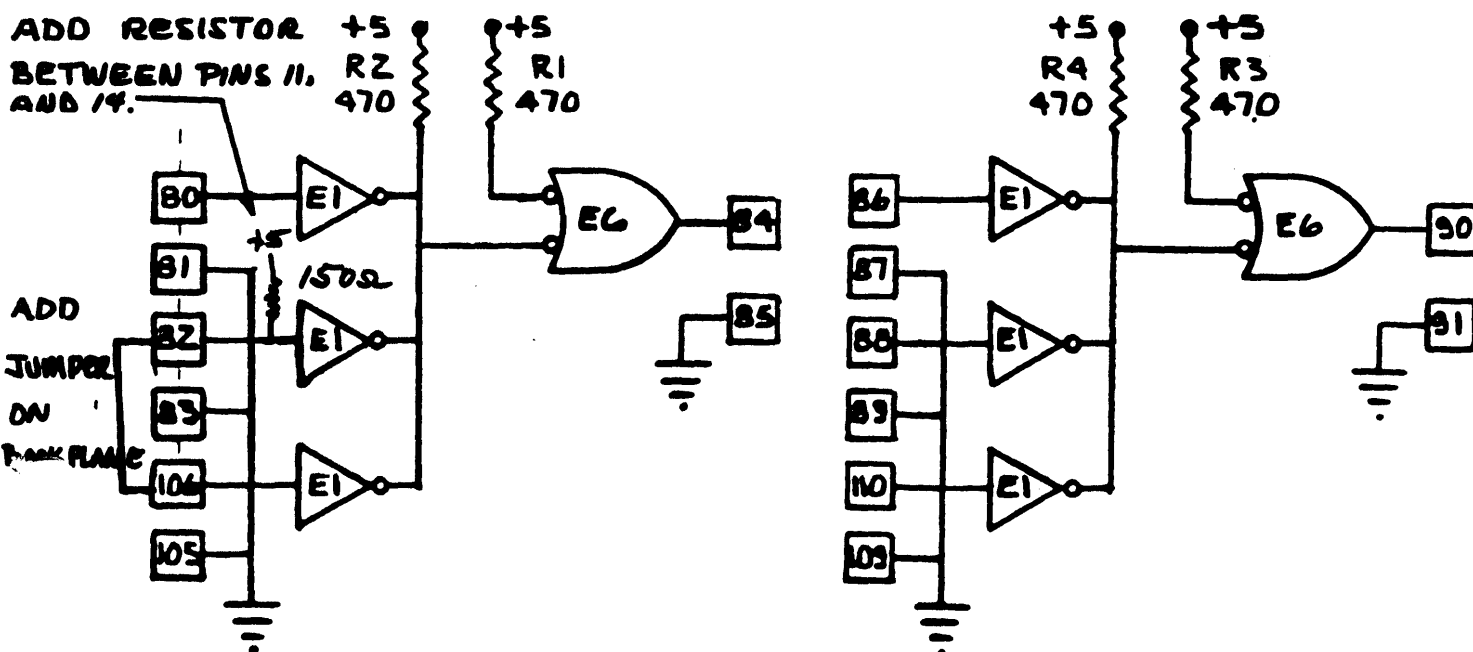
9. ABL
10. CONSOLE
11. _____
12. _____
13. _____
14. _____
15. _____

Priority Look Ahead Required? X Yes No

The system priority network is long enough to incorporate "priority look ahead". The look ahead feature insures that the end of the priority line is made aware of an interrupt at the beginning of the line without having to wait for propagation delays through the priority network.

The priority look ahead is installed on the I/O Expander slot 12 (R/H) view chassis A3.

The following components are on the I/O Exp. as indicated per 91C0435.



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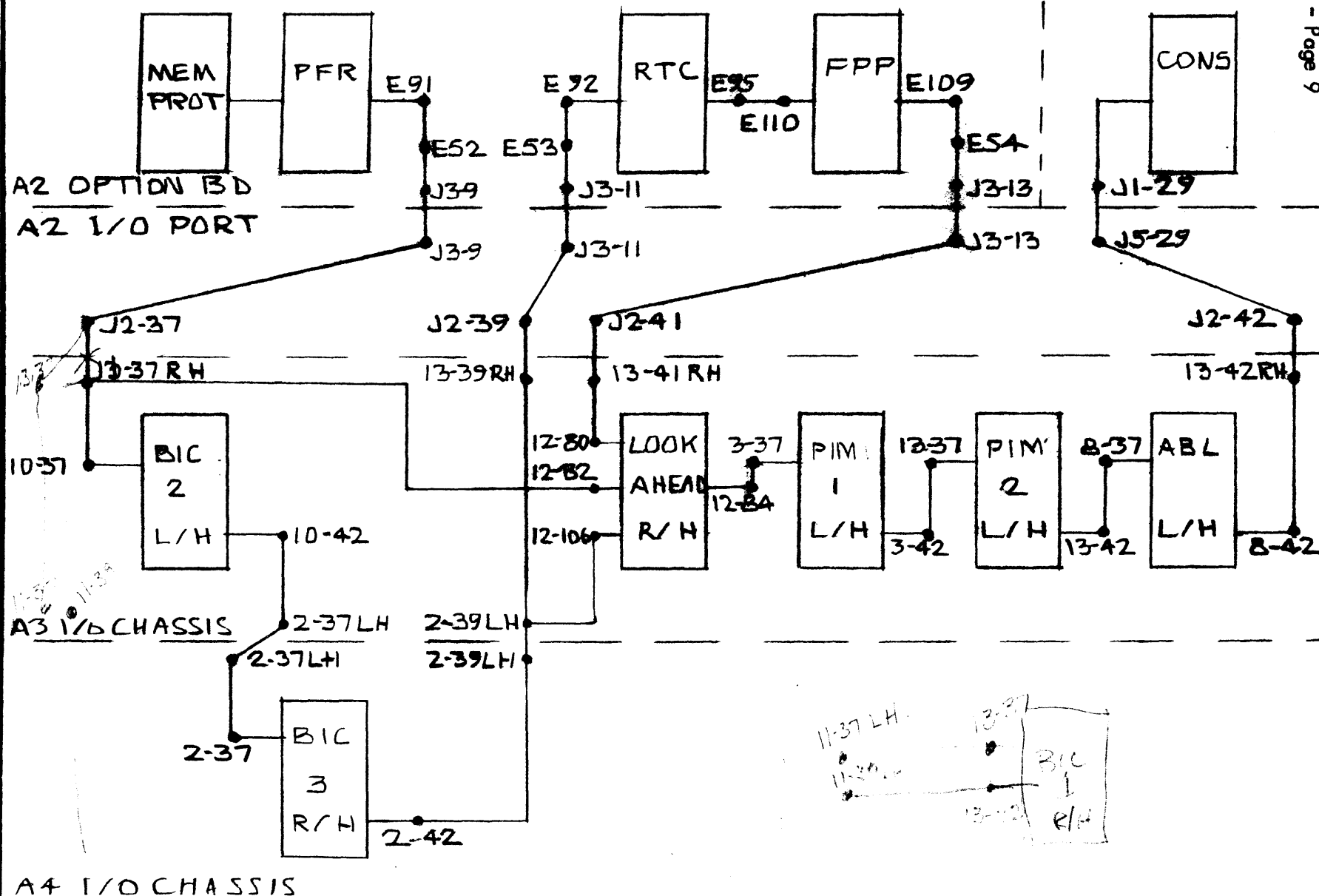
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6.1.2 SYSTEM PRIORITY WIRING DIAGRAM

SO 64489 - Page 9



6.1.3 Priority WiringChassis A2 (Option Board)

<u>From</u>	<u>To</u>
E91	E52
E92	E53
E95	E110
E109	E54

NOTE: If E-109 and E-110 are not on Option Board, connect E95 to J4-12, and connect E54 to J6-11 (refer to 01A1682).

Chassis A2 (I/O Port)

<u>From</u>	<u>To</u>
J2-37	J3-9
J2-39	J3-11
J2-41	J3-13
J2-42	J5-29

Chassis A3 (Use 30 AWG Twisted Pair)

<u>Signal</u>		<u>Signal</u>	
<u>From</u>	<u>To</u>	<u>From</u>	<u>To</u>
13-37 RH	 10-37 LH	12-84 RH	 3-37 LH
13-38 RH	 10-38 LH	12-85 RH	 3-38 LH
13-37 RH	12-82 RH	12-106 RH	 2-39 LH
13-39 RH	 2-39 LH	12-105 RH	 2-40 LH
13-40 RH	 2-40 LH	3-42 LH	 13-37 LH
13-41 RH	12-80 RH	3-40 LH	 13-38 LH
13-42 RH	 8-42 LH	13-42 LH	 8-37 LH
13-40 RH	 8-40 LH	13-40 LH	 8-38 LH
		10-42 LH	 2-37 LH
		10-40 LH	 2-38 LH

Chassis A4 (Use 30 AWG Twisted Pair)

<u>From</u>	<u>To</u>
2-37 LH	 2-37 RH
2-34 LH	 2-34 RH
2-39 LH	 2-42 RH
2-36 LH	 2-36 RH

6.2 Device Address Assignments

DA	DEVICE	DA	DEVICE
		040	PIM #1 (IA=100-117)
01	TTY	041	
02	UASC 1	042	
03	UASC 2	043	PIM #2 (IA=160-177)
04	UASC 3	044	All PIM Enable/Disable
05	UASC 4	045	MP
06	UASC 5	046	
07	UASC 6	047	RTC
010	MT	050	
011		051	
012		052	
013		053	
014		054	
015	DISC	055	
016	ABL (DISC)	056	
017		057	
020	BTC #1	060	
021	BTC #1	061	
022		062	
023		063	
024	BIC #2	064	BIO #1
025	BIC #2	065	
026	BIC #3	066	
027	BIC #3	067	
030		070	
031		071	
032		072	
033		073	
034		074	WCS
035	LP 1	075	WCS
036	LP 2	076	
037	HIGH SPEED	077	CONSOLE

6.2.1 Device Address WiringChassis A3 LH

<u>PIM #1</u>	<u>Wiring</u>
Slot 3	64-66
DA 40	67-69
IA 100-117	63-74 70-72

<u>UASC</u>	<u>Wiring</u>
Slot 4	76-83, 66-65
DA = 02	77-85, 69-67
	78-87, 71-72

<u>Buff I/O #1</u>	<u>Wiring</u>
Slot 5	65-66
DA = 64	68-69 71-72

<u>Disc ABL</u>	<u>Wiring</u>
Slot 8	65-66
DA = 16	67-69 70-72

<u>PIM #2</u>	<u>Wiring</u>
Slot 13	65-64
DA 43	70-72
IA 160-177	63-106 67-68

<u>BIC #2</u>	<u>Wiring</u>
Slot 10	65-69
DA 24,25	70-71 59-72 115-118

Chassis A4 RH

<u>BIC #3</u>	<u>Wiring</u>
Slot 2	65-68
DA 26,27	70-71 59-72 69-72 115-118

<u>LP</u>	<u>Wiring</u>
Slot 4	64-66, 82-76
DA = 35	68-69, 84-77 70-72, 87-78

Chassis A3 RH

<u>Disc (Board #1)</u>	<u>Wiring</u>	<u>BTC</u>	<u>Wiring</u>
Slot 3	64-66	Slot 9	65-66
DA = 15	68-69	DA = 20, 21	68-69
	70-72		71-72

Mag Tape - DA = 10, Hardwired on Board #2

6.3 PIM Interrupt Wiring

(Use 30 AWG Twisted Pair)

<u>PIM #1</u>	<u>DA = 40</u>		<u>IA = 100-117</u>		
<u>Signal</u>	<u>From</u>		<u>To</u>		<u>Function</u>
IL00	A3 RH 9-75		A3 LH 3-108		BTC #1 Complete
R	A3 RH 9-76		A3 LH 3-107		
IL01	Reserved				
IL02	A3 LH 10-75		A3 LH 3-104		BIC #2 Complete
R	A3 LH 10-76		A3 LH 3-103		
IL03	A4 RH 2-75		A4 LH 2-77		BIC #3 Complete
R	A4 RH 2-76		A4 LH 2-78		
	A3 LH 2-77		A3 LH 3-110		
R	A3 LH 2-78		A3 LH 3-109		
IL04	Reserved				
IL05	A3 RH 3-113		A3 LH 3-88		Disc "0" Seek Complete
R	A3 RH 3-114		A3 LH 3-87		
IL06	Spare				
IL07	A4 LH 8-104		A4 LH 2-63		MT Motion Complete
R	A4 LH 8-103		A4 LH 2-64		
	A3 LH 2-63		A3 LH 3-86		
R	A3 LH 2-64		A3 LH 3-85		

<u>PIM #2</u>	<u>DA = 43</u>		<u>IA = 166-177</u>	
<u>Signal</u>	<u>From</u>	<u>To</u>	<u>Function</u>	
IL00 thru IL03	Spares			
IL04 R	A3 LH 4-91	A3 LH 13-102	UASC Read Ready	
	A3 LH 4-94	A3 LH 13-101		
IL05 R	A3 LH 4-89	A3 LH 13-88	UASC Write Ready	
	A3 LH 4-90	A3 LH 13-87		
IL06 R	A2(I/O Port) J3-3	A2(I/O Port) J2-75	TTY Read Ready	
	A2(I/O Port) J3-4	A2(I/O Port) J2-76		
IL06 R	A3 RH Slot 13-75	A3 LH Slot 13-112		
	A3 RH Slot 13-76	A3 LH Slot 13-111		
IL07 R	A2(I/O Port) J3-5	A2(I/O Port) J2-77	TTY Write Ready	
	A2(I/O Port) J3-6	A2(I/O Port) J2-78		
IL07 R	A3 RH Slot 13-77	A3 LH 13-86		
	A3 RH Slot 13-78	A3 LH Slot 13-85		

6.4 BIC Delete Wiring

DELETE the BIC wiring Chassis A4, Slot 2 LH to Slot 13 RH, Pins 49, 50, 52, 54, 56, 58 and 60.

6.5 Mag Tape/Disc Interslot Wiring

6.5.1 Mag Tape Wiring

Install mag tape interboard wiring into Chassis A4 LH, Slots 5 to 8 per Wire List No. 95W0271 contained in the Appendix, Section 9.0.

6.5.2 Disc Interboard Wiring

Install the -7510 disc interboard wiring per attached Wire List No. 95W1131 in the specified Chassis -

A3 RH Slot 9 = PMA/BTC #1
A3 RH Slot 6 = Disc. Cont. Board #2
A3 RH Slot 3 = Disc. Cont. Board #1

NOTE: The E-Bus is to be continued across disc controllers.
Re-install per Wire List No. 95W1131.

6.6 N/A

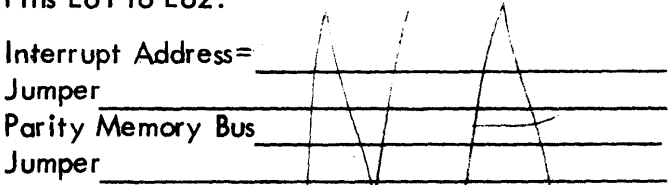
6.7 Mainframe Wiring6.7.1 Central Processor Wiring - refer to 01A1331

1. Install "Processor to Memory A" Jumpers.
2. Memory protect is installed, so jumper Pins F to F.
3. Clock source is WCS clock, jumper Pins J2 to J3
4. Memory Wraparound is for 32K ADD JUMPERS 22C TO 21B & A29 TO 28D.

6.7.2 Control Console - refer to 01A1335

1. Control Disable - to disable all switches, install jumpers between Pins C and E.
2. ABL - RMD ADD jumpers between A-A & B-B

6.7.3 Option Board Wiring - refer to 01A1332

1. PFR Option to be enabled, remove jumpers between E7 and E8, E9 and E10.
2. RTC $FRC = 100 \mu s$, ADD jumper between E13 TO E18,
 $IIC = 10K\Omega$, ADD jumper E13 TO E14
 Disable RTC interrupts on a J MARK instruction.
 Jumper between E11 and E12.
3. Memory Parity DISable this option, ADD jumper clip between Pins E61 to E62.


Interrupt Address= _____
 Jumper _____
 Parity Memory Bus _____
 Jumper _____
4. Memory Protect Memory Bus Selection ADD jumpers for "A" bus selection. ENable this option, ADD jumper clips E98 to E99 and E100 and E101. Memory Map is NOT IN system.
5. Interrupt Clock Setup for interrupt rate of 990. ADD jumpers between Pins E2 and E3, E4 and E5.
6. TTY ENable TTY DELETE jumper E96 to E97.
 Setup TTY for BPS 110, 2 Stop Bits. Install jumpers as follows:

DELETE: E44 to E45

ADD: E20 to E21 E30 to E31 E38 to E39
 E24 to E25 E32 to E33 E40 to E41
 E28 to E29 E36 to E37 E42 to E43
 E107 to E108

7. Memory Time
Out LogicInstall JUMPERS B50 TO B51 A25 TO B49

8. PMA

Data Transfer Mode = 620 compatible mode.

ADD: Jumpers E73-E74, E75-E76, E77-E78, E79-E80.

Hog Mode: NOT USED will control HogMode: DELETE jumper A27 - B27PMA Memory Request - Jumper B25 - C25B Port NOT shared between PMA and CPUADD E89-E90.9. PMA Address
Bits 9-15

ADD Jumpers	<u>B11-C11</u>	<u>B13-C13</u>
	<u>B15-C15</u>	<u>B17-C17</u>
	<u>B19-C19</u>	<u>B21-C21</u>
	<u>B23-C23</u>	

6.7.4 WCS Wiring - refer to 01A1444

1. Device Address - 74, 75. Install jumper clips between E2 and E3, E4 and E5.
2. Page Address - 1. Install jumper clips between E9 and E10, E11 and E12.
3. Fine Clock Output - Install jumper clip between E34 and E35.
4. Memory Request Disable for Micro Step Mode - Install jumper clip between E36 and E37.
5. Page Select Signal - Install jumper clips between E15 and E16.
6. Module 1 Enable - Install jumper clip between E21 and E22.
7. Decoder RAM NOT Present ADD jumper clip between E23 and E24.
8. Control Store Data Driver NO jumper NOT enable interlock control.
9. BCS Entry Table - Setup for 32 words NO jumper clips between E31 and E32, E28 and E29, E25 and E26.
10. Memory Port Selection - Install jumper clips for "A" Port select.
11. Memory DONE YDNM - Install jumper clip between B3-C3
12. Address 15 MAY 15 - Install jumper clip between B1-C1
13. Memory Lockout Control ADD jumper C4-BA
14. Address 15 Control - Install jumper clip between E17 and E18.
15. WCAEN - True if Decoder ROM is Selected - Install jumper clip between E61 and E62.
16. WXCSEN - True if CCS ROM is Selected - Install jumper clip between E27 and E30.

6.7.5 MOS Memory - refer to 01A1323

For bank address selection wiring, refer to attached memory jumper configuration sheets (see Section 9.0, Appendix).

		Slot	
Memory Bank #1	=	0- 7K	1
Memory Bank #2	=	8- 15K	3
Memory Bank #3	=	16-23K	5
Memory Bank #4	=	24-31K	7

Mainframe Chassis
A2

6.7.6 Floating Point Processor

Time Out Enable	-	Jumper B4C-10 to B5B-13
+5V Control	-	Jumper P1A-6 to J7-1
ADD Wire List 95W1100	-	Jumper B4C

6.8 Miscellaneous Special Wiring

1. DELETE all voltage wiring to Slot 2 LH (Front View)
Chassis A4, Slot 13 RH (Front View) Chassis A3
2. DELETE all I/O wiring Slot 11 LH to Slot 12 LH,
Chassis A3 Pins 1-60.
3. SPFA
A2 (I/O Port) J3-7 A2 (I/O Port) J2-115
A3 RH Slot 13-115 A3 LH Slot 12-115
4. Disable BIMES
BIC #2 - Jumper A3 LH Slot 10-93 to Pin 73
BIC #3 - Jumper A4 RH Slot 2-93 to Pin 73
5. Disable BTMES
BTC - Jumper A3 RH Slot 9-96 to Pin 73

7.0 SPECIAL SYSTEM INFORMATION

1. Install Data Save on Power Supply.
2. Setup UASC as follows:

Baud Rate- 9600	Install Jumpers	- E2, E3, E4
Parity - None	DELETE	- E13
Stop Bits - One	Install	- E14
Data Bits - Eight	DELETE	- E15, E16
3. SETUP Buffered I/O as follows:

Pulse Width	10 usec	R10 = 3.9K	C37 = .001 MFD
Bit Configuration	16 Bits		

8.0 CABLE IDENTIFICATION

CABLE DESIGN.	FROM	TO	PART NUMBER	CABLE LENGTH	FUNCTION
X1	A1 J1	A2 J1	53P0658	48"	Fan Power
X2	A1 J4	A2 J2	53P0659	48"	DC Power
X3	A1 J3	A2 J3	53P0780	48"	DC Power
X4	A1 J1	A4 PS	53P0685	60"	AC Sequence
X5	A6 PS	A5 PS	53P0696	60"	AC Sequence
X6	A5 Captive	A3 J30	53P0686	30"	I/O Exp. Power
X7	A6 Captive	A4 J30	53P0686	30"	I/O Exp. Power
X8	A2 P2 (CPU)	A2 P2 (Flt Pt) A2 P2 (WCS)	53P0674-004	Mod	WCS
X9	A2 P3 (DCA)	A2 P3 (Opt)	53P0675-007	Mod	Aux I/O
X10	A2 P3 (CPU)	A2 P3 (Flt Pt) A2 P3 (WCS)	53P0674-004	Mod	WCS
X11	A2 P4 (Flt Pt)	A2 P4 (Opt)	53P0674-006	Mod	Processor
X12	A2 P5 (DCA)	A2 P5 (Opt) A2 P5 (CPU) A2 P5 (WCS) A2 P5 (Flt Pt) A2 P1 (CONS)	53P0676-008	Mod	I/O
X13	A2 P6 (CPU)	A2 P6 (Flt Pt) A2 P6 (WCS) A2 P6 (Opt)	53P0674-006	Mod	WCS
X14	A2 J2 (DCA)	A3 RH Slot 13	53P0715	24"	I/O
X15	A2 P8 (Opt)	C1 (TTY)	53P0777	240"	TTY
X16	A7 P/S	A2 (WCS)	53P0703	72"	FPP Power
X17	A8 P/S	A2 (Flt Pt)	53P0703	72"	WCS Power
X18	A3 RH Slot 12	A3 LH Slot 11	53P0665	60"	I/O Expander Cable

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9.0 APPENDIX

1. Board Layout
2. Cabinet Layout
3. Semiconductor Memory Configuration Sheets (4)
4. PIM Pin Assignment Sheet
5. W/L No. 95W0271 - REV. "A"
6. W/L No. 95W1131 "A"
7. W/L No. 95W1100 "A"
8. DA Wiring Tables
9. PIM DA Wiring Tables